Trident

TVGA9200CXr SUPER VGA CONTROLLER

Features

- Single-chip solution for IBM PC/AT 32-bit VESA Local Bus (VL-Bus)
- Integrated 24-bit true color DAC
- Supports up to 2 MB of DRAM
- Supports 256Kx4, 256Kx8, 256Kx16, and 512Kx8 DRAM chips
- Requires only two 256Kx4 DRAM chips for VGA solution
- Fully hardware compatible with VGA, EGA, and MDA at the register level
- Programmable DRAM timing
- Supports linear addressing
- Built-in data bus transceiver and feature connector support
- Pseudo 16-bit BIOS operation
- Supports 80/132-column text in 25, 30, 43, or 60 rows
- 0.8 µm low power CMOS technology

Benefits

- Provides a versatile and high-performance solution. Compatibility with the VL-Bus standard provides a video subsystem design path for future generation PCs
- Improved performance and reduced footprint for video subsystem designs
- Provides resolutions of 640x480 in 16, 256, 32K, 64K, and 16M colors, 800x600 in 16, 256, 32K and 64K colors, 1024x768 in 16 and 256 colors, and 1280x1024 in 16 and 256 colors
- Many DRAM configurations available for the video memory subsystem
- Highly integrated, small footprint solution
- Chipset will support virtually any VGA, EGA, and MDA application software
- Flexible DRAM interface design
- Eliminates bank switching overhead by linear addressing
- Reduced footprint for video subsystem designs
- Only one 32KB EPROM required to achieve 16-bit BIOS operation
- Many high resolution text modes for spreadsheet and database applications
- Provides high performance and cost savings

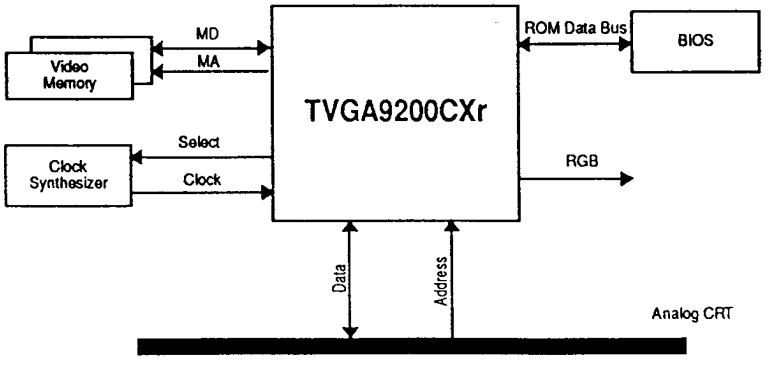


Figure 1. TVGA9200CXr Application Diagram

General Description

The TVGA9200CXr is Trident's high performance, integrated solution for VGA (Video Graphics Array) systems. High performance is achieved by zero-wait state direct memory write, faster base DRAM clock rates, 2 MB linear addressing, and 32-bit VL-Bus interface.

The on-chip command FIFO allows maximum bus transfer speeds for applications like Windows or AutoCAD which write directly to video memory. Performance is further increased by improved DRAM access. Linear addressing eliminates bank switching overhead for high resolution drivers. A VL-Bus interface eliminates data transfer bottlenecks that are common with standard PC buses. The VL-Bus interface can provide performance improvement up to 30% greater than that of a standard TVGA9200CXr PC/AT bus solution.

The TVGA9200CXr is also a very versatile and integrated solution. The integrated DAC provides support for a true color 640x480 mode, 800x600-32K/64K color mode, and non-interlaced 1024x768-16/256 color modes. The integrated DAC combined with the integrated data bus transceivers and feature connector support mean that a complete video subsystem solution can be achieved by adding only DRAM and a clock synthesizer.

Programmable DRAM timing allows the designer to optimize the TVGA9200CXr DRAM interface for the particular speed DRAM chosen for a design. 2 MB DRAM supports enables images up to 1280x1024 in 16 colors to be stored in on-board DRAM while another image is displayed on screen. Display support for Super VGA,VGA, EGA, and MDA monitors assures TVGA9200CXr solutions can be matched up with virtually any monitor on the market.

Compatibility

The TVGA9200CXr is fully compatible with all standard IBM VGA modes, EGA and MDA modes, and allows:

- Use of application software that uses any of the above modes
- Emulation of EGA and MDA modes on a VGA monitor

Extended Graphics and Text Modes

Extended graphics modes support includes:

- 640x480 in 16.8M million colors
- 640x400, 640x480, and 800x600 in 32K or 64K colors
- 640x400, 640x480, 800x600, 1024x768 (interlaced or non-interlaced), and 1280x1024 (interlaced) in 256 colors from a palette of 256K colors or 16M colors
- 800x600, 1024x768, and 1280x1024 (interlaced or non-interlaced) in 16 colors from a palette of 256K or 16M
- 1024x768 in 4 colors from a palette of 256K or16M
- Extended text modes offer 80-column text with 30, 43 , and 60 rows; and 132-column text with 25, 30, 43, and 60 rows

Hardware Features

The TVGA9200CXr supports the 32-bit VL-Bus. The TVGA9200CXr offers an auto-sensing feature which allows it to function in different CPU clock speed.

A CPU command FIFO allows fast CPU write operations. On the display side, maximum DRAM

clock speed has improved, and linear addressing eliminates bank switching overhead for all display resolutions.

The chip allows programmable DRAM timing and supports 256Kx4, 256Kx8, 256Kx16, and 512Kx8 DRAM. Table 1 outlines the amount and speed of Fast Page Mode 256Kx4 DRAM required to implement the 16-, 256-, 32K-, and 16M-color modes. For other types of DRAM, typically 80ns speed is required. The DRAM speed requirements are based on the default DRAM timing parameters.

Table 1. 16, 256, 32K, 64K, and 16M-Color DRAM Requirements

	Colors				DRAM Count				Speed ns	
Resolution	16	256	32K[1]	16M	2	4	8	16	100	80
Standard VGA	•				•					•
640x480		•				•				•
640x480			•				•		•	
640x480				•						•
800x600	•				•					•
800x600		•					•		•	
800x600			•				•			•
1024x768 (Interlaced)	•					•			•	
1024x768 (Non-interlaced)	•					•				•
1024x768 (Interlaced)		•					•		•	
1024X768 (Non-interlaced)		•					•			•
1280x1024 (Non-interlaced)	•						•			•
1280x1024 (Interlaced)		•						•		•

[1]Same DRAM requirement for 64K color

Software Drivers Supported

Extended graphics and text modes are supported by software application drivers developed by Trident. The following applications are supported:

- AutoCAD
- Autoshade
- CADKEY
- Framework
- GEM
- Lotus
- MS Windows
- MS Word
- P-CAD
- Symphony
- Ventura
- VersaCAD
- WordPerfect
- Wordstar
- OS/2
- SCO X-Windows (contact SCO)

Contact Trident for the latest high-resolution driver releases.

TVGA9200CXr Applications

The TVGA9200CXr works with your hardware to allow you to develop a high performance, integrated video subsystem. The small footprint design is ideal for motherboard applications and high performance VL-Bus add-on cards.

A minimum configuration requires a TVGA9200CXr, one 256Kx16 DRAM chips, TCK9004 clock synthesizer, 32KB EPROM, 15-pin connector, 14.318 MHz crystal, jumpers, and miscellaneous ferrite beads, capacitors, resistors.

TVGA9200CXr Components

The TVGA9200CXr consists of eight major components: Sequencer, CRT Controller, Graphics Controller, Attribute Controller, DAC, Host Bus Interface, Display Memory Bus Interface and Command FIFO. These components are used to generate video output and timing for video memory and the monitor.

Sequencer

The sequencer provides basic memory timing for DRAM interfacing, and a character clock for the CRTC and for controlling regenerative memory fetch. The sequencer uses a 64 byte video cache to let the CPU access display memory during active display intervals. Video data from the cache can be output to the video screen while the CPU accesses video memory. This greatly increases performance over standard implementations for CPU access.

CRT Controller

The CRT (Cathode Ray Tube) Controller provides complete control for horizontal and vertical synchronous timing, address interface between video memory and display screen, cursor and underline timing, and refresh addressing for dynamic RAMs.

Graphics Controller

During the active display interval, the Graphics Controller directs data from video memory to the Attribute

Controller. In graphics modes, memory data is formatted into serialized form and sent to the Attribute Controller. In text mode, the parallel attribute byte goes directly to the Attribute Controller without going through the Graphics Controller. During video memory read/write operations, the Graphics Controller acts as an interface to the CPU. The Graphics Controller can perform logic operations on memory data before it reaches the display memory or system data bus.

Attribute Controller

The Attribute Controller takes in data from video memory and formats it for output on the display monitor. In addition, the Attribute Controller takes care of blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table. The attribute code is used to determine character color, blinking, bold, etc. In graphics mode, the Graphics Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the DAC. Here it is used as an address to the 18/24-bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.

DAC

The integrated true color DAC provides support for 640x480-16, 256, 32K, 64K, and 16M color modes, 800x600-16, 256, 32K, and 64K color modes, 1024x768-16 and 256 color modes, and 1280x1024-16 and 256 color modes. A 256K or 16M color palette is selectable. True color and 15/16-bit per pixel modes may bypass the color palette look-up table, or be routed through the color look up table (e.g. for applications which require gamma correction). The DAC module outputs RGB analog signals to directly drive an analog VGA or Super VGA monitor.

Host Bus Interface

The TVGA9200CXr supports the 32-bit VL-Bus by setting or resetting select configuration bits during the system reset time. The configurations, such as, Type A/B of VL-Bus transfer, Device timing, and VL-Bus time base can be set by the configuration bits. Please refer to Table 2 for details.

The TVGA9200CXr video BIOS is located at C0000 - C7FFF. The BIOS PROM data width can be configured as 16-bit or 8-bit at system reset time by pulling MD7 high or low, respectively. If the on-board BIOS is not used, the PROM chip(s) can be disabled by pulling MD6 low at system reset time.

Display Memory Bus Interface

The TVGA9200CXr can address up to 2MB of video memory depending on the mode (text or graphics). The TVGA9200CXr provides a bus interface for the video display DRAM. The interface provides address multiplexing, data multiplexing, refresh, and $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals. Nineteen address pins (MA9, MAA8-MAA0 and MAB8-MAB0 for Bank A and B) and 32 data pins (MD31-MD0) are available for display memory.

Command FIFO

The FIFO also greatly enhances memory write performance when connected to the VL -Bus. Each CPU write data will be stored in the FIFO without actually being written into memory so that CPU does not have to wait when the memory is busy in sending output. When the memory bus is available, data is written into memory from the FIFO.

MD & RMD Defintions at System Reset

Table 2, 3 and 4 list the definition for MD29-MD15, MD7-MD0 and RMD7-RMD0 at system reset.

Table 2. MD29-MD16 Definitions

MD	Logic Value[1]	Definition
MD30	0	Used for crippled 512Kx8 DRAM (MA9 is forced to logical 1)
	1	Default
MD29	0	Configured as 10 bit row and 8 bit column address for 256Kx16 asymmetric DRAM
	1	Default
MD28	0	Pins $\overline{WE3}$-$\overline{WE0}$ defined as $\overline{CASA3}$-$\overline{CASA0}$.
	1	Default
MD27-MD24	NA	Sets base address of the linear address window
MD23	-	Reserved
MD22	0	Type B transfer VL-Bus operation (CPUCLK > 33MHz)
	1	Type A transfer VL-Bus operation (CPUCLK <= 33MHz)
MD21	-	Reserved
MD20	0	Selects 1x clock as VL-Bus time base
	1	Selects 2x clock as VL-Bus time base
MD19-MD18	00	Supports 256Kx16 DRAM Pin 134 is used as MA9 for 2MB case. Pin 134 not used for 1MB case.
	01	Supports 512Kx4 or 512Kx8 DRAM. Pin 134 is used as MA9.
	10	Supports 256Kx4 or 256Kx8 DRAM up to 2MB. Pin 134 is used as $\overline{MCASB}$.
	11	Supports 256Kx4 or 256Kx8 DRAM up to 1MB. Pin 134 is used as $\overline{NMI}$.
MD17	0	Selects LA23-20
	1	Selects SA19-17, $\overline{HAD}$
MD16	-	Reserved
MD15	0	Select 386SX VL-Bus
	1	Select 486DX/SX or 386DX VL-Bus

[1]Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

Table 3. MD7-MD0 Definitions (information contained in Power Up Mode Register 2, 3C5.0F)

MD	Logic Value[1]	Definition
MD7	0	8-bit BIOS
	1	16-bit BIOS
MD6	0	ROM disable
	1	ROM enable
MD5	0	I/O port at 2xx
	1	I/O port at 3xx
MD4	-	Reserved
MD3-MD0	(see Note 2)	Dip switch settings

[1]Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.
[2]Data is read into a 4-bit register. The data values can be used by the BIOS or application software.

Table 4. RMD7-RMD0 Definitions (information contained in Configuration Port Register 1, 3C5.0C)

MD	Logic Value[1]	Definition
RMD7	0	8-bit video memory
	1	16-bit video memory
RMD6-RMD5	00	Reserved
	01	8-bit DRAM data bus
	10	16-bit DRAM data bus
	11	32-bit DRAM data bus
RMD4	0	Selects 46E8 for port control
	1	Selects 3C3 for port control
RMD3	-	Reserved
RMD2	1	Reserved
RMD1	0	Standard BIOS wait states
	1	Extended BIOS wait states
RMD0	0	Slow mode address decode (Uses latched address)
	1	Fast mode address decode (Uses unlatched address)

[1]Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor. No pull-up resistor required for a Logical 1 value.

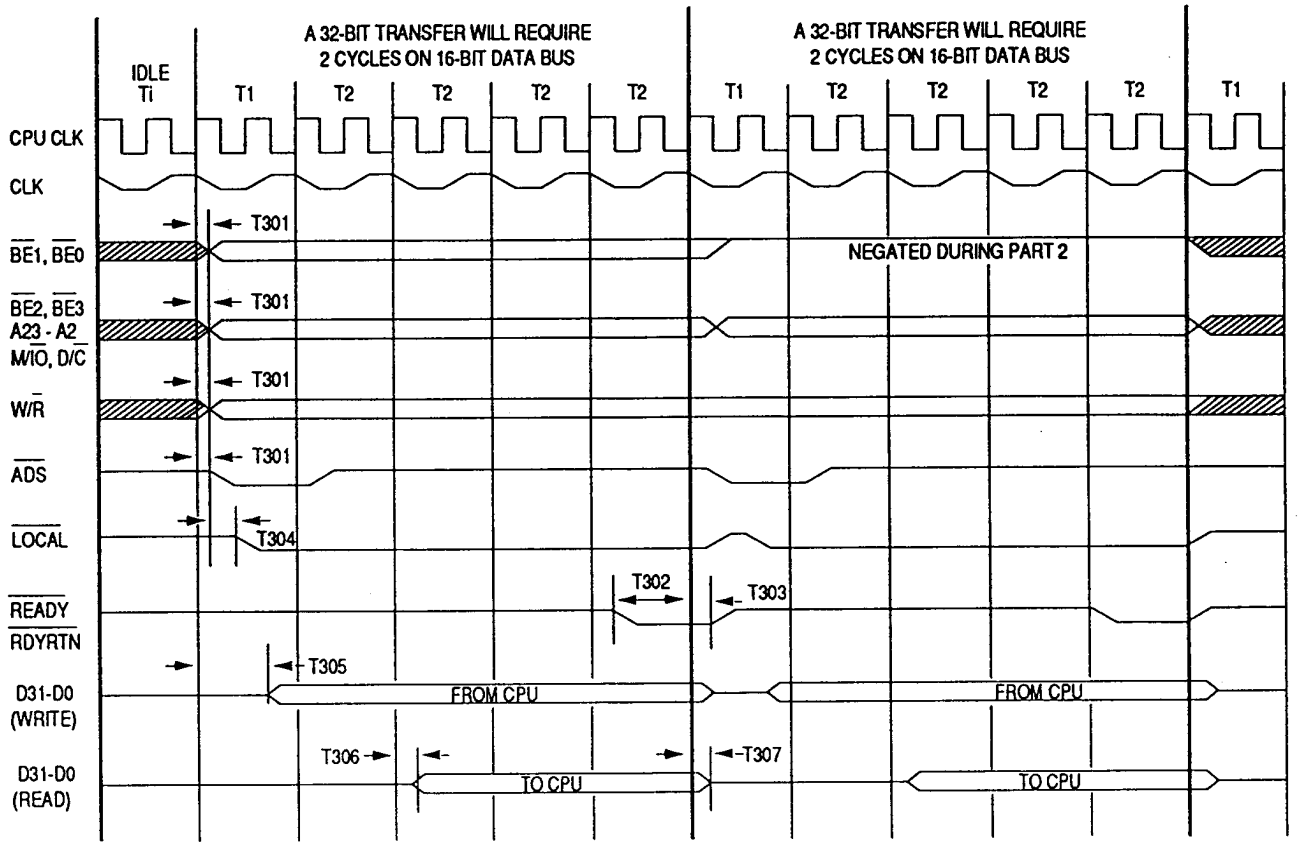


Figure 2. 386DX and 386SX VL-Bus Timing Type A Transfer

Table 5. 386DX and 386SX VL-BusTiming Type A Transfer (33MHz CPU)

SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	30	
T1	1st clock period	30	
T2	2nd clock period	30	
T301	$\overline{ADS}$, A25-A2(386DX)/A25-A1(386SX), M/$\overline{IO}$, D/$\overline{C}$, $\overline{BE3}$-$\overline{BE0}$ valid delay	4	15
T302	$\overline{READY}$ setup time	20	
T303	$\overline{READY}$ hold time	4	
T304	$\overline{LOCAL}$ ready to $\overline{ADS}$ low		20
T305	Write data valid delay	7	24
T306	Read data bus drive to CPU CLK rising edge		5
T307	Read data hold time	3	

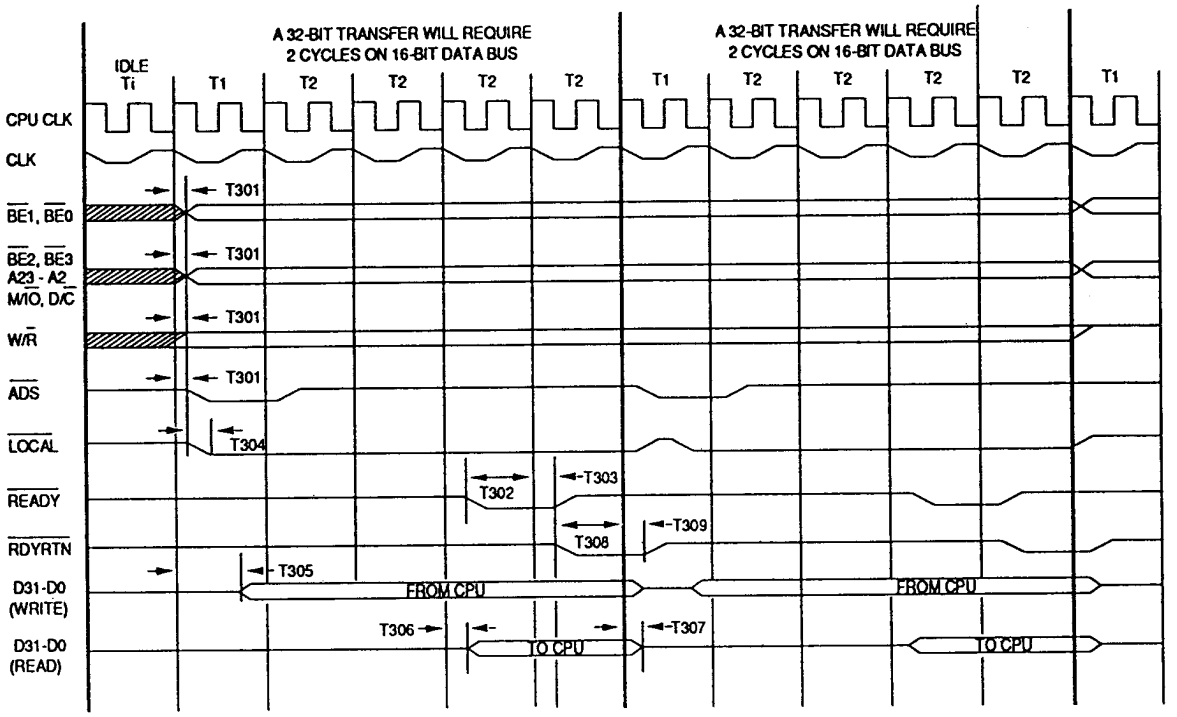


Figure 3. 386DX VL-Bus Timing Type B Transfer

Table 6. 386DX VL-Bus Timing Type B Transfer (33 MHz CPU)

SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	30	
T1	1st clock period	30	
T2	2nd clock period	30	
T301	$\overline{ADS}$, A25-A2, M/$\overline{IO}$, D/$\overline{C}$, $\overline{BE3}$-$\overline{BE0}$ valid delay	4	15
T302	$\overline{READY}$ setup time	20	
T303	$\overline{READY}$ hold time	4	
T304	$\overline{LOCAL}$ ready to $\overline{ADS}$ low		20
T305	Write data valid delay	7	24
T306	Read data bus drive to CPU CLK rising edge	5	
T307	Read data hold time	3	
T308	$\overline{RDYTRN}$ setup time (for 9200CXr & CPU)	7	
T309	$\overline{RDYRTN}$ hold time (for TVGA9200CXr & CPU)	4	

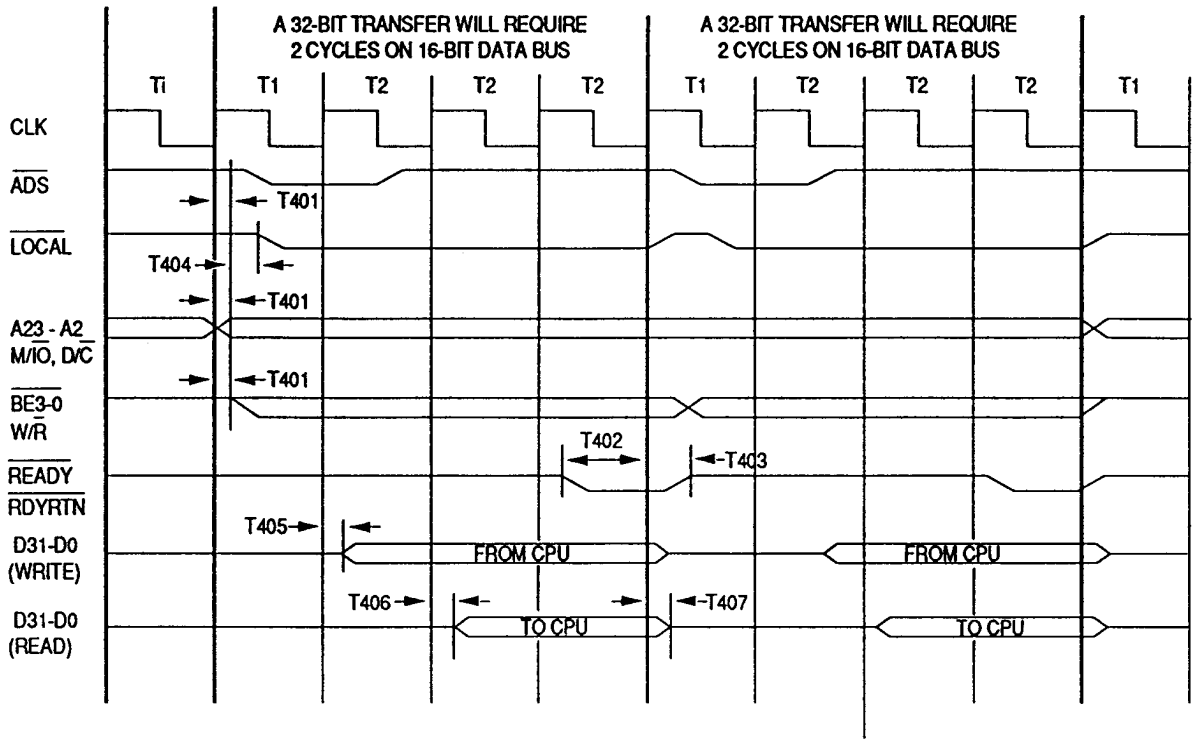


Figure 4. 486SX and 486DX VL-Bus Timing Type A Transfer

Table 7. 486SX and 486DX VL-Bus Timing Type A transfer (33 MHz CPU)

SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	30	125
T1	1st clock period	30	125
T2	2nd clock period	30	125
T401	$\overline{ADS}$, A25-A2, M/$\overline{IO}$, D/$\overline{C}$, $\overline{BE3}$-$\overline{BE0}$ valid delay		20
T402	$\overline{READY}$ setup time for CPU	20	

SYM	Description	Min (ns)	Max (ns)
T403	$\overline{READY}$ hold time for CPU	4	
T404	$\overline{LOCAL}$ ready to $\overline{ADS}$ low		20
T405	Write data valid delay	3	18
T406	Read data bus drive to CPU CLK rising edge		5
T407	Read data hold time	3	

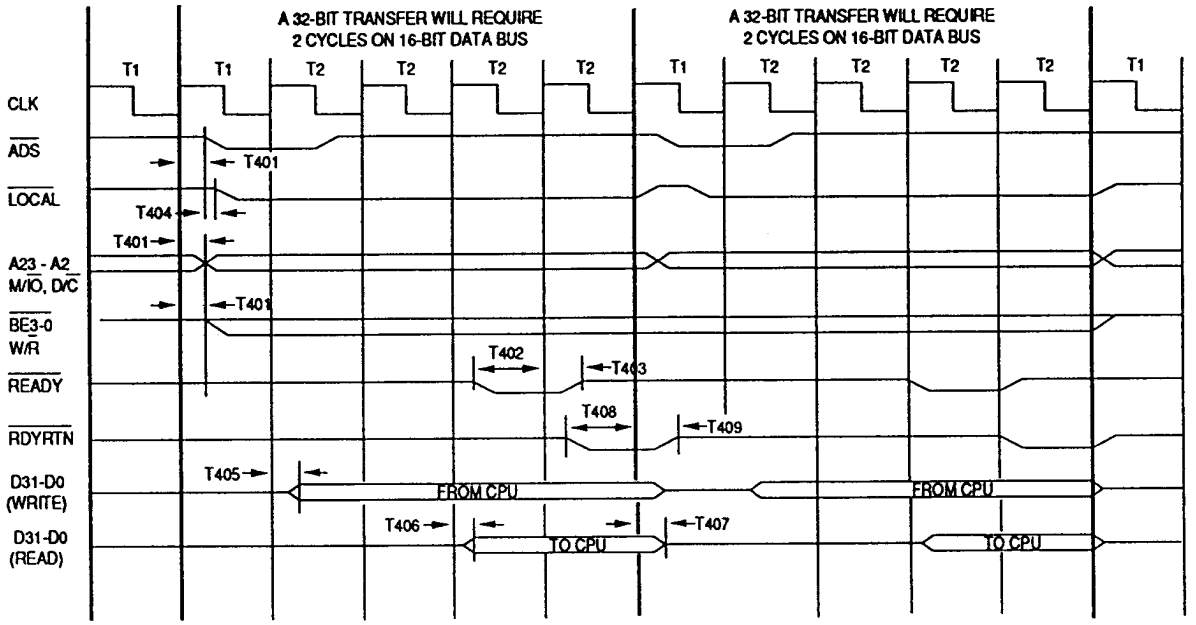


Figure 5. 486SX and 486DX VL- Bus Timing Type B Transfer

Table 8. 486SX and 486DX VL-Bus Timing Type B Transfer (50 MHz CPU)

SYM	Description	Min (ns)	Max (ns)
Ti	Idle period	20	62.5
T1	1st clock period	20	62.5
T2	2nd clock period	30	62.5
T401	$\overline{ADS}$, A25-A2, M/$\overline{IO}$, D/$\overline{C}$, $\overline{BE3}$-$\overline{BE0}$ valid delay	3	12
T402	$\overline{READY}$ setup time	10	
T403	$\overline{READY}$ hold time	4	
T404	LOCAL ready to $\overline{ADS}$ low		20
T405	Write data valid delay	3	12
T406	Read data bus drive to CPU CLK rising edge		5
T407	Read data hold time	3	
T408	$\overline{RDYRTN}$ setup time (for TVGA9200CXr & CPU)	5	
T409	$\overline{RDYRTN}$ hold time (for TVGA9200CXr & CPU)	2	

Table 9. Vertical and Horizontal Timing

Mode	CLK (MHz)	Type	Display	Max Colors	VERTICAL TIMING (ms) T1	T2	T3	T4	T5	Polarity	HORIZONTAL TIMING (µs) T6	T7	T8	T9	T10	T11	Polarity
0,1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.477	2.066	3.813	31.778	-
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
56	40.0	A/N	132x60	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5B[2]	50.35	APA	800x600	16	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
5C[3]	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	+	6.356	25.422	0.556	1.668	4.131	31.778	-
5C[4]	25.2	APA	640x400	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
5D[3]	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.556	1.668	4.131	31.778	-
5D[4]	25.2	APA	640x480	256	1.430	12.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
5E	57.3	APA	800x600 (I)	256	1.073	10.057	0.151	11.130	0.067	-	5.587	27.937	0.139	1.676	3.771	33.524	+
5E	36.0	APA	800x600 (NI)	256	0.711	17.067	0.028	17.778	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5E	50.3	APA	800x600 (NI)	256	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
5F	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	0.204	1.260	3.956	28.151	+
5F	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
5F[2]	75.0	APA	1024x768	16	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024x768(I)	4	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	1.069	1.782	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	+	9.265	17.105	-1.782	4.633	4.811	26.370	+
62	44.9	APA	1024x768 (I)	256	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	-.178	2.851	2.316	28.151	+
62	65.0	APA	1024x768 (NI)	256	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
62[2]	75.0	APA	1024x768	256	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
63	75.0	APA	1280x1024	16	1.120	10.705	0.379	11.835	0.084	+	3.965	17.035	0.255	0.205	3.400	21.000	+
64	75.0	APA	1280x1024	256	1.120	10.705	0.379	11.835	0.084	+	3.965	17.035	0.255	0.205	3.400	21.000	+
6C	75.0	APA	640x480	16M	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
70/71[1]	77.0	APA	512x480	32/64K	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
74/75[1]	50.35	APA	640x480	32/64K	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
76/77[1]	72.0	APA	800x600	32/64K	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-

[1]Same timing for 32K and 64K color modes

[2]Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801

[3]Mode used for 16-bit memory interface

[4]Mode used for 32-bit memory interface

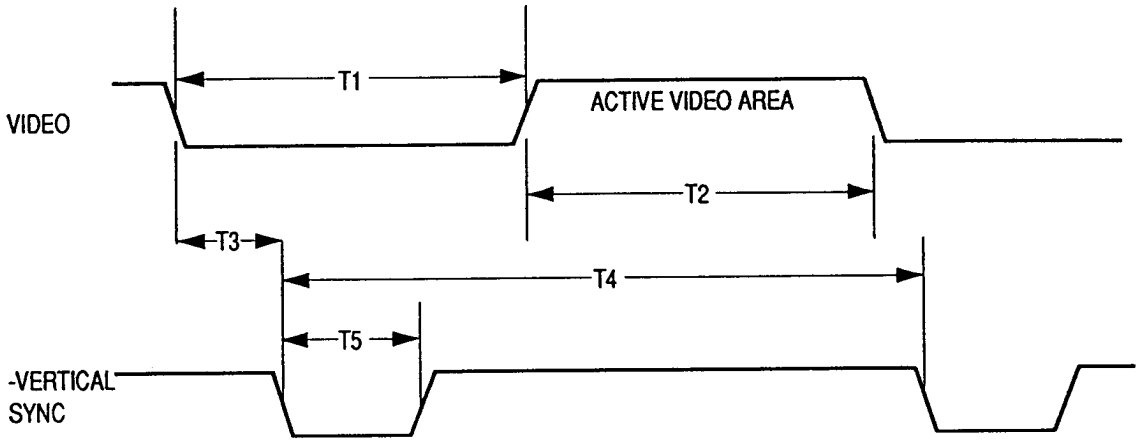


Figure 6-A. Vertical Timing (ms)

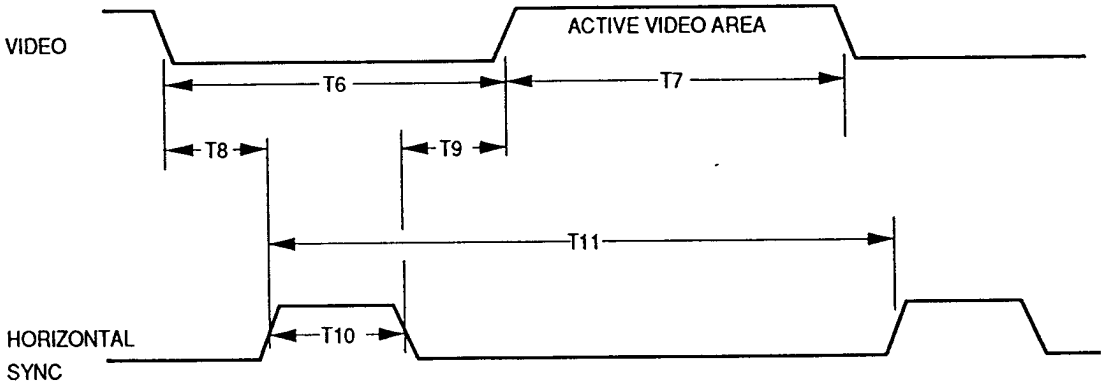


Figure 6-B. Horizontal Timing (μs)

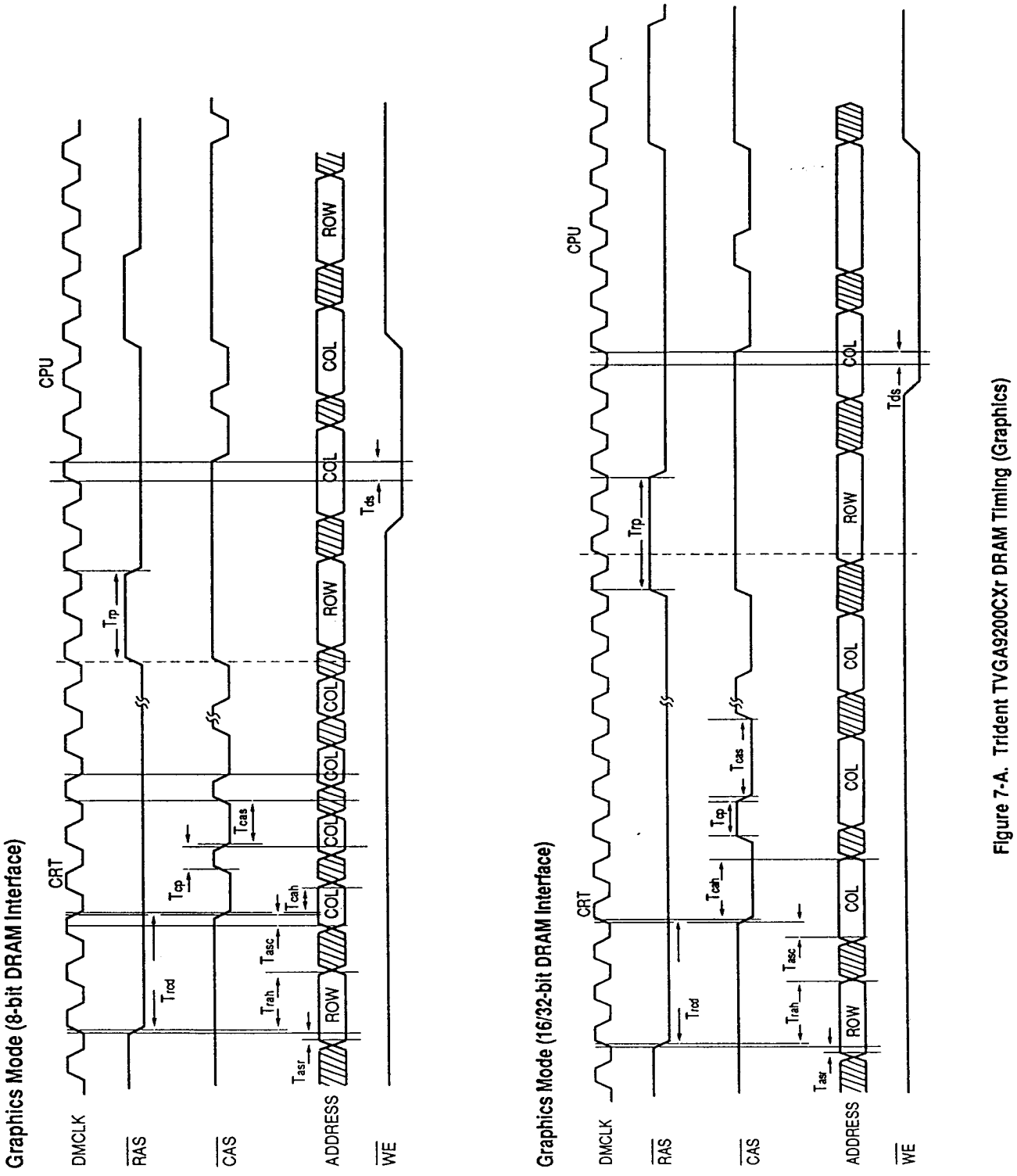


Figure 7-A. Trident TVGA9200CXr DRAM Timing (Graphics)

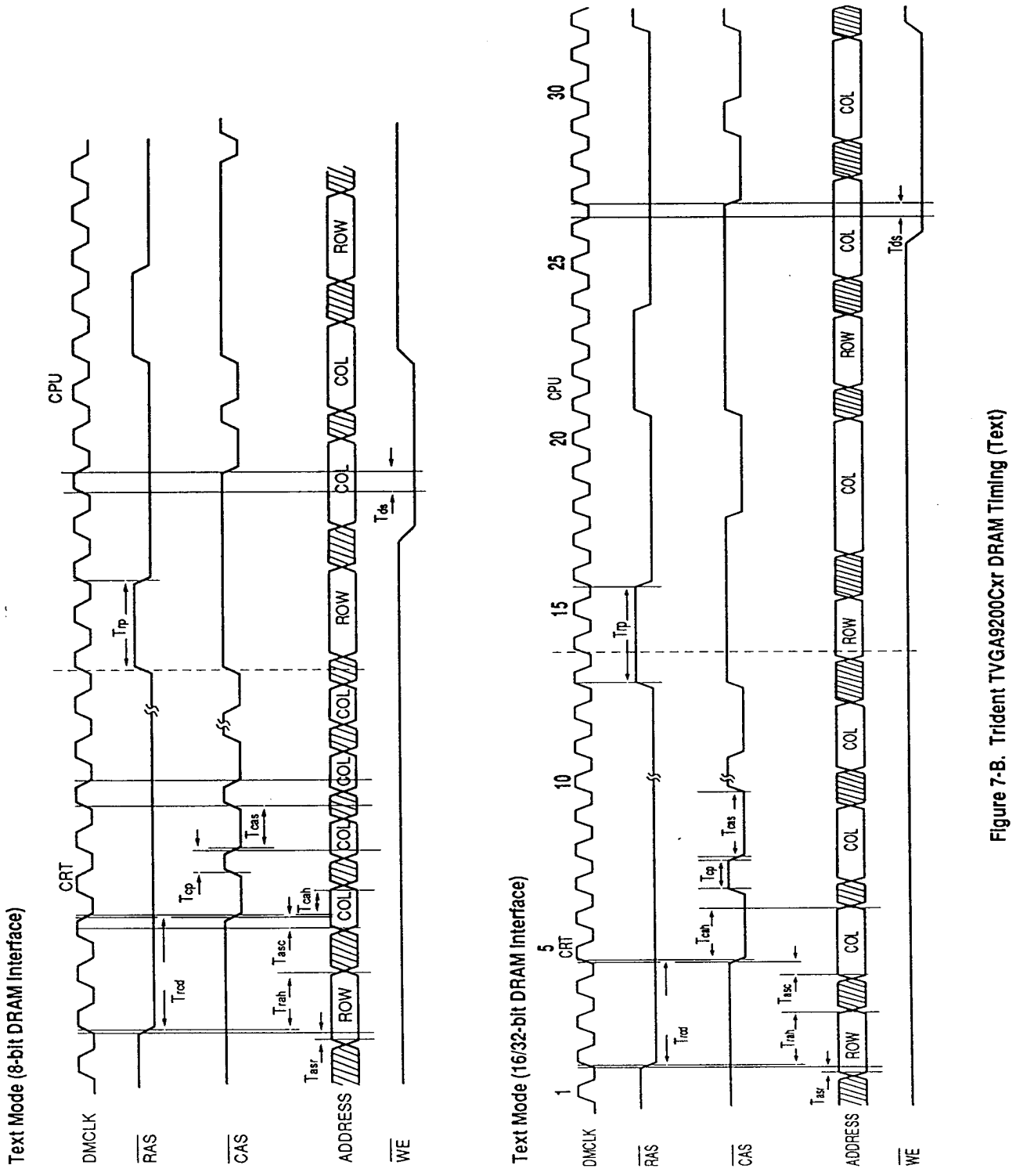


Figure 7-B. Trident TVGA9200Cxr DRAM Timing (Text)

Table 10. Worst Case Memory Timing Parameters

Parameter	8 bit DRAM Interface	16 bit DRAM Interface	32 bit DRAM Interface
Trcd 1	2.5t + 1.5ns	3t + 1.5ns	3t + 3ns
Trah 2	1.5t + 2ns	2t + 2ns	2t + 2ns
Tasr 3	≥ 0	≥ 0	≥ 0
Tasc 4	≥ 0.5t	≥ t	≥ t
Tcah 5	t	2t	2t
Tcp 6	0.5t - 2.5ns	t - 5ns	t - 6ns
Tcas 7	t - 4ns	2t - 6.5ns	2t - 10ns
Tds 8	≥ 0	≥ 0	≥ 0
Trp 9	2t - 1.5ns	3t - 4ns	3t - 6ns
Test Load	25pf	50pf	85pf

[1](t=1/DMCLK. Note, VCLK becomes DMCLK when VCLK > DMCLK)

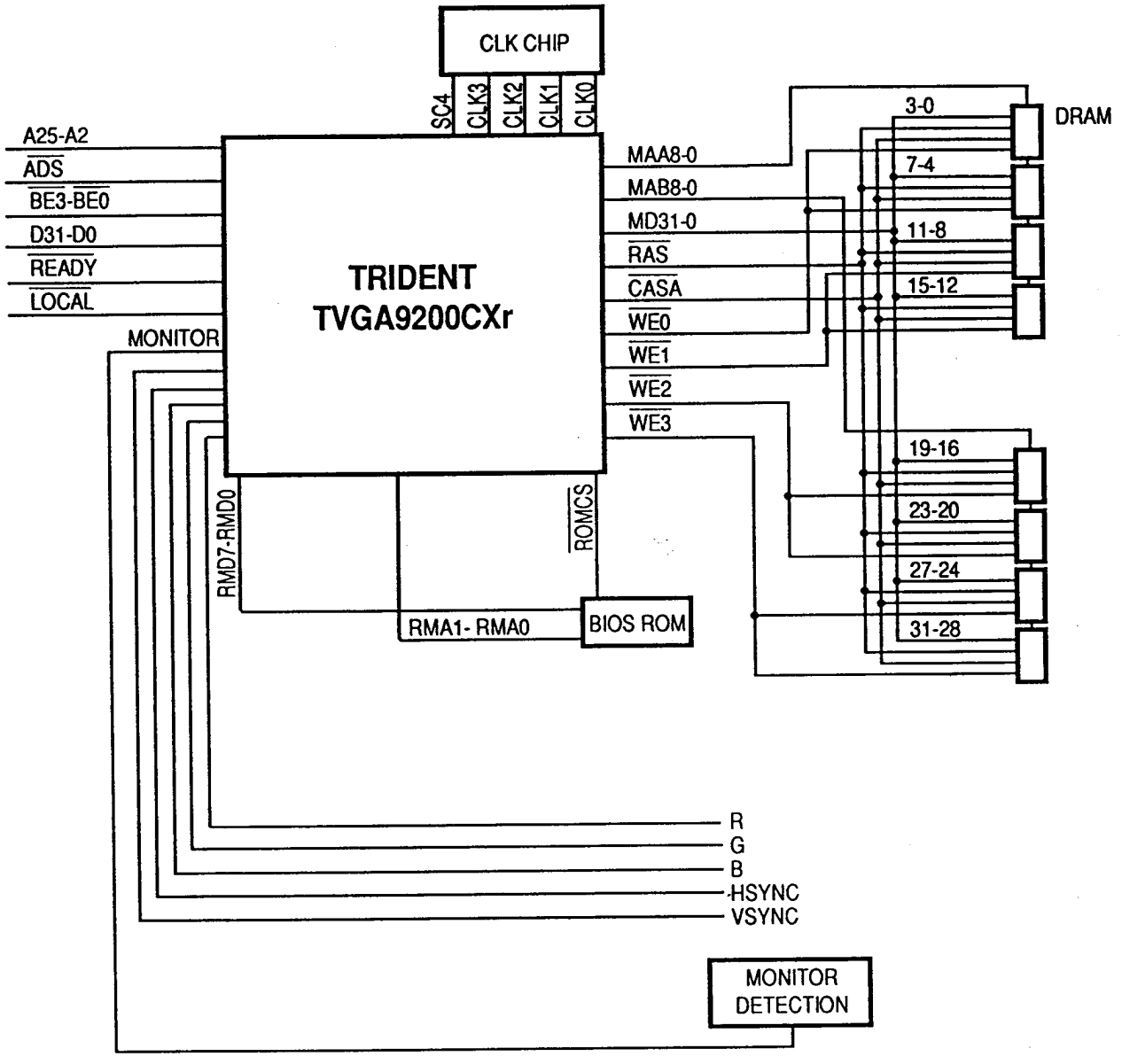


Figure 8. Application For Eight 256Kx4 DRAM (486DX VL-Bus)

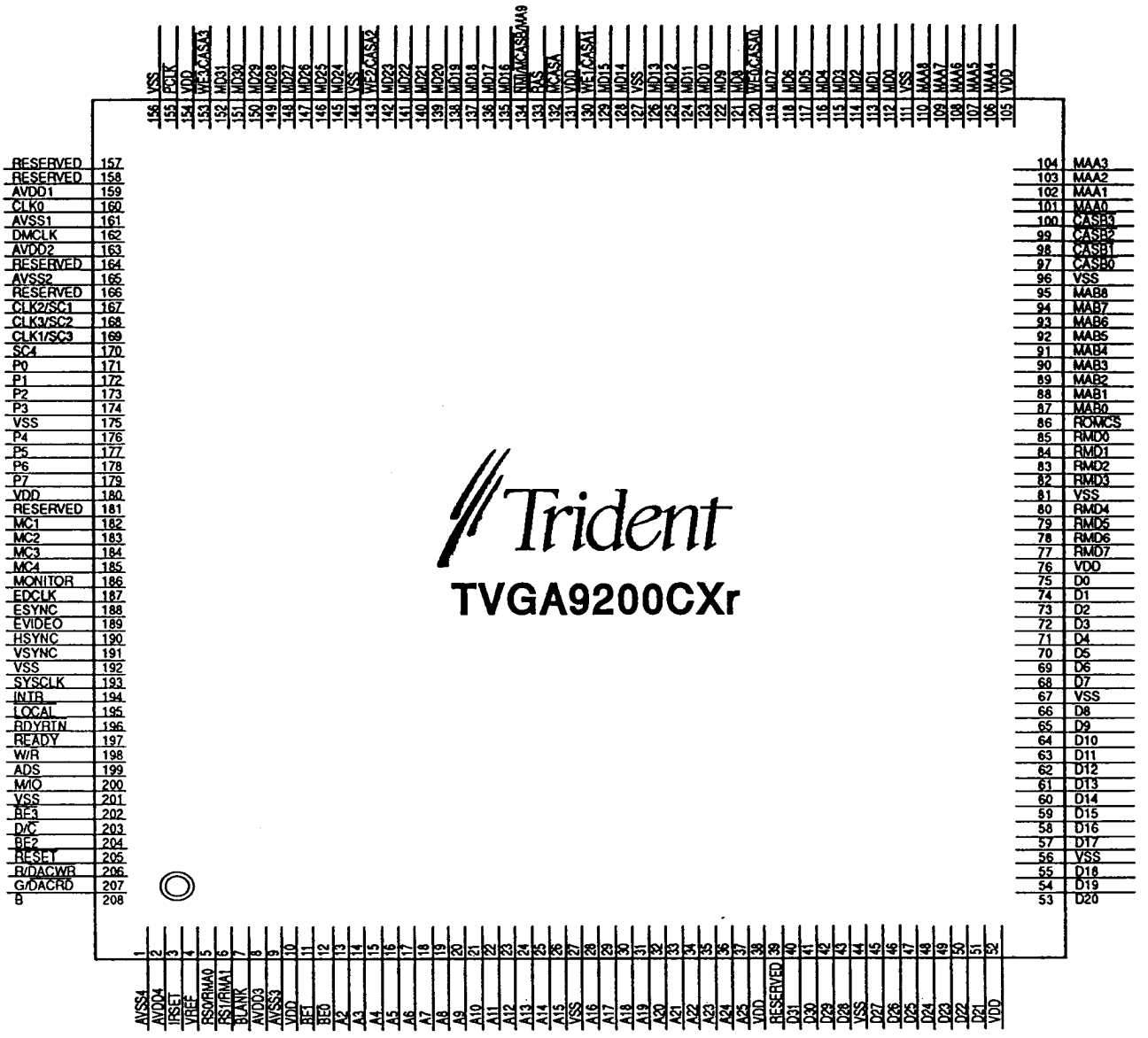


Figure 9. TVGA9200CXr Pin-Out (VL-Bus)

Table 11. TVGA9200CXr Pin Description - Continued

Pin	Pin Type	Pin Number	Description
Host Interface - VL-Bus Signals			
D/$\overline{C}$	I	203	Local bus data or control cycle
M/$\overline{IO}$	I	200	Local bus memory or I/O cycle
W/$\overline{R}$	I	198	Local bus write or read access
$\overline{READY}$	O	197	Local bus cycle ready
$\overline{ADS}$	I	199	System status
SYSCLK	I	193	System clock
A25-A2/A1	I	37-28,26-13/204	Address bus, bit 25 to bit 2 (386DX, 486DX)/ bit 23 to bit 1 (386SX)
$\overline{BE3}$-$\overline{BE2}$	I	202,204	Byte enable for D31-D24 and D23-D16 (386DX, 486DX only)
$\overline{BE1}$-$\overline{BE0}$	I	11,12	Byte enable for D15-D8 and D7-D0
$\overline{RDYRTN}$	I	196	Ready return; terminate Local bus transaction
$\overline{BS16}$	O	181	Not connected
D31-D0	I/O	40-43,45-51, 53-55,57-66,68-75	Data bus, bit 31 to bit 0
INTR	O	194	Interrupt request
$\overline{RESET}$	I	205	System reset (active low); the falling edge latches configuration information into internal registers from memory data lines and RMD7-RMD0
$\overline{LOCAL}$	O	195	CPU Local Bus cycle. A logical 0 indicates a Local Bus cycle.
Common Bus Signals			
RESERVED	I	39	Default to Logical 0
$\overline{NMI}$/$\overline{MCASB}$/MA9	O	134	Non-maskable interrupt/drive $\overline{CAS}$ for 2MB 256Kx4 or 256Kx8 DRAM/tenth address pin for 512Kx4 or x8, or 2MB 256Kx16 DRAM
Display Memory Interface			
$\overline{MCASA}$	O	132	Column address strobe for Bank A
$\overline{WE3}$-$\overline{WE0}$/ $\overline{CASA3}$-$\overline{CASA0}$	O	153,143,130,120	Write enable pins 3-0/Column access strobe pins 3-0 for Bank A (for 1MB DRAM configurations which require multiple $\overline{CAS}$)
$\overline{CASB3}$-$\overline{CASB0}$	O	100-97	Column access strobe pins 3-0 for Bank B (for 2MB DRAM configurations which require multiple $\overline{CAS}$)
$\overline{RAS}$	O	133	Row address strobe
MAA8-MAA0	O	110-106,104-101	Multiplexing address bus of display memory Bank A
MAB8-MAB0	O	95-87	Multiplexed address bus of display memory Bank B
MD31-MD0	I/O	152-145, 142-135, 129-128, 126-121, 119-112	Memory data bus (bit 31 to bit 0)
DMCLK	I	162	DRAM clock
MC4-MC1	O	185-182	DRAM clock select pins for external clock synthesizer

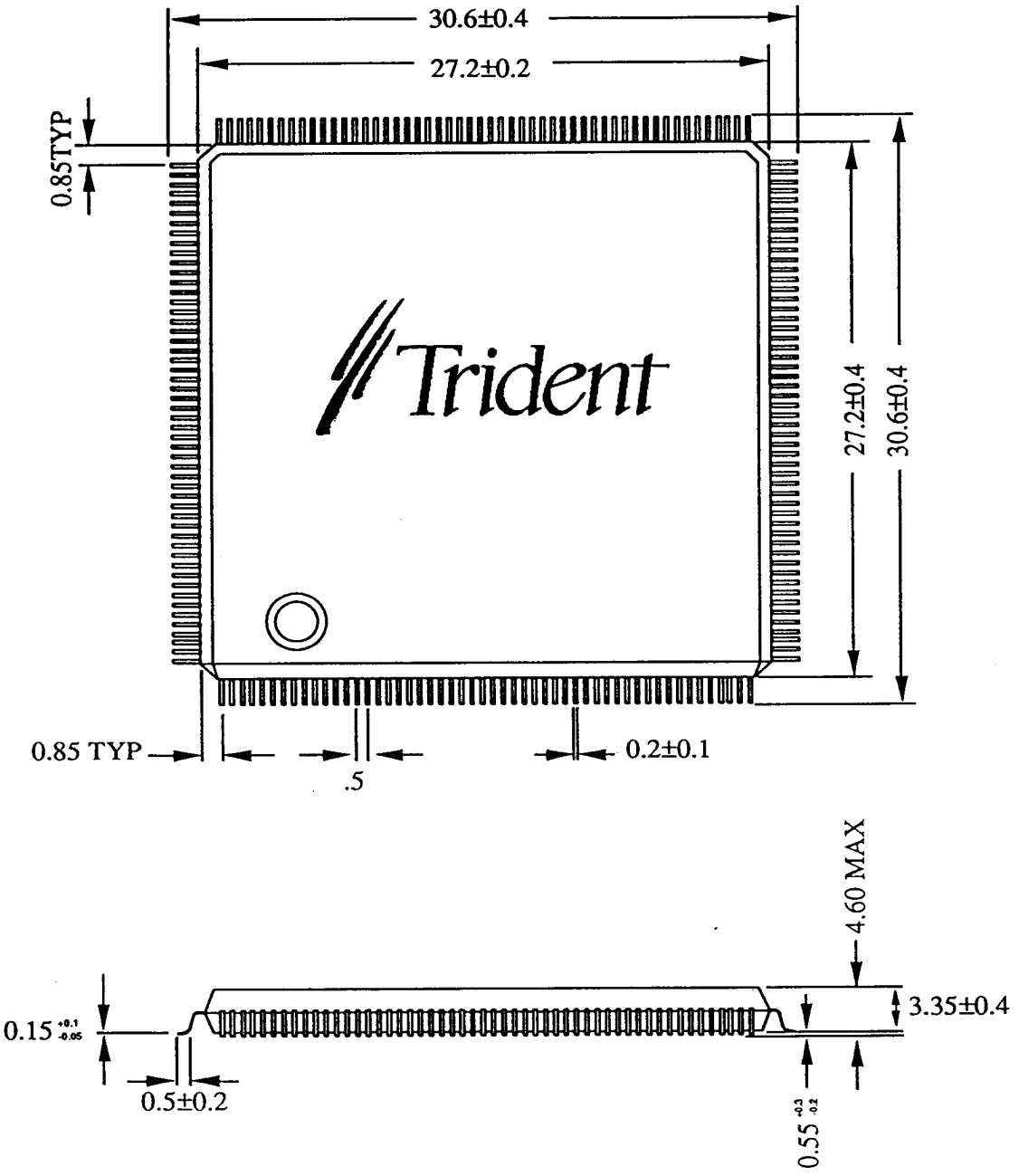
Table 11. TVGA9200CXr Pin Description - Continued

Pin	Pin Type	Pin Number	Description
Video Interface			
VSYNC	O	191	Vertical synchronization pulse, polarity programmable
HSYNC	O	190	Horizontal synchronization pulse, polarity programmable
RMD7-RMD0	I/O	77-80, 82-85	ROM/DAC data bus bits 7 - 0
RS1/RMA1	I/O	6	DAC register select bit 1 / ROM address bit 1 (ROM for VL-Bus enabled)
RS0/RMA0	I/O	5	DAC register select bit 0 / ROM address bit 0 (ROM for VL-Bus enabled)
P7-P0	I/O	179-176, 174-171	Pixel data address bits 7-0 from feature connector or for external DAC
PCLK	I/O	155	Pixel clock input from feature connector/Pixel clock output for external DAC
$\overline{\text{BLANK}}$	I/O	7	Blank input from feature connector/Blank output for external DAC
R/$\overline{\text{DACWR}}$	O	206	Red output/Write strobe for external DAC
G/$\overline{\text{DACRD}}$	O	207	Green output/Read strobe for external DAC
B	O	208	Blue output
SA1-SA0	O	204,11	Used as $\overline{\text{BE}}$ inputs from the CPU bus
VREF	I	4	External voltage reference pin
IRSET	I	3	Full scale RGB output voltage adjust control
Clock Synthesizer Interface			
CLK1/SC3	I/O	169	Video clock input 1 from external oscillator/Clock select output 3 to external clock synthesizer
CLK2/SC1	I/O	167	Video clock input 2 from external oscillator/Clock select output 1 to external clock synthesizer
CLK3/SC2	I/O	168	Video clock input 3 from external oscillator/Clock select output 2 to external clock synthesizer
CLK0	I	160	Video clock input from an external oscillator or clock synthesizer
SC4	O	170	Clock select output 4 to an external clock synthesizer
BIOS Interface			
RMD7-RMD0	I/O	85-82, 80-77	ROM/DAC data bus bits 7 - 0
$\overline{\text{ROMCS}}$	O	86	BIOS EPROM chip select
RS0/RMA0	O	5	DAC register select bit 0/ROM address bit 0 (ROM for VL-Bus enabled)
RS1/RMA1	I/O	6	DAC register select bit 1/ROM address bit 1 (ROM for VL-Bus enabled)
Other External Interfaces			
EVIDEO	I	189	External pixel data enable (feature connector)
EDCLK	I	187	External clock enable (feature connector)

Table 11. TVGA9200CXr Pin Description - Continued

Pin	Pin Type		Description
ESYNC	I	188	External sync enable (feature connector)
MONITOR	I	186	Monitor type detect (analog monitors)
Power Pins			
AVSS4-1	GND	1, 9, 165, 161	Analog Ground
AVDD4-1	PWR	2, 8, 163, 159	Analog Power
VSS	GND	27, 44, 56, 67, 81, 96, 111, 127, 144, 156, 175, 192, 201	Digital Ground
VDD	PWR	10, 38, 52, 76, 105, 131, 154, 180	Digital Power

[1]Pins definition in parentheses are for linear addressing



Lead positional tolerance: 0.08mm for maximum lead width (0.3mm)

Figure 10. TVGA9200CXr Packaging - PFP 208 Pins (dimensions in mm)

March 1993 Rev. 1