RCC615

125 Mbaud Twisted Pair Transceiver (TPT)

Preliminary Information

Features

- Compliant with FDDI TP-PMD standards
- Controlled symmetric transmit output rise/fall time
- Tristatable transmit output
- Adjustable transmit amplitude for longer cables
- DC Restoration (Baseline wander compensation)
- No receive input attenuation required
- Adaptive line equalization
- Compatible with existing FDDI/Fast Ethernet Physical layer (PHY) chips
- 28 pin PLCC
- 525mW power dissipation

Applications

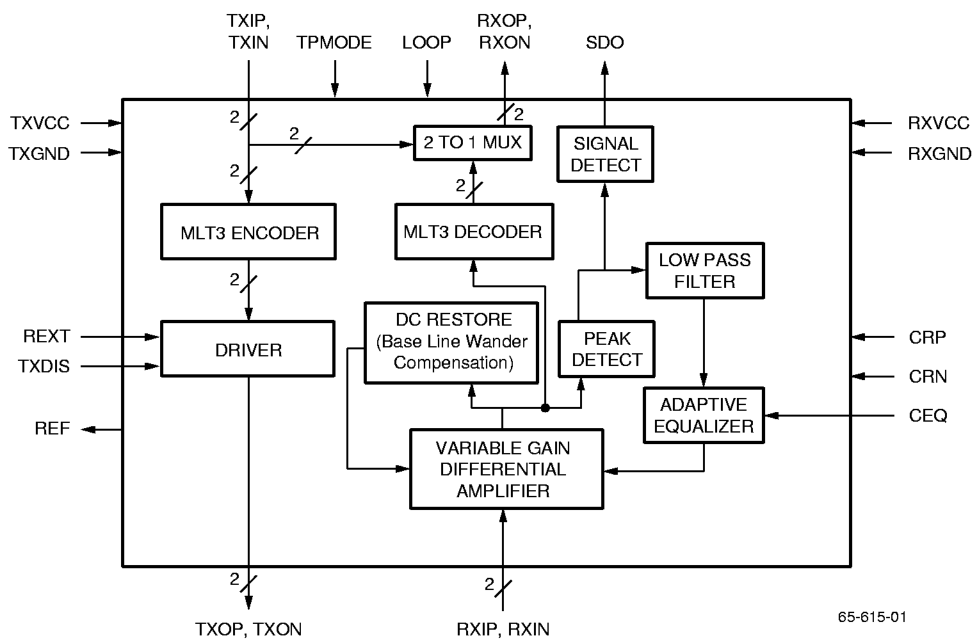
- FDDI
- 100 Mbps Fast Ethernet
- Bus Extenders
- Serial Video Communication
- Fast Ethernet/FDDI test equipment

Description

The RCC615 is a monolithic 125 Megabaud twisted pair transceiver (TPT) designed for IEEE 802.3 Fast Ethernet & American National Standard's (ANSI's) Fiber Distributed Data Interface (FDDI) applications. It implements the Physical Media Dependent Layer requirements of the FDDI (TP_PMD) standard. It can be used in a PHY layer solution for FDDI or 100base-TX Fast ethernet.

The RCC615 Integrates MLT3 encoding, driving, receiving, adaptive equalization, base line wander compensation (DC restoration) and MLT3 decoding. It operates with a single +5V supply.

Block Diagram



Rev. 0.9.6

Functional Description

Transmitter Section

The RCC615 transmitter section includes the MLT3 Encoder and Twisted pair driver. The transmittter drives either unshielded or shielded twisted pair cables to implement FDDI TP/PMD standard.

The differential PECL data from TXIP, TXIN goes through a MLT3 Encoder. The MLT3 encoder is enabled when the TPMODE pin is LOW. The data is encoded per the following rules: The encoded output takes on one of three possible levels: High, Middle, or Low. Whenever the input signal changes state, the output will also change state. If the output is in the middle state, the state to which it will change to is dependent on the previous state. If the previous state was high(low), then the output will change to a low(high) state from the middle state. If the output is at either a high or a low state, then the next transition will cause the output to change to the middle state. The encoder conforms to the diagram shown in Figure 1.

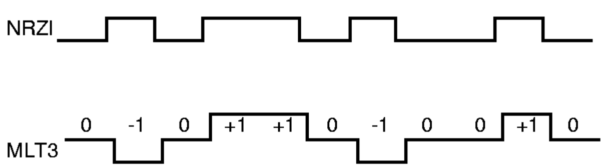


Figure 1. MLT3-NRZI Conversion Diagram

When TPMODE pin is high, the MLT3 encoder is bypassed and the data directly goes to the current source driver. The driver output current is controlled by external resistor between REXT and REF pins.

The voltage at the output is a function of the load termination across the differential output. If R is the effective load termination and I is the current source, the peak to peak output voltage V = IR. I = 40/REXT(in kΩ) mA, where REXT is the resistor connected between the REXT and REF pins. The TP driver provides a differential 2 V peak to peak swing voltage output across TXOP, TXON through a 100Ω termination in parallel with two 50Ω pullup resistor, when REXT = 1KΩ.

TXOP,TXON are connected externally to a coupling transformer and then to the twisted pair cable medium. The driver can be tristated by means of a pin TXDIS. When TXDIS is HIGH, the output presents a high impedance. In 2-level mode (TPMODE = HIGH), the output amplitude is half that of 3-level mode.

The transition time of the output is closely matched and controlled to reduce radiated emissions and to comply with FCC class B regulations.

Receiver Section

The signal from the transformer drives RXIP and RXIN and goes through a differential amplifier stage and then to a peak detect circuitry. The output of the peak detector goes to the signal detect comparator and to a low pass filter to remove the AC components. The low pass filter output then goes to an adaptive equalizer.

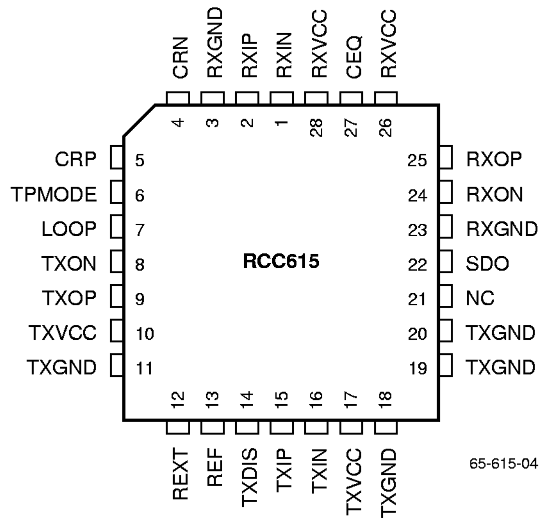
The equalizer output provides an adaptive gain control for the variable gain differential amplifier to compensate for the cable distortion. The gain depends on the measured peak value of the input. The equalizer filter characteristics can be adjusted by means of an external capacitor connected between CEQ and ground (1000pF is suggested).

The variable gain differential amplifier output also goes through the DC restoration and decode circuitry. The purpose of the DC restoration (baseline wander compensation) circuit is to provide DC restoration to the data stream on the occurrence of a long run-length. During those instances, the average DC tends to drift away from the decode circuit's threshold. The DC restoration circuit integrates the decoder output to provide a DC offset to the envelope to center it around the threshold of the decoder circuit. The MLT3 decoder also provides 3-level to 2-level conversion. The decoder conforms to the diagram shown in Figure 1.

The decoder output goes through a 2 to 1 multiplexer. The other input to the multiplexer comes from the transmitter inputs TXIP, TXIN. If LOOP signal is HIGH, the transmit input is looped back to RXOP, RXON through the multiplexer. Under this condition, the transmitter output (TXOP, TXON) presents a logic LOW voltage. If LOOP is LOW, the decoder output is enabled and routes the signal to RXOP, RXON.

The receive section also includes a signal detect logic. The signal detect logic filters the input signal and if the signal exceeds a specified level, the SDO output will go HIGH.

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Type	Description
CEQ	27	Analog	**Equalizer Capacitor.** A capacitor is connected between CEQ and RXGND to adjust the gain of the adaptive equalizer. 1000 pF is recommended.
CRP, CRN	5, 4	Analog	**DC Restoration Capacitor Positive, DC Restoration Capacitor Negative.** A capacitor is connected at each of CRP, and CRN to RXGND to provide DC restoration. 1000 pF is recommended.
LOOP	7	TTL I/P	**Loop.** If LOOP is HIGH, it loops the transmit input data, TXIP,TXIN to the receiver output, RXOP,RXON. If LOOP is LOW, the normal operation occurs.
REF	13	Analog O/P	**Reference.** Provides the reference voltage to set the transmit output amplitude when an external resistor is connected between REF and REXT. It is nominally 2.5 Volts.
REXT	12	Analog	**External Resistor.** It is connected between REXT and REF to adjust the amplitudes of TXOP, TXON. For MLT3 signals, the peak-to-peak differential voltage of 2V is generated across TXOP, TXON when the effective differential load is 50Ω and REXT = 1KΩ.
RXGND	3, 23	Power	**Receive Ground.** Chip ground for receive circuity. RXGND should be connected to the printed circuit board's ground plane through a ferrite bead of value 0.2μH to 1μH.
RXIP, RXIN	2, 1	I/P	**Receive Input Positive, Receive Input Negative.** (MLT3 inputs if TPMODE = 0, NRZI inputs if TPMODE = 1). Receive differential data inputs.
RXOP, RXON	25, 24	PECL DIFF O/P	**Receive Output Positive, Receive Output Negative.** Differential NRZI receive data to the PHY chip. Do not tie external termination below 510Ω to RXGND. For 50Ω applications, 50Ω from the outputs to 3V may be connected.
RXVCC	26, 28	Power	**Receive Positive Supply.** The nominal value is 5V ±5%. RXVCC should be bypassed to RXGND with a 0.1μF chip capacitor placed as close to the pin as possible.

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Pin Descriptions (continued)

Pin Name	Pin Number	Pin Type	Description
SDO	22	PECL O/P	**Signal Detect.** When SDO is HIGH, it indicates that the receive input is active. Do not tie any external termination resistor to SDO.
TXGND	11, 18, 19, 20	Power	**Transmit Ground.** Chip ground for transmit circuity. TXGND should be connected to the printed circuit board's ground plane through a ferrite bead of value 0.2µH to 1 µH.
TPMODE	6	TTL I/P	**Twisted Pair Encode Mode.** When TPMODE is LOW, the transmit output is MLT3 encoded with three levels. When TPMODE is HIGH, the transmit output is NRZI with two levels.
TXDIS	14	TTL I/P	**Transmit Disable.** If TXDIS is HIGH, the transmitter disables the TXOP, TXON output and presents a high impedance. If TXDIS is LOW, the transmitter enables normal data transmission through RCC615.
TXIP,TXIN	15,16	PECL DIFF I/P	**Transmit Input Positive, Transmit Input Negative.** Differential NRZI Transmit data from the PHY chip.
TXOP,TXON	9,8	O/P	**Transmit Output Positive, Transmit Output Negative.** (MLT3 outputs if TPMODE = 0, NRZI outputs if TPMODE = 1). Transmit differential current driver data outputs.
TXVCC	10,17	Power	**Transmit Positive Supply.** The nominal value is 5V ±5%. TXVCC should be bypassed to TXGND with a 0.1µF chip capacitor placed as close to the pin as possible.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Units
Positive power supply	0	6	V
Voltage applied to any PECL/MLT3 outputs	-0.5	V_{CC}	V
Voltage applied to any TTL inputs	-0.5	V_{CC}	V
Voltage applied to any PECL inputs	-0.5	V_{CC}	V
Current from any PECL/MLT3 outputs	-50	+50	mA
Operating Temperature	0	70	°C
Storage Temperature	-65	150	°C
Junction Temperature	-55	150	°C
Lead Soldering (10 seconds)		300	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Ta	Ambient Operating Temperature	0		70	°C
V_{CC}	Positive Supply Voltage (TXVCC and RXVCC)	4.75	5.00	5.25	V
R_{utp}	Unshielded Twisted Pair Differential Load Resistance	99.8	100	100.2	Ω
R_{stp}	Shielded Twisted Pair Differential Load Resistance	149.7	150	150.3	Ω

DC Electrical Characteristics

RXVCC, TXVCC = 5V ±5%, RXGND, TXGND = 0V, unless otherwise indicated

Parameter		Conditions	Min.	Typ.	Max.	Units
Transmitter Section						
Vihc	TTL input Voltage HIGH		2.0		V_{CC}	V
Vilc	TTL input Voltage LOW		0		0.8	V
Iinc	TTL Input Current				25	µA
C	Input Capacitance			3.0		pF
Vcm	Com. Mode Range (TXIP, TXIN)		3.3	3.7	4.1	V
Vdiff	Diff. Input Voltage (TXIP, TXIN)		0.4		2.0	Vpp
Iip	PECL Input Current		-20	0	20	µA
Vomh	MLT3 Positive Peak Voltage	Diff load R = 100Ω ±0.2% and 50Ω on both TXOP, TXON to VCC		4.2		V
Voml	MLT3 Negative Peak Voltage			3.2		V
Vohn	NRZI Output Voltage HIGH			4.2		V
Voln	NRZI Output Voltage LOW			3.2		V
Receiver Section						
Vdif	RXIP, RXIN Diff Input Voltage		0.4		2	V
Vcm	RXIP, RXIN Com. Mode Range			2.6		V
Vocm	RXOP, RXON Com. Mode Range	510Ω to GND on RXOP, RXON		V_{CC}–1.5		V
Vodiff	RXOP, RXON Diff Output Voltage			1.5		Vpp
Vohp	SDO Output HIGH		V_{CC}–1.1		V_{CC}–0.7	V
Volp	SDO Output LOW		V_{CC}–2		V_{CC}–1.4	V
Vonth	SDO Turnon threshold			350		mV
Vofth	SDO Turnoff threshold			260		mV
Power Section						
ICC	Power Supply Current			110		mA
PD	Power Dissipation			525		mW

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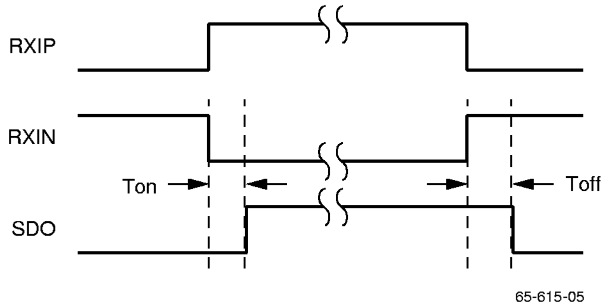
AC Electrical Characteristics[1]

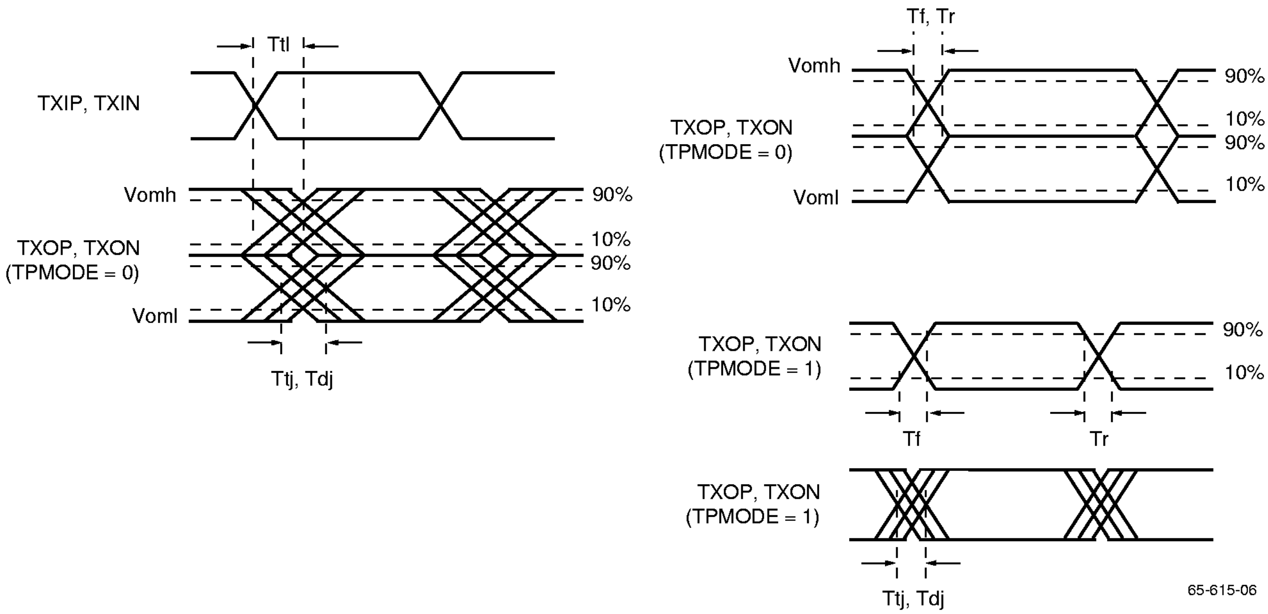
V_{CC} = 5V ±5%, GND = 0V, unless otherwise indicated



Parameter		Conditions	Min.	Typ.	Max.	Units
Receiver Section						
Ton	SDO turnon delay @ CEQ = 1000pF	Diff I/P > 1V		1	1000	µs
Toff	SDO turnoff delay @ CEQ = 1000pF	Diff I/P <0.2V		200	350	µs

Note:
1. Test conditions (unless otherwise indicated:) PECL Input rise and fall times ≤ 2ns, R_L = 100Ω. TTL Input rise and fall times ≤ 15ns. Transition density ≥ 0.1.

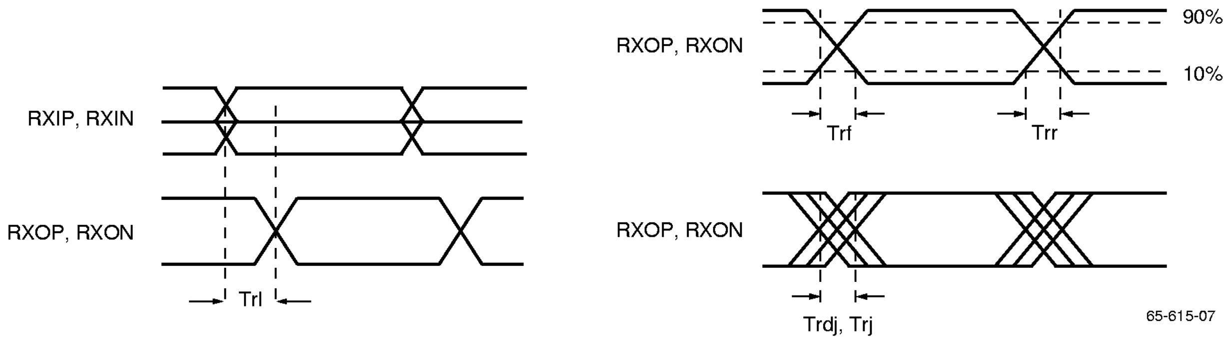
Timing Diagrams



Transmitter Timing

Parameter		Conditions	Min.	Typ.	Max.	Units
Tr	TXOP, TXON rise time 10% to 90%	100Ω termination		2.7		ns
Tf	TXOP, TXON fall time			2.7		ns
Tdj	TXOP, TXON duty cycle distortion (peak-to-peak)			0.3		ns
Ttj	Random jitter			300		ps
Ttl	Transmit latency			5.0		ns

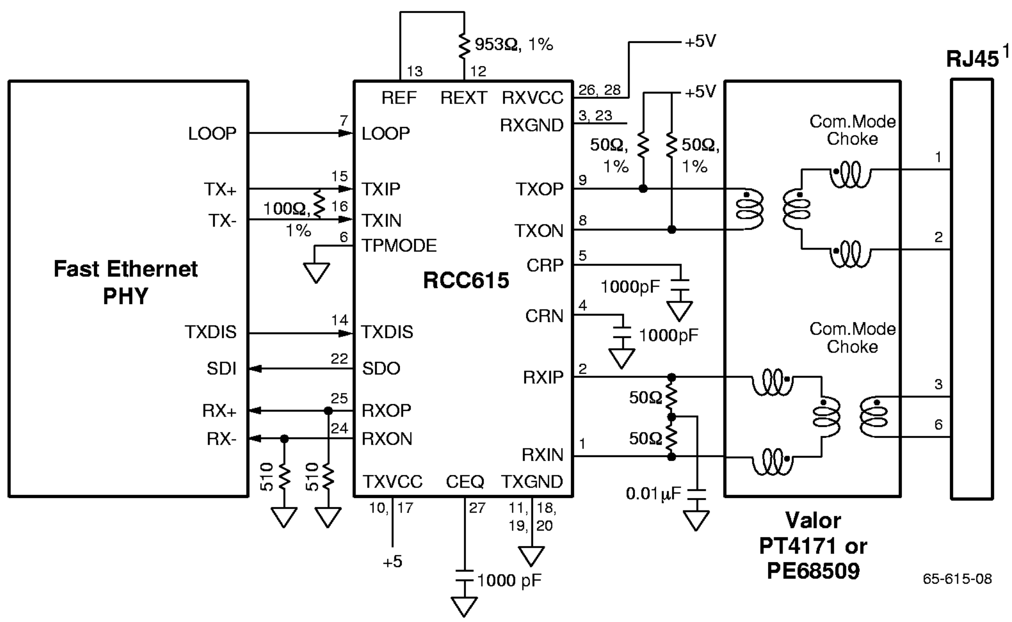
Timing Diagrams (continued)



Receiver Timing

Parameter		Conditions	Min.	Typ.	Max.	Units
Trr	RXOP, RXON rise time	10% to 90%		1.5		ns
Tfr	RXOP, RXON fall time	90% to 10%		1,5		ns
Trdj	RXOP, RXON duty cycle distortion (peak-to-peak) @ 100m calbe (UTP)			0.5		ns
Trj	RXOP,RXON peak to peak jitter			400		ps
Trl	Receive latency	@ 100m UTP		5		ns

Applications Discussion



Notes:

1. For FDDI applications, the receive pins are 7 and 8 instead of 3 and 6 on the RJ45 connector.
2. TXVCC and RXVCC should be connected individually to circuit board's +5 volts through ferrite bead of value 0.2μH to 1μH (e.g. FAIR-RITE BEAD #274-3019-446).
3. TXGND and RXGND should be connected individually to circuit board's ground through ferrite bead of value 0.2μH to 1μH (e.g. FAIR-RITE BEAD #276-3019-446). The current handling capability should be 100mA.
4. For 50Ω applications, RXOP, RXON may be connected with 50Ω to 3V.

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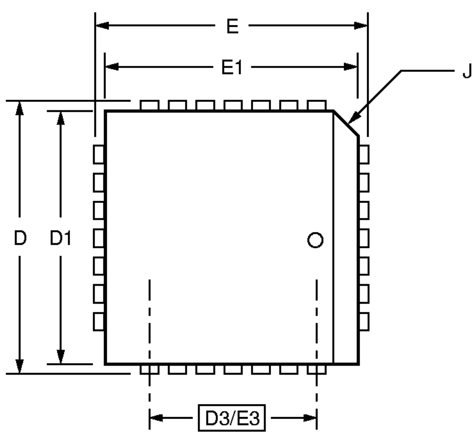
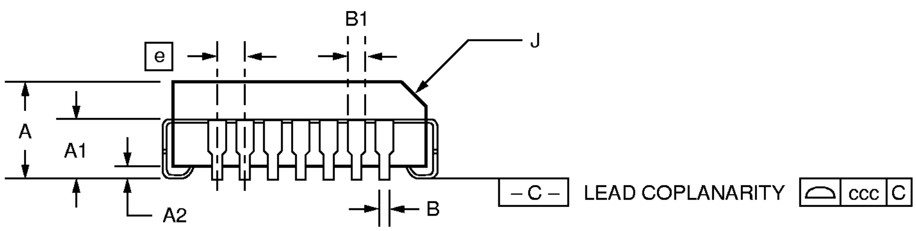
Mechanical Dimensions – 28 Lead PLCC (QA) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.04	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	8
ND/NE	7		7		
N	28		28		
ccc		.004		0.10	

Notes:

1. Cavity mismatch = .004 (0.10mm)
2. Cavity frame offset = .002 (0.05mm) excluding leadframe tolerances.
3. Mold protrusions: Parting Line = .006 (0.15mm), Top or Bottom = .001 (0.025mm)
4. Variation in lead position = .005 (0.13mm)
5. Shoulder instrusions & protrusions: Intrusions = .002 (0.05mm), Protrusions = .003 (0.08mm)
6. Package warpage, WARP FACTOR = 2.5 = $\frac{\text{WARP (mils)}}{\text{Package Length (inches)}}$
7. Ejector pin depth = .010 (0.25mm) maximum.
8. Corner and edge chamfer = 45°C.





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Ordering Information

Product Number	Package
RCC615V	28 PLCC

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5/20/98 0.0m 001
Stock#DS50000615