

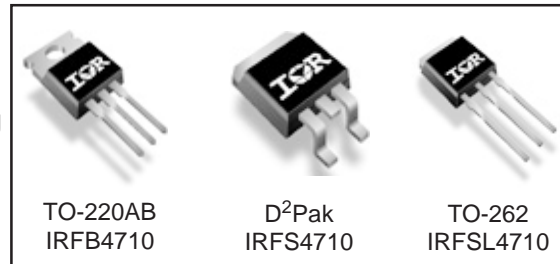
**Applications**

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies

$V_{DSS}$	$R_{DS(on) \max}$	$I_D$
100V	0.014Ω	75A

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	75	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	53	
$I_{DM}$	Pulsed Drain Current ①	300	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ②	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	200	
	Linear Derating Factor	1.4	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	8.2	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.74	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑤	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

Notes ① through ⑦ are on page 11

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# IRFB/IRFS/IRFL4710

International  
**IR** Rectifier

## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	0.011	0.014	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 45A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.5	—	5.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 95V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

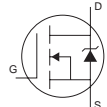
## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

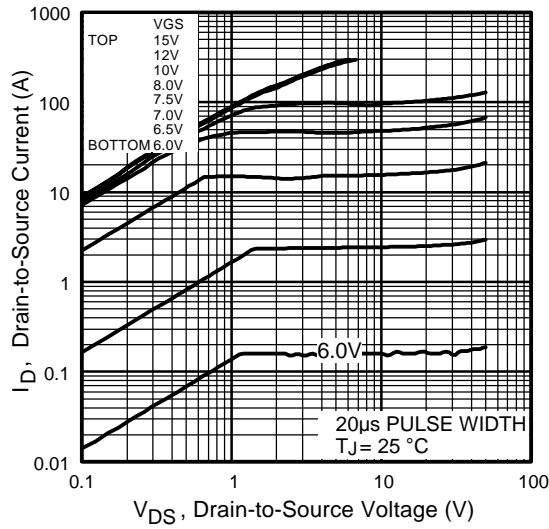
	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	35	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 45A
Q <sub>g</sub>	Total Gate Charge	—	110	170	nC	I <sub>D</sub> = 45A
Q <sub>gs</sub>	Gate-to-Source Charge	—	43	—		V <sub>DS</sub> = 50V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	40	—		V <sub>GS</sub> = 10V,
t <sub>d(on)</sub>	Turn-On Delay Time	—	35	—	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	130	—		I <sub>D</sub> = 45A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	41	—		R <sub>G</sub> = 4.5Ω
t <sub>f</sub>	Fall Time	—	38	—		V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	—	6160	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	440	—		V <sub>DS</sub> = 25V
C <sub>riss</sub>	Reverse Transfer Capacitance	—	250	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1580	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	280	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 80V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	430	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V ⑤

## Avalanche Characteristics

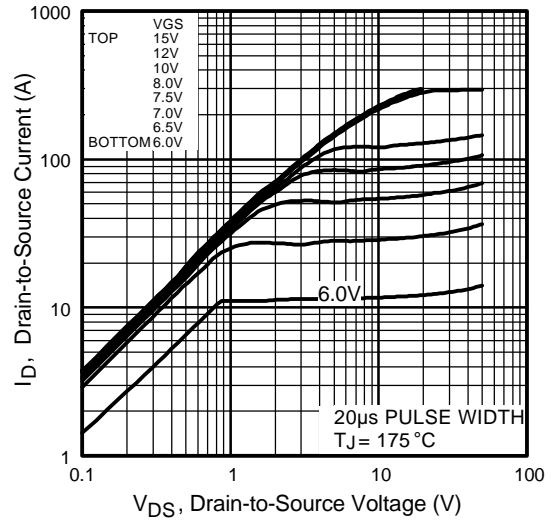
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	190	mJ
I <sub>AR</sub>	Avalanche Current①	—	45	A
E <sub>AR</sub>	Repetitive Avalanche Energy①	—	20	mJ

## Diode Characteristics

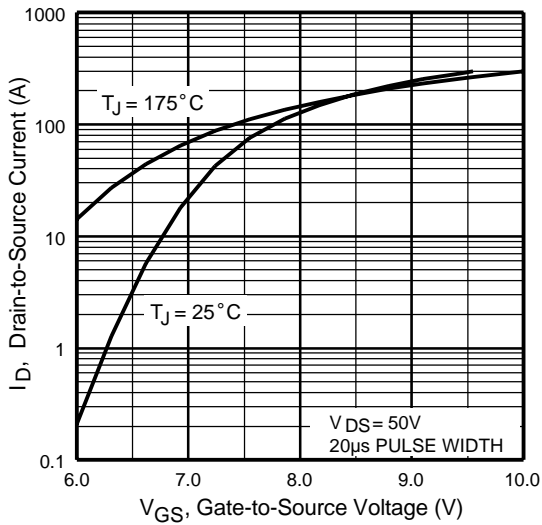
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	300		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 45A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	74	110	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 45A
Q <sub>rr</sub>	Reverse Recovery Charge	—	180	260	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				



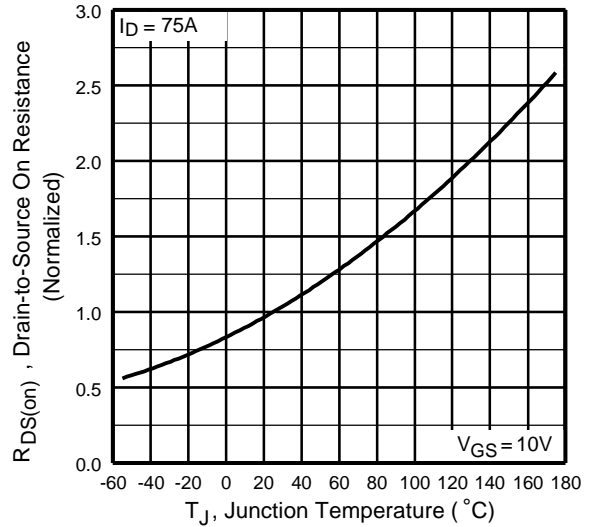
**Fig 1.** Typical Output Characteristics



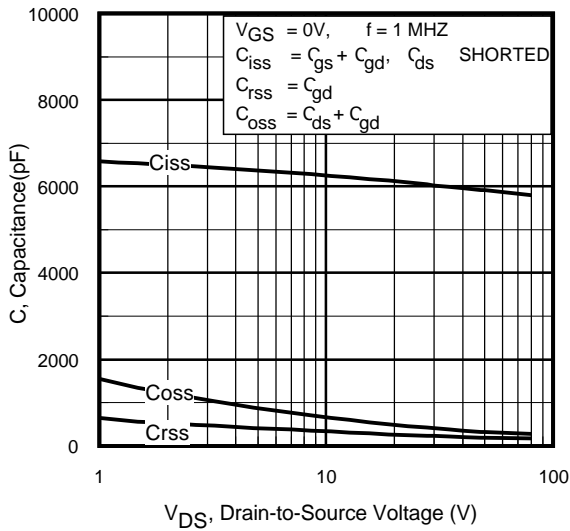
**Fig 2.** Typical Output Characteristics



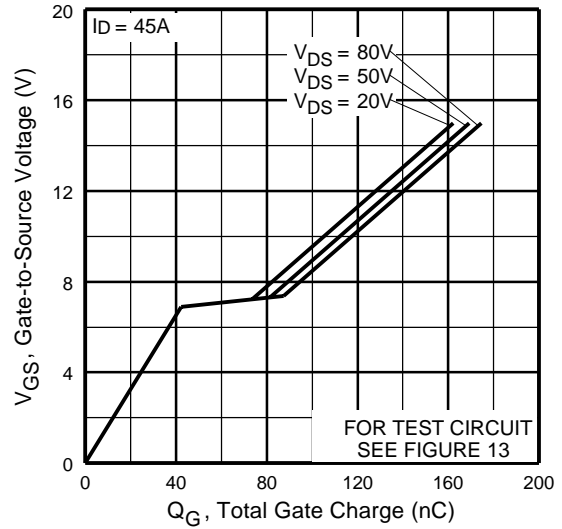
**Fig 3.** Typical Transfer Characteristics



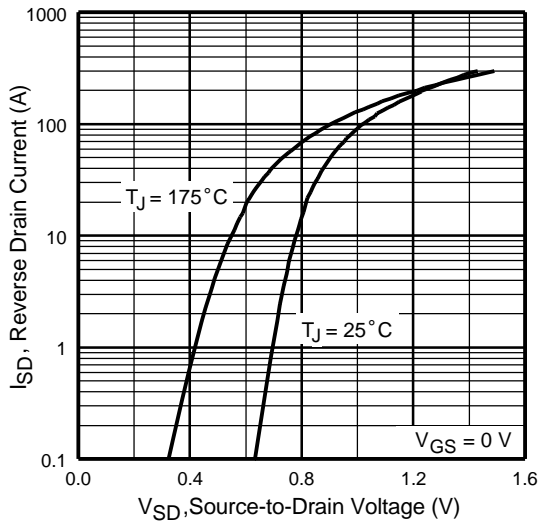
**Fig 4.** Normalized On-Resistance Vs. Temperature



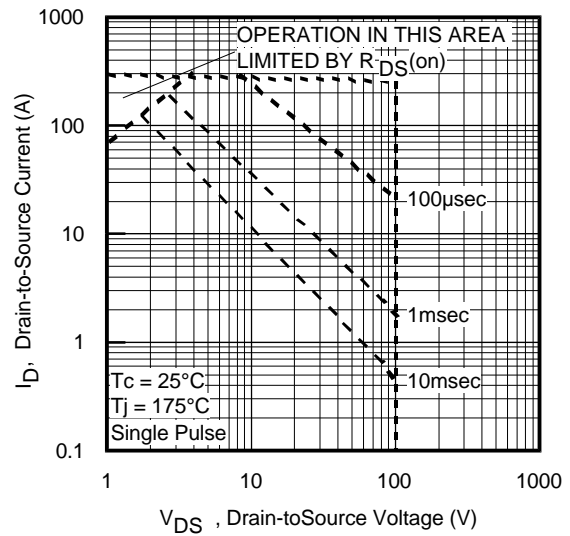
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

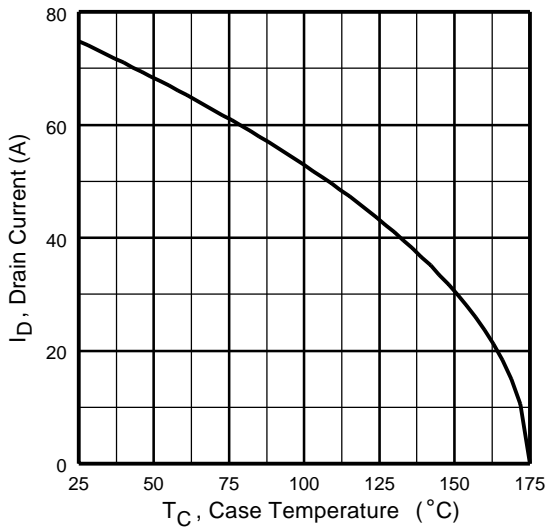


Fig 9. Maximum Drain Current Vs. Case Temperature

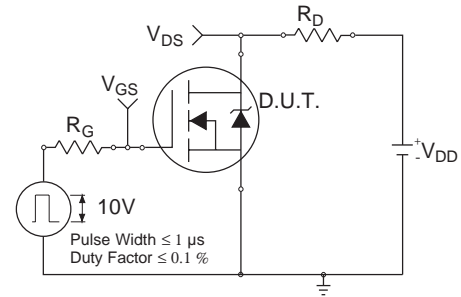


Fig 10a. Switching Time Test Circuit

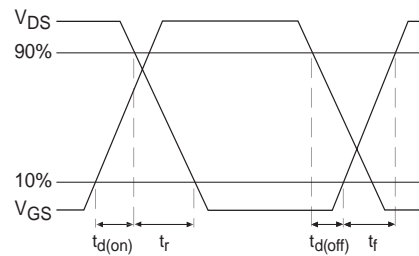


Fig 10b. Switching Time Waveforms

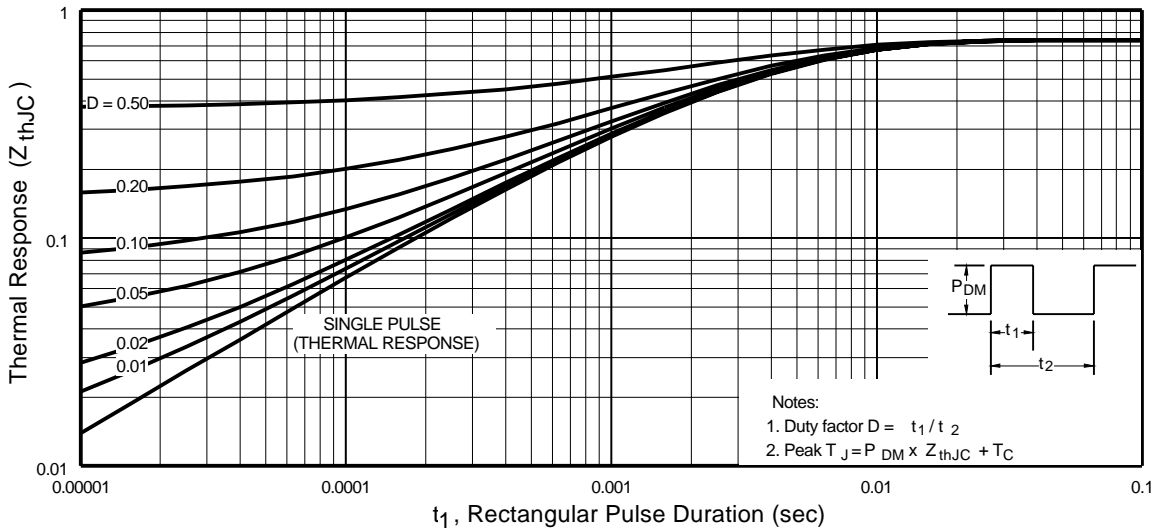
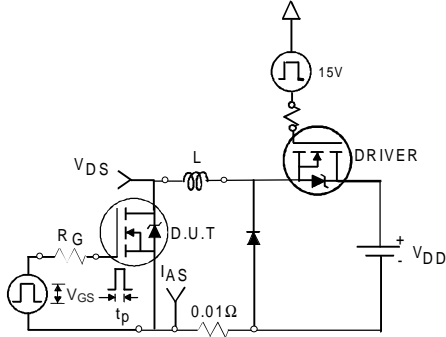
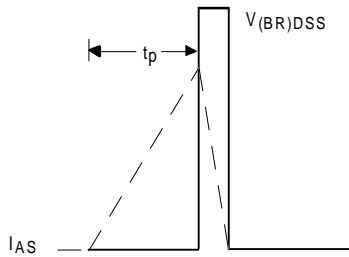


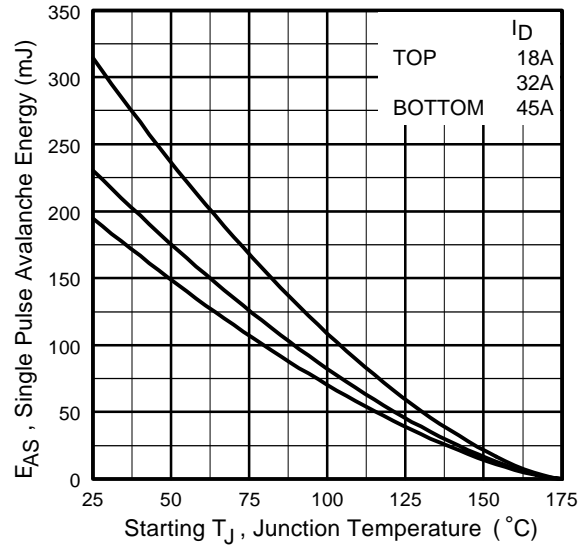
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



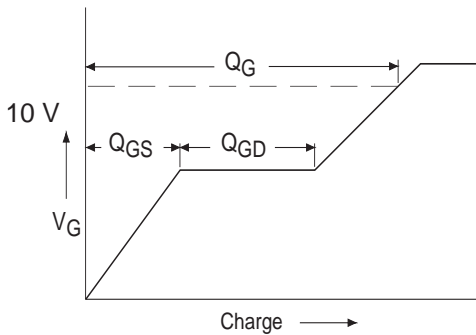
**Fig 12a.** Unclamped Inductive Test Circuit



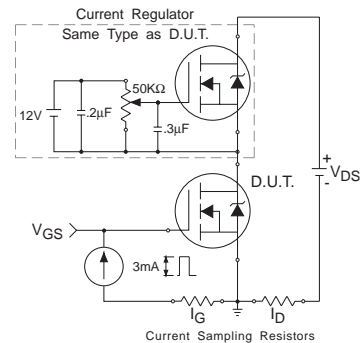
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRFB/IRFS/IRFL4710



## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



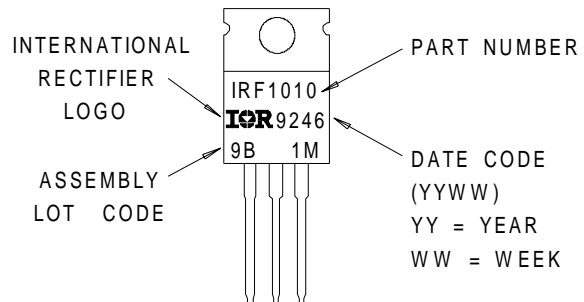
**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

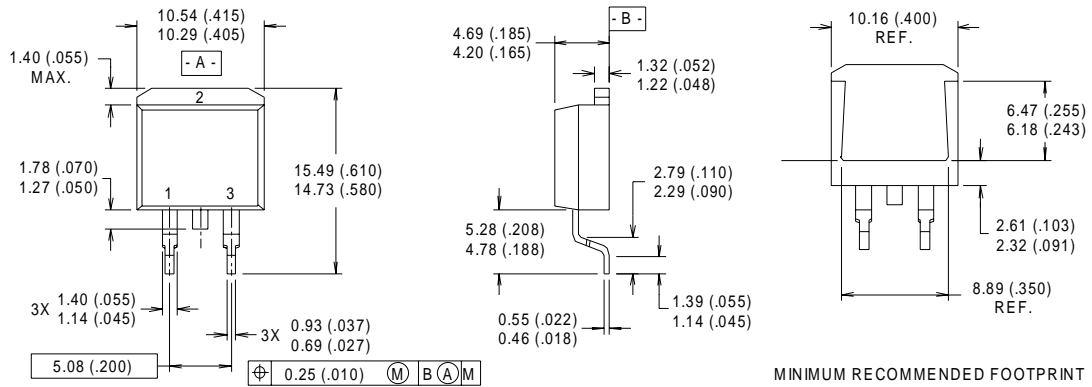
## TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010  
WITH ASSEMBLY  
LOT CODE 9B1M





## D<sup>2</sup>Pak Package Outline



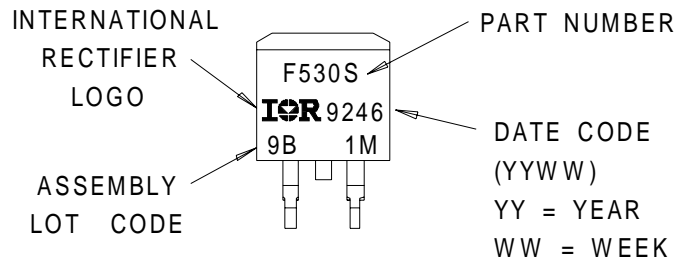
**NOTES:**

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

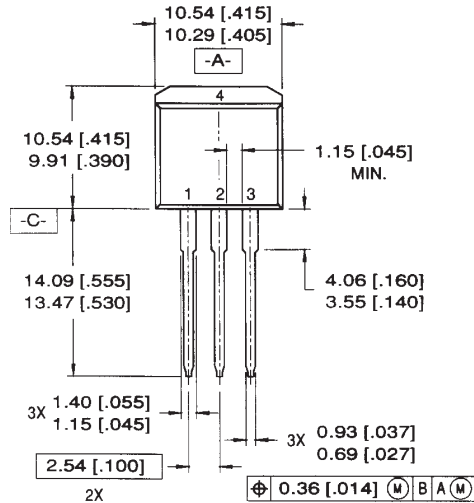
## D<sup>2</sup>Pak Part Marking Information



# IRFB/IRFS/IRFL4710

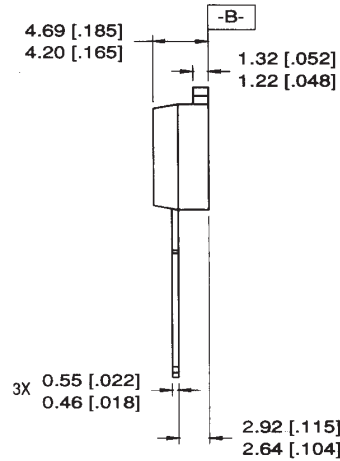


## TO-262 Package Outline



### LEAD ASSIGNMENTS

- 1 = GATE      3 = SOURCE
- 2 = DRAIN     4 = DRAIN

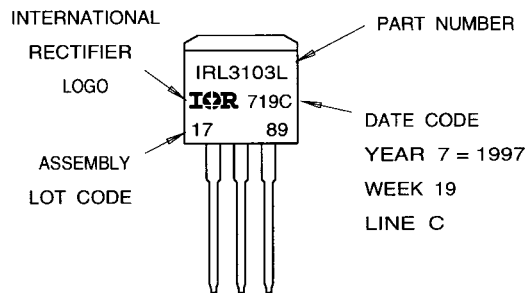


### NOTES:

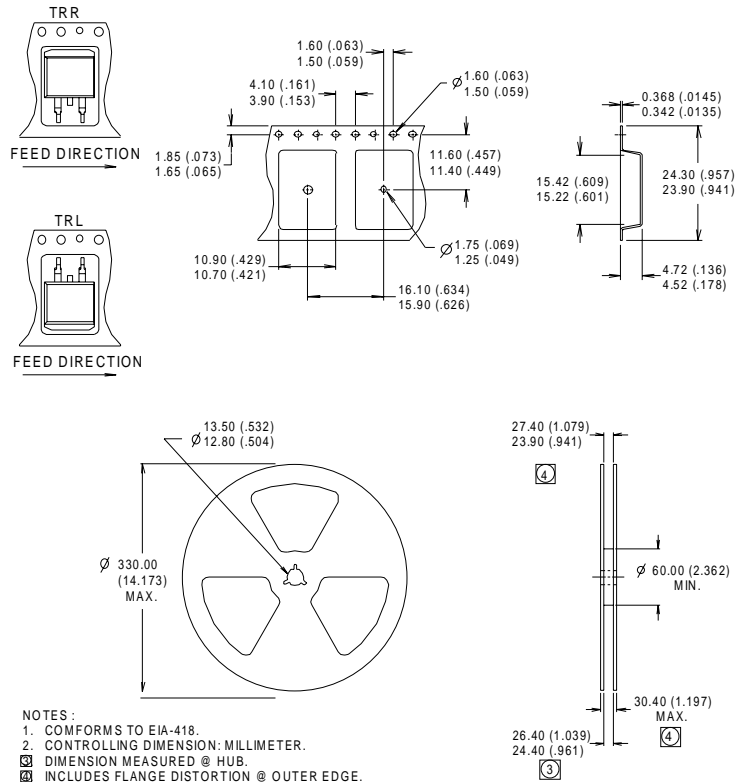
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



D<sup>2</sup>Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 190\mu\text{H}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 45\text{A}$ ,  $V_{GS} = 10\text{V}$
- ③  $I_{SD} \leq 45\text{A}$ ,  $di/dt \leq 420\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ).  
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.