

Intel® 81348 I/O Processor

Datasheet

Product Features

- Two Integrated Intel XScale® processors
 - 667 MHz, 800 MHz and 1.2 GHz
 - ARM* V5TE Compliant
 - Instruction/Data Cache: 32 KByte, 4-way Set Associative, NRU Replacement Algorithm, Lockable
 - Unified Level 2 Cache: 512 KByte Set Associative, NRU Replacement Algorithm
 - 128-Entry Branch Target Buffer
 - 8-Entry Write Buffer
 - 8-Entry Fill and Pend Buffer
- Internal Bus 128-bit wide at 333 MHz and 400 MHz depending on processor speed
- Can support either PCI-X or PCI Express* as an endpoint
- Can support both PCI-X Central Resource and PCI Express* Root Complex
- Support for PCI Express* Lane Widths of x1, x2, x4, x8
- Eight Serial-Attached SCSI links — also capable of supporting direct-attached SATA targets
- Integrated SRAM Memory Controller (1 MB); dedicated to the SAS transport
- Address Translation Unit
 - 2 KB or 4 KB Outbound Read Queue
 - 4 KB Outbound Write Queue
 - 4 KB Inbound Read and Write Queue
- Application DMA Controller
 - Three Independent Channels Connected to the MCU and the South Internal Bus
 - 4 KByte Data Transfer Queue
 - CRC 32C Calculation
 - Performs Optional XOR on Read Data
- Multi-ported Memory Controller
 - Intel XScale® processor inputs and north internal bus, south internal bus and ADMA input ports
 - PC3200 and PC4300 Double Data Rate (DDR2 400, DDR2 533)
 - Up to 4 GB of 64-bit DDR2 400, DDR2 533
 - Optional Single-bit Error Correction, Multi-bit Detection ECC Support
 - Supports Registered and Unbuffered DDR2 Memory
 - 36-bit Addressable
 - 32-bit Memory Support
- Two Programmable 32-bit Timers and Watchdog Timer
- Sixteen General Purpose I/O Pins
- Eight ACTIVITY/STATUS pairs — one per SAS port
- Three I²C Bus Interface Units
- Two UART (16550) Units
 - 64 Byte Receive and Transmit FIFOs
 - 4 pin Master/Slave Capable
- Peripheral Bus Interface
 - 8-, 16-bit Data Bus with Two Chip Selects
 - 25 Demultiplexed Address Lines
- Interrupt Controller Unit
 - Four Priority Levels
 - Interrupt Pending Register
 - Vector Generation
 - 16 External Interrupt Pins with High Priority Interrupt (HPI#)
- 1357-ball, Flip Chip Ball Grid Array (FCBGA), 37.5 mm x 37.5 mm and 1.0 mm ball pitch



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Revision History

| Date | Revision | Description |
|---------------|----------|---|
| December 2007 | 003 | Revised for 4 GB memory support. |
| April 2007 | 002 | Updated Legal page 2. Edited text in Section 2.2.2. Revise PCIXCAP description in Table 5. Updated Table 19 for Cgp, Cpcix, Cddr2 and Lpin values. Revised Table 18 for Tcase (Tc) maximum value to 100C. Revised Figure 28. |
| October 2006 | 001 | Initial release. |



1.0 Introduction

1.1 About This Document

This document is a reference guide for the external architecture of the Intel® 81348 I/O Processor (also known as the 81348).

1.1.1 Terminology

To aid the discussion of the 81348 architecture, the following terminology is used:

| | |
|-----------------|--|
| Downstream | At or toward a PCI bus with a higher number (after configuration) |
| Word | 16 bits of data |
| Dword | 32 bits of data |
| Qword | 64 bits of data |
| Host processor | Processor located upstream from the 81348 |
| Local processor | Intel XScale® processor within the 81348 |
| Local bus | 81348 internal bus |
| Local memory | Memory subsystem on the Intel XScale® microarchitecture, DDR2 SDRAM or Peripheral Bus Interface busses |
| Upstream | At or toward a PCI bus with a lower number (after configuration) |

1.1.2 Other Relevant Documents

1. *Intel XScale® Microarchitecture Developer's Manual* (Order Number 273473)—Intel Corporation
2. *PCI Local Bus Specification*, Revision 2.3—PCI Special Interest Group
3. *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0a*—PCI Special Interest Group
4. *PCI Hot-Plug Specification*, Revision 1.0—PCI Special Interest Group
5. *PCI Bus Power Management Interface Specification*, Revision 1.1—PCI Special Interest Group
6. *PCI Express Specification*, Revision 1.0a—PCI Special Interest Group





2.0 Features

2.1 About the Intel® 81348 I/O Processor

The 81348 is a single- or dual-function PCI device that integrates two Intel XScale® processors with intelligent peripherals including a PCI bus interface and eight Serial-Attached SCSI (SAS) engines. The 81348 also supports two internal busses: North XSI bus and South XSI bus. With the two internal busses, transactions can take place simultaneously on each bus. The north XSI bus provides the two Intel XScale® processors with low-latency access to either the DDR2 SDRAM Memory Controller, the on-chip SRAM Memory Controller, or the SAS Engines control registers. Peripherals that generate large burst transactions are located on the south XSI bus, thus allowing the two Intel XScale® processors exclusive access to the north XSI bus.

The 81348 consolidates the following features into a single system:

- Two Intel XScale® processors running at speeds up to 1.2 GHz
- Eight Serial Protocol Links capable of Serial-Attached SCSI (SAS) or Serial ATA (SATA) operation
- PCI-Local Memory Bus Address Translation Unit, function 0 programming interface
- Messaging Unit, function 0 programming interface
- Application Direct Memory Access (DMA) Controller (including offload for up to a 16-source XOR operation)
- Transport DMA Controllers
- Peripheral Bus Interface Unit
- Integrated DDR2 Memory Controller
- Integrated SRAM Memory Controller
- Two programmable timers per Intel XScale® processor
- Watchdog timer per Intel XScale® processor
- Three I²C Bus Interface Units
- Two Serial Port Units
- Sixteen General-Purpose Input/Output (GPIO) ports
- ACTIVITY/STATUS pin pairs—one per SAS Engine
- Internal North Bus-South Bus Bridge

It is an integrated processor that addresses the needs of intelligent I/O storage applications and helps reduce intelligent I/O system costs.

The 81348 can support PCI-X 1.0b and/or PCI Express* as a reset option. The PCI bus is an industry standard, high-performance, low-latency system bus. The 81348 PCI bus is capable of 133 MHz operation in PCI-X 1.0b mode (as defined by the *PCI-X Addendum to the Local Bus Specification*, Revision 1.0b). Also, the processor supports a 66 MHz conventional PCI mode (as defined by the *PCI Local Bus Specification*, Revision 2.3). The addition of the Intel XScale® processors brings intelligence to the PCI bus application bridge. 81348 supports an x8 PCI Express* interface.

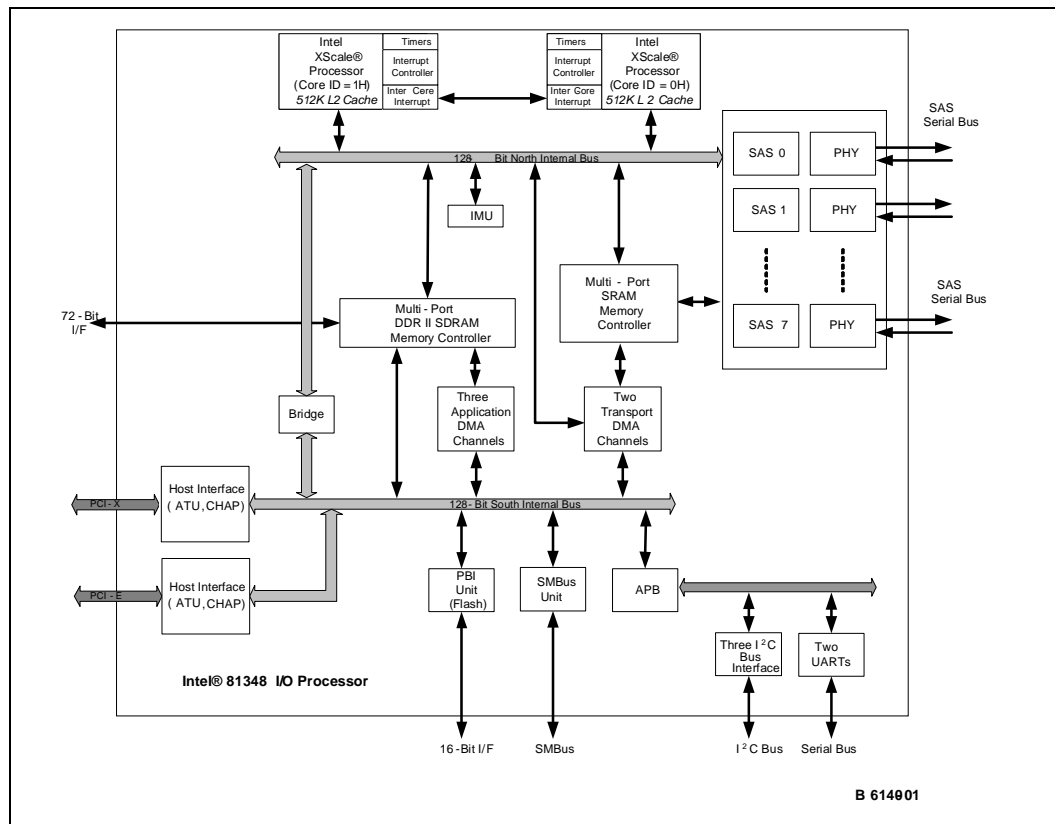
The 81348 can be set up as a single- or dual-function PCI device at reset using external straps. Refer to the "Clocking and Reset" section in the Intel® 81348 I/O Processor *Developer's Manual* for a description of the reset options. When the 81348 is configured as a single-function device, the host programming interface is presented as the Address Translation Unit (ATU) and the Messaging Unit (MU). The MU provides the messaging interface between the host processor and the 81348.

When the 81348 is configured as a dual-function device, PCI function 0 host programming interface is presented as the ATU with the MU. The reset strapping options determine how the controller's SAS/SATA ports are assigned to function 1 and function 0.

Both the address and data busses on the 81348 south XSI bus are byte-wise parity protected. All the peripherals connected to the south XSI bus can check and generate parity.

Figure 1 is a block diagram of the 81348.

Figure 1. Intel® 81348 I/O Processor Functional Block Diagram





2.2 Intel® 81348 I/O Processor Features

The 81348 combines two Intel XScale® processors with powerful new features to create an intelligent I/O storage processor. This single- or dual-function PCI device is fully compliant with the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0 and *PCI Express Specification*, Revision 1.0. Features specific to 81348 include the following:

- Address Translation Unit
- Messaging Unit
- Flash Interface Unit
- Chip Architecture Performance Unit
- I²C Bus Interface Units
- Multi-Port SRAM Memory Controller
- Application DMA Controllers
- XSI System Controller (north and south)
- DDR2 SDRAM Memory Controller
- Transport DMA Controllers
- UART Units
- Address and Data Bus Parity Protection
- Inter-Processor Communication
- Timers
- Watchdog Timers
- Eight SAS Link Engines with integrated PHYs

The 81348 is based upon two Intel XScale® processors. The processor operates at a maximum frequency of 1.2 GHz. The instruction cache is 32 Kbytes in size and is 4-way set associative. Also, the processor includes a data cache that is 32 Kbytes and is 4-way set associative. The Intel XScale® processors also support a unified 512-Kbyte Level 2 (L2) cache that is 8-way set associative.

The 81348 includes sixteen General Purpose I/O (GPIO) pins, and eight ACTIVITY/STATUS pin pairs which are used for SAS links for activity and status indicators. Each SAS link uses one ACTIVITY/STATUS pin pair.

Note: The subsections that follow provide a brief overview of each feature. Refer to the appropriate chapter in the *Intel® 81348 I/O Processor Developer's Manual* for full technical descriptions.

2.2.1 Host Interface

The 81348 can be set up as either a single- or dual-function PCI device, providing PCI-X or PCI Express* interface or both PCI-X and PCI Express* interfaces. The PCI interface is selected as a reset option. When set up as a single-function PCI device, the Address Translation Unit (ATU) and the Messaging Unit (MU) provide the programming interface between the host processor and the 81348. When set up as a dual-function device, the ATU and the MU provide the programming interface between the host processor and the 81348 for function 0, whereas the Third-Party Messaging Interface (TPMI) provides the programming interface between the host processor and the 81348 for function 1.

The PCI interface is selected as a reset option.



2.2.2 Internal Busses

The 81348 is built around two internal busses: north internal bus and south internal bus. The two busses use the same bus protocol. The north internal bus is 128 bits wide and operates at up to 400 MHz. The north bus connects the two Intel XScale® processors, which have direct access to the DDR2 SDRAM and SRAM. The Intel XScale® processors also have direct access to the SAS/SATAFibre Channel engine memory-mapped registers. The north XSI bus is designed to provide the two Intel XScale® processors with low-latency access.

The south internal bus is 128 bits wide and operates at up to 400 MHz. The south XSI bus provides the data paths for burst transactions generated by the DMAs. The south XSI bus internal address and data busses are parity-protected on a byte-wise basis. Agents on the south XSI bus can generate and check address and data parity. The point-to-point interfaces between the agents and the DDR2 and SRAM Memory Controllers are also parity-protected on a byte-wise basis.

Note: Internal busses run at 333MHz for 667MHz core speed. Internal busses run at 400MHz for 800MHz and 1.2GHz core speeds.

2.2.3 Application DMA Controllers

There are three Application DMA Controllers. The Application DMA Controller is dual-ported—with one of its ports connected to the south XSI bus and the other port to the DDR2 SDRAM Memory Controller. This Application DMA Controller allows low-latency, high-throughput data transfers between PCI bus agents and the DDR2 memory. The DMA controller also allows data transfer between DDR2 Memory. The DMA Controller supports chaining and unaligned data transfers. It is programmable through the Intel XScale® processor and the host processor.

In addition to simple data transfers, the ADMA performs XOR operations with up to 16 sources.

2.2.4 Address Translation Unit

The Address Translation Unit (ATU) allows PCI transactions direct access to the 81348 local memory. The ATU provides interface for the RAID Controller PCI function. The ATU supports transactions between PCI address space and the 81348 address space. Address translation is controlled through programmable registers accessible from both the PCI interface and the Intel XScale® processor. Dual access to registers allows flexibility in mapping the two address spaces. The ATU also supports the following extended capability configuration headers:

1. Power Management header, as defined by *PCI Bus Power Management Interface Specification*, Revision 1.1.
2. Message Signaled Interrupt capability structure, as specified in *PCI Local Bus Specification*, Revision 2.3.
3. PCI-X Capabilities List Item, as specified in the *PCI-X Addendum to the Local Bus Specification*, Revision 1.0b.



2.2.5 Messaging Unit

The Messaging Unit (MU) provides data transfer between the PCI system and the 81348. It uses interrupts to notify each system when new data arrives. The MU has four messaging mechanisms: Message Registers, Doorbell Registers, Circular Queues, and Index Registers. Each allows a host processor or external PCI device and the 81348 to communicate through message passing and interrupt generation. The MU, in conjunction with the ATU, exists as the PCI interface for PCI function 0 when function 0 is set up as a RAID controller.

2.2.6 DDR2 Memory Controller

The DDR2 Memory Controller allows direct control of the 400/533 MHz DDR2 SDRAM memory subsystem. It features programmable chip selects and support for error-correction codes (ECC). The DDR2 Memory Controller is multi-ported with the following interfaces: south internal bus, ADMA controllers, north internal bus. The memory controller interface configuration support includes unbuffered DIMMs, registered DIMMs, and discrete DDR2 SDRAM devices.

2.2.7 SRAM Memory Controller

The SRAM Memory Controller allows direct control of a 1.0 MByte SRAM memory subsystem. It supports error correction codes (ECC). The SRAM Memory Controller is ported with the following port: North internal bus.

2.2.8 Peripheral Bus Interface

The Peripheral Bus Interface Unit is a data communication path to the flash memory components or other peripherals of a 81348 hardware system. The PBI includes support for either 8- or 16-bit devices. To perform these tasks at high bandwidth, the bus features a burst-transfer capability which allows successive 8/16-bit data transfers.

2.2.9 I²C Bus Interface Units

There are three I²C (Inter-Integrated Circuit) Bus Interface Units that allow the Intel XScale® processor to serve as a master and slave device residing on the I²C bus. The I²C0 allows the I/O processor to interface to a storage enclosure processor, SEP. For more information, refer to *I²C Peripherals for Microcontrollers* (Philips Semiconductor)¹.

2.2.10 UART Units

The 81348 includes two UART units. The UART unit allow the two Intel XScale® processors to serve as a master and slave device residing on the UART bus. The UART units use a serial bus consisting of a two-pin interface. UART0 allows the 81348 to interface to a console port for debugging. Also refer to the National Semiconductor* 16550 device specification².

1. <http://www.semiconductors.philips.com/buses/i2c/>
2. <http://www.national.com/pf/PC/PC16550D.html>



2.2.11 Interrupt Controller Unit

Each Intel XScale® processor supports an Interrupt Controller Unit (ICU). The ICU aggregates interrupt sources both external and internal sources of the 81348 to the Intel XScale® processor. The ICU supports high-performance interrupt processing with direct interrupt service routine vector generation on a per-source basis. Each source has programmability for masking, processor interrupt input, and priority.

2.2.12 XSI System Controller

Each XSI bus (north and south) employs an XSI system controller. The XSI system controller observes all the address or data bus requests from requestors and completors connected to the XSI bus. The XSI system controller handles XSI address bus arbitration, XSI data bus arbitration, framing Address bus cycles, and framing Data bus cycles. The XSI system controller provides the shared address and shared data paths from/to units.

2.2.13 Inter-Processor Communication

Each Intel XScale® processor can interrupt or issue a reset to the second Intel XScale® processor. Each processor can generate up to 32 interrupts to the second processor.

2.2.14 Timers

The 81348 supports two programmable 32-bit timers per processor. The 81348 also supports one watchdog timer per processor.

2.2.15 GPIO

The 81348 includes sixteen General-Purpose I/O (GPIO) pins, and eight ACTIVITY/STATUS pin pairs.



3.0 Package Information

3.1 Package Introduction

The 81348 is offered in a 1357-ball FCBGA5 package.

3.2 Functional Signal Definitions

This section defines the pins and signals.

3.2.1 Signal Pin Descriptions

Table 1. Pin Description Nomenclature

| Symbol | Description |
|-----------|--|
| I | Input pin only |
| O | Output pin only |
| I/O | Pin can be either an input or an output |
| OD | Open-drain pin |
| PWR | Power pin |
| GND | Ground pin |
| — | Pin must be connected as described |
| Sync(...) | Synchronous. Signal meets timings relative to a clock. <ul style="list-style-type: none"> • Sync(P): Synchronous to P_CLKIN • Sync(M): Synchronous to M_CK[2:0] / M_CK#[2:0] • Sync(T): Synchronous to TCK |
| Async | Asynchronous. Inputs can be asynchronous relative to all clocks. All asynchronous signals are level-sensitive. |
| R/W | Indicates read or write capability. |
| Rst(P) | The pin is reset with WARM_RST# or P_RST# . |
| Rst(M) | The pin is reset with M_RST# . M_RST# is asserted when the memory subsystem is reset. |
| Rst(PB) | The pin is reset with PB_RSTOUT# . PB_RSTOUT# is asserted when the Peripheral Bus Interface subsystem is reset. |
| Rst(T) | The pin is reset with TRST# . |
| ActLow | The pin is an active-low signal. |
| Diff | The pin is a differential signal pair. <ul style="list-style-type: none"> • "P" at the end of a differential pin name indicates "positive". • "N" at the end of a differential pin name indicates "negative". |



Table 2. DDR2 SDRAM Signals (Sheet 1 of 2)

| Name | Count | Type | Description |
|----------------------------------|-------|----------------------------------|---|
| M_CK[2:0], M_CK#[2:0] | 6 | O Diff | Memory Clockout: is used to provide the three differential clock pairs to the unbuffered DIMM for the external SDRAM memory subsystem. Registered DIMMs use only the M_CK[0]/M_CK#[0] pair, which drives the input to the on-DIMM PLL. |
| M_RST# | 1 | O Async ActLow | Memory Reset: indicates that the memory subsystem has been reset. It is used to re-initialize registered DIMMs. |
| MA[14:0]^a | 14 | O Sync(M) Rst(M) | Memory Address Bus: carries the multiplexed row and column addresses to the SDRAM memory banks. Auto-precharge is not supported. |
| BA[2:0] | 3 | O Sync(M) Rst(M) | SDRAM Bank Address: controls which of the internal banks to read or write. BA[1:0] are used for 512 Mbit technology memory. BA[2:0] are used for 1 Gbit technology memory. |
| RAS# | 1 | O Sync(M) Rst(M) ActLow | SDRAM Row Address Strobe: indicates the presence of a valid row address on the Multiplexed Address Bus MA[13:0] . |
| CAS# | 1 | O Sync(M) Rst(M) ActLow | SDRAM Column Address Strobe: indicates the presence of a valid column address on the Multiplexed Address Bus MA[13:0] . |
| WE# | 1 | O Sync(M) Rst(M) ActLow | SDRAM Write Enable: indicates whether the current memory transaction is a read or write operation. |
| CS[1:0]# | 2 | O Sync(M) Rst(M) ActLow | SDRAM Chip Select: enables the SDRAM devices for a memory access. One for each physical bank. |
| CKE[1:0] | 2 | O Sync(M) Rst(M) | SDRAM Clock Enable enables: the clocks for the SDRAM memory. Deasserting places the SDRAM in self-refresh mode. One for each physical bank. |
| DQ[63:0] | 64 | I/O Sync(M) Rst(M) | SDRAM Data Bus: carries 64-bit data to and from memory. During the data cycle, read or write data is present on one or more contiguous bytes. During write operations, unused pins drive to determinate values. |
| CB[7:0] | 8 | I/O Sync(M) Rst(M) | SDRAM ECC Check Bits: carry the 8-bit ECC code to and from memory during data cycles. |
| DQS[8:0], DQS#[8:0] | 18 | I/O Sync(M) Rst(M) Diff | SDRAM Data Strobes: carry differential or single-ended strobe signals, output in write mode, and input in read mode for source synchronous data transfer. |
| DM[8:0] | 9 | O Sync(M) Rst(M) | SDRAM Data Mask: controls which bytes on the data bus are to be written. When DM[8:0] is asserted, the SDRAM devices do not accept valid data from the byte lanes. |
| M_VREF | 1 | I | SDRAM Voltage Reference: is used to supply the input switching reference voltage for the memory input signals. |
| ODT[1:0] | 2 | O Sync(M) Rst(M) | On-Die Termination: is used to turn on SDRAM on-die termination during writes. |



Table 2. DDR2 SDRAM Signals (Sheet 2 of 2)

| Name | Count | Type | Description |
|-----------------|-------|------|--|
| M_CAL[0] | 1 | O | Memory Calibration: Connected to an external calibration resistor. Memory output drivers reference the resistor to dynamically adjust drive strength to compensate for temperature and voltage variations. This pin connected through a 24.9 Ω 1% resistor to ground. |
| M_CAL[1] | 1 | O | Memory Calibration: Connected to an external calibration resistor. Memory output drivers reference the resistor to dynamically adjust ODT resistance to compensate for temperature and voltage variations. This pin connected through a 301 Ω 1% resistor to ground. |
| Total | 135 | | |

- a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.



Table 3. Peripheral Bus Interface Signals

| Name | Count | Type | Description |
|-------------------|-------|------------------------|--|
| A[24:0] | 25 | O Rst(PB) | Peripheral Address Bus: carries the address bits for the current access. The PBI interface can address up to 32 MBytes. |
| D[15:0] | 16 | I/O Rst(PB) | Peripheral Data Bus: carries read or write data to and from memory. During write operations to 8-bit wide memory regions, the PBI drives unused bus pins to determinate values. |
| POE# | 1 | O Rst(PB) ActLow | Peripheral Output Enable: indicates whether bus access is write or read with respect to I/O processor and is valid during entire bus access. This pin can be used to control output enable on a peripheral device. 0 = Read 1 = Write |
| PWE# | 1 | O Rst(PB) ActLow | Peripheral Write Enable: indicates to the peripheral device whether or not to write data to the addressed space. This pin can be used to control the write enable on the peripheral device. 0 = Write 1 = Read |
| PCE[1:0]# | 2 | O Rst(PB) ActLow | Peripheral Chip Enable: Specifies which of the two memory address ranges are associated with the current bus access. The pin remains valid during the entire bus access. Note: These pins must be pulled up to V_{CC3P3} with external 8.2K Ω 5%, 1/16 Ω resistors for proper operation. |
| PB_RSTOUT# | 1 | O ActLow | Peripheral Bus Reset Out: can be used to reset the peripheral device. It has the same timing as the internal bus reset. |
| Total | 46 | | |



Table 4. Compact PCI Hot Swap Signals

| Name | Count | Type | Description |
|-----------------------------------|-------|------------------------|---|
| HS_ENUM# | 1 | OD Rst(P) ActLow | Hot Swap Event: Conditionally asserted to notify system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing or quiescing a device driver. |
| HS_LSTAT | 1 | I Rst(P) | Hot Swap Latch Status: Input indicating state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. If Compact PCI Hot Swap not supported, tie this signal low. |
| HS_LED_OUT | 1 | O Rst(P) | Hot Swap LED Output: outputs a logic one to illuminate the Hot Swap blue LED. |
| HS_FREQ[1:0] / CR_FREQ[1:0] | 2 | I/O Rst(P) | Hot Swap Frequency: In Hot Swap mode, these pins are inputs, determining the bus frequency and mode during a PCI-X hot swap event. These are valid only when PCIX_EP# = 0 and HS_SM# = 0. 00 = 133 MHz PCI-X 01 = 100 MHz PCI-X 10 = 66 MHz PCI-X 11 = 33 or 66 MHz. PCI (frequency depends on P_M66EN) Central Resource Frequency: While in Central Resource mode, these pins are outputs, which control the external PCI-X clock generator. These are valid only when PCIX_EP# = 1. 00 = 133 MHz 01 = 100 MHz 10 = 66 MHz 11 = 33 MHz • These pins have internal pull-ups. |
| Total | 5 | | |



Table 5. PCI Bus Signals (Sheet 1 of 3)

| Name | Count | Type | Description |
|-------------|-------|------------------------------------|---|
| P_AD[63:32] | 32 | I/O Sync(P) Rst(P) | PCI Address/Data: is the upper 32 bits of the PCI data bus driven during the data phase. |
| P_AD[31:0] | 32 | I/O Sync(P) Rst(P) | PCI Address/Data: is the multiplexed PCI address and lower 32 bits of the data bus. |
| P_CBE[7]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[6]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[5]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[4]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[3]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[2]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[1]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_CBE[0]# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Command and Byte Enables: are multiplexed on the same PCI pins. During the address phase, they define the bus command. During the data phase, they are used as byte enables. |
| P_PAR64 | 1 | I/O Sync(P) Rst(P) | PCI Bus Upper DWORD Parity is even parity across P_AD[63:32] and P_CBE_#[7:4]. |
| P_REQ64# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Request 64-Bit Transfer indicates the attempt of a 64-bit transaction on the PCI bus. When the target is 64-bit capable, the target acknowledges the attempt with the assertion of P_ACK64_#. |
| P_ACK64# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Acknowledge 64-Bit Transfer indicates that the device has positively decoded its address as the target of the current access and the target is willing to transfer data using the full 64-bit data bus. |



Table 5. PCI Bus Signals (Sheet 2 of 3)

| Name | Count | Type | Description |
|-----------|-------|--|---|
| P_PAR | 1 | I/O Sync(P) Rst(P) | PCI Bus Parity is even parity across P_AD[31:0] and P_CBE_#[3:0]. |
| P_FRAME# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Cycle Frame is asserted to indicate the beginning and duration of an access. |
| P_IRDY# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction. During a write, it indicates that valid data is present on the address/data bus. During a read, it indicates that the processor is ready to accept the data. |
| P_TRDY# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Target Ready indicates the target agent's ability to complete the current data phase of the transaction. During a read, it indicates that valid data is present on the address/data bus. During a write, it indicates that the target is ready to accept the data. |
| P_STOP# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Stop indicates a request to stop the current transaction on the PCI bus. |
| P_DEVSEL# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Device Select is driven by a target agent that has successfully decoded the address. As an input, it indicates whether or not an agent has been selected. |
| P_SERR# | 1 | I/O OD Sync(P) Rst(P) ActLow | PCI Bus System Error is driven for address parity errors on the PCI bus. |
| P_RSTOUT# | 1 | O Async ActLow | PCI Reset Out is based on P_RST# and WARM_RST#. It brings PCI-specific registers, sequencers, and signals to a consistent state. When either P_RST# or WARM_RST# is asserted, it causes P_RSTOUT# to assert and: <ul style="list-style-type: none"> • PCI output signals are driven to a known consistent state. • PCI bus interface output signals are three-stated. • Open-drain signals such as P_SERR_# are floated. P_RSTOUT# can be asynchronous to P_CLK when asserted or deasserted. |
| P_PERR# | 1 | I/O Sync(P) Rst(P) ActLow | PCI Bus Parity Error is asserted when a data parity error occurs during a PCI bus transaction. |
| P_M66EN | 1 | I | PCI Bus 66 MHz Enable indicates the speed of the PCI bus. When this signal is sampled high, the PCI bus speed is 66 MHz; when low, the bus speed is 33 MHz. |
| P_IDSEL | 1 | I Sync(P) | PCI Bus Initialization Device Select is used to select the 81348 during a configuration read or write. Note: In central resource mode this pin must be pulled down to V _{SS} with an external 4.7K Ω 5%, 1/16 Ω resistor for proper operation. |

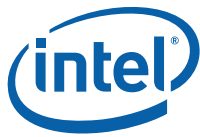


Table 5. PCI Bus Signals (Sheet 3 of 3)

| Name | Count | Type | Description |
|--------------------|-------|----------------------------------|--|
| P_GNT[0]# / P_REQ# | 1 | O Sync(P) ActLow | <p>PCI Bus Grant:</p> <ul style="list-style-type: none"> Internal arbiter mode: This is one of four output grant signals from the internal arbiter. <p>PCI Bus Request:</p> <ul style="list-style-type: none"> External arbiter mode: This is the output request signal for the ATU. |
| P_REQ[0]# / P_GNT# | 1 | I Sync(P) Rst(P) ActLow | <p>PCI Bus Request:</p> <ul style="list-style-type: none"> Internal arbiter mode: This is one of four input request signals to the internal arbiter. <p>PCI Bus Grant:</p> <ul style="list-style-type: none"> External arbiter mode: This is the input grant signal to the ATU. |
| P_GNT[3:1]# | 3 | O Sync(P) ActLow | <p>PCI Bus Grant:</p> <ul style="list-style-type: none"> External arbiter mode: Not used Internal arbiter mode: These are three of four output grant signals from the internal arbiter. |
| P_REQ[3:1]# | 3 | I Sync(P) Rst(P) ActLow | <p>PCI Bus Request:</p> <ul style="list-style-type: none"> External arbiter mode: Not used Internal arbiter mode: These are three of four input request signals to the internal arbiter. |
| P_PCIXCAP | 1 | I | PCI-X Capability: Refer to the <i>Intel® 81348 I/O Processor Specification Update</i> for more details. |
| P_BMI | 1 | O Sync(P) Rst(P) | PCI Bus Master Indicator indicates that the I/O processor is mastering a transaction on the PCI bus. |
| P_CAL[0] | 1 | O | PCI Calibration is connected to an external calibration resistor. The V_{CCVIO} PCI output drivers reference the resistor to dynamically adjust the drive strength to compensate for voltage and temperature variations. This pin is connected through a 22.1 Ω 1% resistor to ground. |
| P_CAL[1] | 1 | O | PCI Calibration is connected to an external calibration resistor. The PCI output drivers reference the resistor to dynamically adjust the ODT resistance to compensate for voltage and temperature variations. This pin is connected through a 121 Ω 1% resistor to ground. |
| P_CAL[2] | 1 | O | PCI Calibration is connected to an external calibration resistor. The V_{CC3P3} PCI output drivers reference the resistor to dynamically adjust the drive strength to compensate for voltage and temperature variations. This pin is connected through a 22.1 Ω 1% resistor to ground. |
| P_CLKIN | 1 | I | PCI Bus Input Clock provides the AC timing reference for all PCI transactions. |
| P_CLKOUT | 1 | O | PCI Bus Output Clock: When REFCLKN/REFCLKP are used, the I/O processor can generate the PCI output clocks. This pin is then connected to P_CLKIN and trace length matched to P_CLKO[3:0] . |
| P_CLKO[3:0] | 4 | O | PCI Bus Output Clocks: When REFCLKN/REFCLKP are used, the I/O processor can generate the PCI output clocks. These pins then provide the PCI clocks to devices on the PCI bus. |
| Total | 105 | | |

**Table 6. PCI Express Signals**

| Name | Count | Type | Description |
|-------------------------|-------|-----------|---|
| REFCLKP, REFCLKN | 2 | I Diff | PCI Express* Clock is the 100 MHz differential input reference clock for the PCI Express* interface. |
| PETP[7:0], PETN[7:0] | 16 | O Diff | PCI Express* Transmit carries the differential output serial data and embedded clock for the PCI Express* interface. |
| PERP[7:0], PERN[7:0] | 16 | I Diff | PCI Express* Receive carries the differential input serial data and embedded clock for the PCI Express* interface. |
| PE_CALP, PE_CALN | 2 | I/O | PCI Express* Calibration pins are connected to an external calibration resistor. The PCI Express* output drivers can reference the resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations. A 1.4K Ω 1% resistor is connected between these two pins. |
| Total | 36 | | |



Table 7. Storage Interface Signals (Sheet 1 of 3)

| Name | Count | Type | Description |
|---------------------------|-------|-----------|---|
| S_CLKNO, S_CLKPO | 2 | I Diff | Storage Clock is the 125 MHz ±100 ppm differential input reference clock for the interface. Note: Should be AC coupled with a 100nF capacitor. |
| S_TXP[7:0], S_TXN[7:0] | 16 | O Diff | Storage Transmit carries the differential output serial data and embedded clock for the interface. Note: Should be AC coupled with a 10nF capacitor. |
| S_RXP[7:0], S_RXN[7:0] | 16 | I Diff | Storage Receive carries the differential input serial data and embedded clock for the interface. Note: Should be AC coupled with a 10nF capacitor. |
| RBIAS[1:0] | 2 | O | Resistor Bias: A 6.49K Ω 1% 1/8 Ω external resistor must be connected between this pin and ground for proper operation. This resistor generates internal bias currents. |
| RBIAS_SENSE[1:0] | 2 | I/O | Resistor Bias Sense is used internally to sense ground. This ball must be connected to the same physical ground point as the RBIAS[1:0] resistor is connected to on the PCB. |
| S_ACT0 / SCLOCK0 | 1 | OD | Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[0]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Clock: (default) When SGPIO[0] is enabled, this pin is the serial output clock running at 99.8 KHz. The falling edge of SCLOCK0 is used to latch SLOAD0 , SDATAOUT0 , and SDATAIN0 . |
| S_STAT0 / SLOAD0 | 1 | OD | Storage Status: When SGPIO[0] is disabled this pin can be used to drive an LED to indicate status of the link for storage engine[0]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Load: (default) When SGPIO[0] is enabled, this pin is the serial load clock. It is driven high to indicate the start of the bit stream. |
| S_ACT1 | 1 | OD | Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[1]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_STAT1 | 1 | OD | Storage Status: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[1]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_ACT2 / SDATAIN0 | 1 | OD | Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[2]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Data In: (default) When SGPIO[0] is enabled, this pin is the serial input data. There are three bits of data per device and up to eight devices are supported. |
| S_STAT2 / SDATAOUT0 | 1 | OD | Storage Status: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[2]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Data Out: (default) When SGPIO[0] is enabled, this pin is the serial output data. There are three bits of data per device and up to eight devices are supported. |



Table 7. Storage Interface Signals (Sheet 2 of 3)

| Name | Count | Type | Description |
|---------------------|-------|------|--|
| S_ACT3 | 1 | OD | Storage Activity: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[3]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_STAT3 | 1 | OD | Storage Status: When SGPIO[0] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[3]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_ACT4 / SCLOCK1 | 1 | OD | Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[4]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Clock: (default) When SGPIO[1] is enabled this pin is the serial output clock running at 99.8 KHz. The falling edge of SCLOCK1 is used to latch SLOAD1, SDATAOUT1 and SDATAIN1. |
| S_STAT4 / SLOAD1 | 1 | OD | Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[4]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Load: (default) When SGPIO[1] is enabled, this pin is the serial load clock. It is driven high to indicate the start of the bit stream. |
| S_ACT5 | 1 | OD | Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[5]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_STAT5 | 1 | OD | Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[5]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_ACT6 / SDATAIN1 | 1 | OD | Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[6]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Data In: (default) When SGPIO[1] is enabled, this pin is the serial input data. There are three bits of data per device and up to eight devices are supported. |
| S_STAT6 / SDATAOUT1 | 1 | OD | Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[6]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. Serial Data Out: (default) When SGPIO[1] is enabled, this pin is the serial output data. There are three bits of data per device and up to eight devices are supported. |



Table 7. Storage Interface Signals (Sheet 3 of 3)

| Name | Count | Type | Description |
|---------|-------|------|--|
| S_ACT7 | 1 | OD | Storage Activity: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate activity on the link for storage engine[7]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| S_STAT7 | 1 | OD | Storage Status: When SGPIO[1] is disabled, this pin can be used to drive an LED to indicate status of the link for storage engine[7]. The pin can be direct driven by the storage engine or driven from an SGPIO. Note: Connect the LED to a series resistor pulled up to VCC. |
| Total | 54 | | |



Table 8. Interrupt Signals

| Name | Count | Type | Description |
|--|-------|---|---|
| P_INT[D:A]# / XINT[3:0]# / GPIO[11:8] | 4 | OD I I/O Async Rst(P) ActLow | <p>When PCIX_EP# = 0:</p> <ul style="list-style-type: none"> PCI Interrupt requests an interrupt from the central resource. The assertion and deassertion is asynchronous. A device asserts its XINT[3:0]# / P_INT[D:A]# line when requesting attention from its device driver. As soon as the XINT[3:0]# / P_INT[D:A]# signal is asserted, it remains asserted until the device driver clears the pending request. <p>When PCIX_EP# = 1:</p> <ul style="list-style-type: none"> External Interrupt requests are used by external devices to request interrupt service. These pins are level-detect inputs and are internally synchronized. These pins go to the XINT[3:0]# inputs of the interrupt controller. The interrupt controller can steer the interrupt to either the FIQ or the IRQ internal interrupt input of the Intel XScale® processor. <p>General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input.</p> |
| XINT[7:4]# / GPIO[15:12] | 4 | I I/O Async ActLow | <p>External Interrupt Requests are used by external devices to request interrupt service. These pins are level-detect and are internally synchronized. These pins go to the XINT[7:4]# inputs of the interrupt controller. The interrupt controller can steer the interrupt to either the FIQ or the IRQ internal interrupt input of the Intel XScale® processor.</p> <p>General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input.</p> |
| GPIO[7:0] / XINT[15:8]# / PMONOUT | 8 | I/O I O Async Rst(p) | <p>General Purpose I/O pins can be selected on a per-pin basis as general-purpose inputs or outputs. The default mode is a general-purpose input.</p> <p>External Interrupts are used by external devices to request interrupt service. These pins are level-detect and are internally synchronized. These pins go to the XINT[15:8]# inputs of the interrupt controller. These interrupts are dedicated to the Intel XScale® processor. To enable a given pin as an interrupt, it needs to be unmasked in the INTCTL[3:0] register.</p> <p>Performance Monitor Out: The PMON unit output indicator generates a signal on the GPIO[7] pin when enabled in the PMONEN register. When enabled it will override the normal GPIO[7] function.</p> |
| HPI# | 1 | I Async ActLow | High-Priority Interrupt causes a high-priority interrupt to the I/O processor. This pin is level-detect only and is internally synchronized. |
| NMIO# | 1 | I Async ActLow | Non-Maskable Interrupt causes a non-maskable data abort to the Intel XScale® processor 0 in the I/O processor. This pin is falling edge-detect only and is internally synchronized. |
| NMI1# | 1 | I Async ActLow | Non-Maskable Interrupt causes a non-maskable data abort to the Intel XScale® processor 1 in the I/O processor. This pin is falling edge-detect only and is internally synchronized. |
| Total | 19 | | |

Table 9. I²C and SM Bus Signals

| Name | Count | Type | Description |
|--------|-------|-----------|--|
| SCL0 | 1 | I/O OD | I ² C 0 Clock provides synchronous operation of the I ² C bus. |
| SDA0 | 1 | I/O OD | I ² C 0 Data is used for data transfer and arbitration of the I ² C bus. |
| SCL1 | 1 | I/O OD | I ² C 1 Clock provides synchronous operation of the I ² C bus. |
| SDA1 | 1 | I/O OD | I ² C 1 Data is used for data transfer and arbitration of the I ² C bus. |
| SCL2 | 1 | I/O OD | I ² C 2 Clock provides synchronous operation of the I ² C bus. |
| SDA2 | 1 | I/O OD | I ² C 2 Data is used for data transfer and arbitration of the I ² C bus. |
| SMBCLK | 1 | I/O OD | SM Bus Clock provides synchronous operation of the SM bus. |
| SMBDAT | 1 | I/O OD | SM Bus Data is used for data transfer and arbitration of the bus. |
| Total | 8 | | |

Note: Open drain outputs require an external pull-up resistor to pull up the signal to 3.3 V. The value of the pull-up resistor depends on the bus loading.



Table 10. UART Signals (Sheet 1 of 2)

| Name | Count | Type | Description |
|---------|-------|----------------------|---|
| U0_RXD | 1 | I Async | UART 0 Serial Input: Serial data input from device pin to the receive shift register. |
| U0_TXD | 1 | O Async | UART 0 Serial Output: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a reset operation. |
| U0_CTS# | 1 | I ActLow Async | <p>UART 0 Clear to Send: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts CTS# high, the transmitting UART must stop transmission to prevent overflow of the receiving UART buffer. The CTS# signal is a modem-status input whose condition can be tested by the host processor or by the UART when in Autoflow Mode as described below:</p> <p>Non-Autoflow Mode: When not in Autoflow Mode, bit[4] (CTS) of the Modem Status Register (MSR) indicates the state of CTS#. Bit[4] is the complement of the CTS# signal. Bit[0] (DCTS) of the Modem Status Register indicates whether the CTS# input has changed state since the previous reading of the Modem Status Register. CTS# has no effect on the transmitter. The user can program the UART to interrupt the processor when DCTS changes state. The programmer can then stall the outgoing data stream by starving the transmit FIFO or disabling the UART with the IER register.</p> <p>Note: When UART transmission is stalled by disabling the UART, the user does not receive an MSR interrupt when CTS# reasserts. This is because disabling the UART also disables interrupts. To work around this, the user can use Auto CTS in Autoflow Mode, or program the CTS# pin to interrupt.</p> <p>Autoflow Mode: In Autoflow Mode, the UART transmit circuitry checks the state of CTS# before transmitting each byte. When CTS# is high, no data is transmitted.</p> |
| U0_RTS# | 1 | O ActLow Async | <p>UART 0 Request to Send: This bit indicates to the remote device whether the UART is ready to receive data. When this bit is low, the UART is ready to receive data. A reset operation sets this signal to its inactive (high) state. LOOP Mode operation holds this signal in its inactive state.</p> <p>Non-Autoflow Mode: The RTS# output signal can be asserted by setting bit[1] (RTS) of the Modem Control Register to 1. The RTS bit is the complement of the RTS# signal.</p> <p>Autoflow Mode: RTS# is automatically asserted by the autoflow circuitry when the receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.</p> |
| U1_RXD | 1 | I Async | UART 1 Serial Input: Serial data input from the device pin to the receive shift register. |



Table 10. UART Signals (Sheet 2 of 2)

| Name | Count | Type | Description |
|---------|-------|----------------------|--|
| U1_TXD | 1 | O Async | UART 1 Serial Output: Composite serial data output to the communications link-peripheral, modem, or data set. The TXD signal is set to the MARKING (logic 1) state upon a reset operation. |
| U1_CTS# | 1 | I ActLow Async | <p>UART 1 Clear to Send: When low, this pin indicates that the receiving UART is ready to receive data. When the receiving UART deasserts CTS# high, the transmitting UART must stop transmission to prevent overflow of the receiving UART buffer. The CTS# signal is a modem-status input whose condition can be tested by the host processor or by the UART when in Autoflow Mode as described below:</p> <p>Non-Autoflow Mode: When not in Autoflow Mode, bit[4] (CTS) of the Modem Status Register (MSR) indicates the state of CTS#. Bit[4] is the complement of the CTS# signal. Bit[0] (DCTS) of the Modem Status Register indicates whether the CTS# input has changed state since the previous reading of the Modem Status Register. CTS# has no effect on the transmitter. The user can program the UART to interrupt the processor when DCTS changes state. The programmer can then stall the outgoing datastream by starving the transmit FIFO or disabling the UART with the IER register.</p> <p>Note: When UART transmission is stalled by disabling the UART, the user does not receive an MSR interrupt when CTS# reasserts. This is because disabling the UART also disables interrupts. To get around this, the user can use Auto CTS in Autoflow Mode, or program the CTS# pin to interrupt.</p> <p>Autoflow Mode: Note: In Autoflow Mode, the UART transmit circuitry checks the state of CTS# before transmitting each byte. When CTS# is high, no data is transmitted.</p> |
| U1_RTS# | 1 | O ActLow Async | <p>UART 1 Request to Send: This bit indicates to the remote device whether the UART is ready to receive data. When low, the UART is ready to receive data. A reset operation sets this signal to its inactive (high) state. LOOP Mode operation holds this signal in its inactive state.</p> <p>Non-Autoflow Mode: The RTS# output signal can be asserted by setting bit[1] (RTS) of the Modem Control Register to 1. The RTS bit is the complement of the RTS# signal.</p> <p>Autoflow Mode: RTS# is automatically asserted by the autoflow circuitry when the receive buffer exceeds its programmed threshold. It is deasserted when enough bytes are removed from the buffer to lower the data level back to the threshold.</p> |
| Total | 8 | | |



Table 11. Miscellaneous Signals

| Name | Count | Type | Description |
|------------------|-------|------------------------|--|
| TCK | 1 | I | Test Clock provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the device on the rising clock edge, and data is clocked out on the falling clock edge. |
| TDI | 1 | I Sync(T) | Test Data Input is the JTAG serial input pin. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port. This signal has a weak internal pull-up to ensure proper operation when this pin is not being driven. |
| TDO | 1 | O Sync(T) Rst(T) | Test Data Output is the serial output pin for the JTAG feature. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats. The behavior of TDO is independent of other resets. |
| TRST# | 1 | I Async ActLow | Test Reset asynchronously resets the Test Access Port controller function of IEEE 1149 Boundary Scan Testing (JTAG). This pin has a weak internal pull-up. Note: This pin must be tied low when not used. |
| TMS | 1 | I Sync(T) | Test Mode Select is sampled on the rising edge of TCK to select the operation of the test logic for IEEE 1149 Boundary Scan testing. This pin has a weak internal pull-up. |
| NC | 54 | I/O | No Connect: Pins have no usable function and must not be connected to any signal, power, or ground. |
| P_RST# | 1 | I Async ActLow | Cold Reset is used to asynchronously reset the I/O processor when it is low. This signal must be asserted whenever the power supplies are outside of the specified ranges. <ul style="list-style-type: none"> Registers are reset to default values. Pins are driven to known states. Sticky configuration bits are reset. |
| WARM_RST# | 1 | I Async ActLow | Warm Reset is the same as a cold reset, except sticky configuration bits are not reset. This pin should only be used when the sticky bit functionality is required. In this scenario, the WARM_RST# pin must be tied to the system reset PCI_RST# signal while the P_RST# pin can be tied to the system power good signal. If the sticky bit functionality is not required, the WARM_RST# pin should not be used and must be tied to Vcc. When the PCI Express interface is used as an endpoint, the PCI Express inband Hot Reset Mechanism can also be used to provide the sticky bit functionality. Note: Driving WARM_RST# using any other methods than suggested above may result in unpredictable behavior of the device. |
| THERMDA | 1 | I | Thermal Diode Anode is the anode of the thermal diode. |
| THERMDC | 1 | O | Thermal Diode Cathode is the cathode of the thermal diode. |
| PUR1 | 1 | I | Pull-Up Required 1: This pin must be pulled up to V _{CC3P3} with an external 8.2K Ω 5%, 1/16 Ω resistor for proper operation. |
| Total | 64 | | |



Table 12. Power and Ground Signals

| Name | Count | Type | Description |
|------------------------|-------|------|--|
| V _{CC1P2PLL0} | 1 | PWR | V _{CC} PLL Storage: Ball connected to a 1.2 V filtered board supply. Provides power to one of two PLLs that control Storage interface. |
| V _{CC1P2PLL1} | 1 | PWR | V _{CC} PLL Storage: Ball connected to a 1.2 V filtered board supply. Provides power to one of two PLLs that control Storage interface. |
| V _{CC1P2PLLP} | 1 | PWR | V _{CC} PLL PCI-X: Ball connected to a 1.2 V filtered board supply. Provides power to PLL that controls the PCI-X logic and interface. |
| V _{CC1P2PLLD} | 1 | PWR | V _{CC} PLL DDR: Ball connected to a 1.2 V filtered board supply. Provides power to the PLL that controls the DDR2 SDRAM interface and processor digital logic. |
| V _{CC3P3PLLX} | 1 | PWR | V _{CC} PLL X: Ball to be connected to a 3.3 V filtered board supply. This pin provides power to a voltage regulator, which supplies power to the PLL that controls the Intel XScale® processor and XSI processor logic. |
| V _{SSPLL0} | 1 | GND | V _{SS} PLL Storage: Ball to be connected to a board ground plane at the location of the V _{CC1P2PLL0} filter. |
| V _{SSPLL1} | 1 | GND | V _{SS} PLL Storage: Ball to be connected to a board ground plane at the location of the V _{CC1P2PLL1} filter. |
| V _{SSPLLP} | 1 | GND | V _{SS} PLL PCI-X: Ball connected to capacitor of the V _{CC1P2PLLP} filter. |
| V _{SSPLLD} | 1 | GND | V _{SS} PLL DDR2 SDRAM: Ball connected to capacitor of V _{CC1P2PLLD} filter. |
| V _{SSPLLX} | 1 | GND | V _{SS} PLL X: Ball connected to capacitor of V _{CC3P3PLLX} filter. |
| V _{CC1P2} | 187 | PWR | 1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the processor logic. |
| V _{CC1P2AE} | 8 | PWR | 1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the PCI Express* analog logic. |
| V _{CC1P2E} | 6 | PWR | 1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the PCI Express* digital logic. |
| V _{CC1P2DS} | 6 | PWR | 1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the storage interface digital logic. |
| V _{CC1P2AS} | 9 | PWR | 1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the storage interface analog logic. |
| V _{CC1P2X} | 119 | PWR | 1.2 V Power: Balls to be connected to a 1.2 V board power plane. These pins provide power to the Intel XScale® processors. |
| V _{CCVIO} | 21 | PWR | VIO Power: Balls to be connected to a 3.3V board power plane. These pins provide 3.3 V power to the PCI-X I/Os. |
| V _{CC1P8} | 30 | PWR | 1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the DDR2 SDRAM interface I/Os. |
| V _{CC1P8E} | 14 | PWR | 1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the PCI Express* interface I/Os. |
| V _{CC1P8S} | 6 | PWR | 1.8 V Power: Balls to be connected to a 1.8 V board power plane. These pins provide power to the storage interface I/Os. |
| V _{CC3P3} | 42 | PWR | 3.3 V Power: Balls to be connected to a 3.3 V board power plane. These pins provide power to the PBI, miscellaneous pins, and PCI-X I/Os in Mode 1. |
| V _{SS} | 373 | GND | Ground: Balls to be connected to a board ground plane. |
| V _{SSE} | 20 | GND | PCI Express* Ground: Balls connected to a board ground plane. |
| V _{SSAS} | 20 | GND | Analog Storage Ground: Balls connected to a board ground plane. |
| V _{SSDS} | 6 | GND | Digital Storage Ground: Balls connected to a board ground plane. |
| Total | 877 | | |



Table 13. Reset Strap Signals (Sheet 1 of 3)

| Name | Count | Type | Description |
|----------------------------|-------|-------------|---|
| BOOT_WIDTH_8# | 1 | Reset Strap | PBI Boot Bus Width: Sets the default bus width for the PBI Memory Boot window. 0 = 8 bits wide 1 = 16 bits wide (default mode) Note: Muxed onto signal A[0] . |
| DF_SEL[2:0] | 3 | Reset Strap | Device Function Select: These straps select the number of storage ports assigned to each function within 81348. Note: DF_SEL[2] muxed onto signal A[9] Note: DF_SEL[1] muxed onto signal A[8] Note: DF_SEL[0] muxed onto signal A[7] See the "Device Function Select" of the Intel® 81348 I/O Processor Developer's Manual for additional details. |
| CFG_CYCLE_EN# | 1 | Reset Strap | Configuration Cycle Enable: Determines whether PCI interface retries configuration cycles until Configuration Cycle Retry bit is cleared in ATU (PCSR[2] and Host Lockout Bit is cleared). 0 = Configuration cycles enabled 1 = Configuration retry enabled (default mode) • PCI-X Interface: Configuration cycles are claimed and terminated with a retry status. • PCI Express* Interface: Configuration requests result in a completion TLP with Configuration Retry Status (CRS). Note: Muxed onto signal A[1] |
| HOLD_X0_IN_RST# | 1 | Reset Strap | Hold Intel XScale® Microprocessor 0 in Reset: Determines whether the Intel XScale® microprocessor number 0 is held in reset until the reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset 1 = Do not hold in reset (default mode) Note: Muxed onto signal A[2] |
| HOLD_X1_IN_RST# | 1 | Reset Strap | Hold Intel XScale® Microprocessor 1 in Reset: Determines whether the Intel XScale® microprocessor number 1 is held in reset until the reset bit is cleared in the PCI Configuration and Status Register. 0 = Hold in reset 1 = Do not hold in reset (default mode) Note: Muxed onto signal A[3] |
| MEM_FREQ[1:0] | 2 | Reset Strap | Memory Frequency: Determines frequency at which DDR2 memory subsystem runs. 00 = Reserved 01 = Reserved 10 = 533 MHz 11 = 400 MHz (Default mode) Note: MEM_FREQ[1] muxed onto signal A[5] Note: MEM_FREQ[0] muxed onto signal A[4] |
| EXT_ARB# | 1 | Reset Strap | External Arbiter: Determines whether the PCI interface enables the integrated arbiter, or use an external arbiter. 0 = External arbiter 1 = Internal arbiter (default mode) Note: Muxed onto signal A[6] |
| INTERFACE_SEL_PCIX# | 1 | Reset Strap | 0 = PCI-X is active 1 = PCI Express is active (default mode) When both interfaces are active, this strap selects the ATU that is function 0 in the internal address map. Note: Muxed onto signal A[10] |
| PCIX_EP# | 1 | Reset Strap | PCI-X End Point: Determines whether the PCI-X interface operates as an endpoint or a central resource. 0 = Endpoint 1 = Central resource (default mode) Note: Muxed onto signal A[11] Note: Setting both PCIX_EP# and PCIE_RC# to endpoint is unsupported. |



Table 13. Reset Strap Signals (Sheet 2 of 3)

| Name | Count | Type | Description |
|---|-------|-------------|---|
| PCIE_RC# | 1 | Reset Strap | PCI-E Root Complex: Determines whether PCI Express* interface operates as an endpoint or a root complex. 0 = Root complex 1 = Endpoint (default mode) Note: Muxed onto signal A[12] Setting both PCIX_EP# and PCIE_RC# to endpoint is unsupported. |
| SMB_A5, SMB_A3, SMB_A2, SMB_A1 | 4 | Reset Strap | SM Bus Address: Maps to address bit[5], bit[3], bit[2], and bit[1] where bits[7:0] represent address SMBus slave port responds to when access is attempted. 0 = Address bit is low 1 = Address bit is high (default mode) Note: SMB_A5 muxed onto signal A[16] Note: SMB_A3 muxed onto signal A[15] Note: SMB_A2 muxed onto signal A[14] Note: SMB_A1 muxed onto signal A[13] |
| PCIX_PULLUP# | 1 | Reset Strap | PCI-X Pull Up: Determines whether PCI interface has on-die pull-ups enabled. These may be used for the central resource bus keepers. 0 = Enable PCI pull-up resistors 1 = Disable PCI pull-up resistors (default mode) Note: Muxed onto signal A[17] |
| PCIX_32BIT# | 1 | Reset Strap | 32-Bit PCI-X Bus: Indicates width of the PCI-X bus to PCI-X Status Register. Enables pull-ups for upper half of bus when in 32-bit mode. 0 = 32-bit wide PCI-X bus 1 = 64-bit wide PCI-X bus (default mode) Note: Muxed onto signal A[18] |
| PCIXM1_100# | 1 | Reset Strap | PCI-X Mode 1 100 MHz Enable: In Central Resource Mode, this bit limits PCI-X bus to 100 MHz while in mode 1: 0 = Limit PCI-X mode 1 to 100 MHz 1 = 133 MHz enabled (default mode) Note: Muxed onto signal A[19] |
| HS_SM# | 1 | Reset Strap | Hot Swap Startup Mode: In End Point Mode, this bit determines whether Hot Swap mode is enabled. 0 = Hot Swap Mode enabled 1 = Hot Swap Mode disabled (default mode) Note: Muxed onto signal A[21] |
| FW_TIMER_OFF# | 1 | Reset Strap | Firmware Timer Off: Disables 400 mS firmware timer for development and debug. When enabled, timer automatically clears Configuration Cycle Retry (CCR) bit in PCSR after 400 mS regardless of processor state. When disabled, CCR bit functions as normal based on state of CFG_CYCLE_EN# pin at rising edge of P_RST#. 0 = Firmware timer disabled 1 = Firmware timer enabled (default mode) Note: Muxed onto signal A[22] |
| CONTROLLER_ONLY# | 1 | Reset Strap | Controller-Only Enable: 0 = Controller only, RAID disabled 1 = RAID enabled (default mode) Note: Muxed onto signal A[23] |
| LK_DN_RST_BYPASS# | 1 | Reset Strap | Link Down Reset Bypass: Disables the full chip reset that would normally be caused by a Link Down or hot reset. 0 = Do not reset on Link Down 1 = Reset on Link Down (default mode) Note: Muxed onto signal A[24] |



Table 13. Reset Strap Signals (Sheet 3 of 3)

| Name | Count | Type | Description |
|---------------|-------|-------------|--|
| CLK_SRC_PCIE# | 1 | Reset Strap | Clock Source PCI-E: Selects PCI Express* Refclk pair as the input clock to the PLLs that control most internal logic. 0 = Source clock is REFCLKP/REFCLKN 1 = Source clock is P_CLKIN (default mode) Note: When P_CLKO[3:0] are used this pin must be pulled low. Note: Muxed onto signal PWE# |
| Total | 25 | | |

Reset strap signals are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default. An external 4.7K ohm 5%, 1/16 ohm pull-down resistor is required to force a logic 0 on these pins.



Table 14. Functional Pin Mode Behavior (Sheet 1 of 4)

| Pin | Boundary Scan High Z | Reset (End Point) | Reset (Central Resource) | Normal | 32-Bit SDRAM | PCIX_32BIT# | PCIX_PULLUP# | When only PCI-X Interface Active | When only PCI Express* Interface Active |
|-----------------------------|----------------------|-------------------|--------------------------|--------|--------------|-------------|--------------|----------------------------------|---|
| M_CK[2:0], M_CK#[2:0] | Z | VO | VO | VO | - | - | - | - | - |
| M_RST# | Z | 0* | 0* | VO | - | - | - | - | - |
| MA[14:0] ^a | Z | VO | VO | VO | - | - | - | - | - |
| BA[2:0] | Z | VO | VO | VO | - | - | - | - | - |
| RAS# | Z | VO | VO | VO | - | - | - | - | - |
| CAS# | Z | VO | VO | VO | - | - | - | - | - |
| WE# | Z | VO | VO | VO | - | - | - | - | - |
| CS[1:0]# | Z | VO | VO | VO | - | - | - | - | - |
| CKE[1:0] | Z | 0* | 0* | VO | - | - | - | - | - |
| DQ[63:32] | Z | Z* | Z* | VB | Z | - | - | - | - |
| DQ[31:0] | Z | Z* | Z* | VB | - | - | - | - | - |
| CB[7:0] | Z | Z* | Z* | VB | - | - | - | - | - |
| DQS[8], DQS#[8] | Z | Z* | Z* | VB | - | - | - | - | - |
| DQS[7:4], DQS#[7:4] | Z | Z* | Z* | VB | Z | - | - | - | - |
| DQS[3:0], DQS#[3:0] | Z | Z* | Z* | VB | - | - | - | - | - |
| DM[8] | Z | VO* | VO* | VO | - | - | - | - | - |
| DM[7:4] | Z | VO* | VO* | VO | - | - | - | - | - |
| DM[3:0] | Z | VO* | VO* | VO | - | - | - | - | - |
| M_VREF | - | AI | AI | AI | - | - | - | - | - |
| ODT[1:0] | Z | 0* | 0* | VO | - | - | - | - | - |
| M_CAL[1:0] | Z | Z* | Z* | AO | - | - | - | - | - |
| A[24:0] | Z | H | H | VO | - | - | - | - | - |
| D[15:0] | Z | H | H | VB | - | - | - | - | - |
| POE# | Z | H | H | VO | - | - | - | - | - |
| PWE# | Z | H | H | VO | - | - | - | - | - |
| PB_RSTOUT# | Z | 0 | 0 | VO | - | - | - | - | - |
| PCE[1:0]# | Z | H | H | VO | - | - | - | - | - |
| HS_ENUM# | Z | Z | Z | VO | - | - | - | - | - |
| HS_LSTAT | - | VI | VI | VI | - | - | - | - | - |
| HS_LED_OUT | Z | 1 | 1 | VO | - | - | - | - | - |
| HS_FREQ[1:0] / CR_FREQ[1:0] | Z | H | H | H | - | - | - | - | - |

Notes:

1 = driven to V_{CC}
 0 = driven to V_{SS}
 X = driven to unknown state
 ID = The input is disabled.
 H = pulled up to V_{CC}
 PD = pull-up disabled
 L = pulled down to V_{SS}
 ODT = On Die Termination
 GND = Tie to Ground.

EA = External Arbiter mode
 IA = Internal Arbiter mode
 Z = output, pull-up/down disabled
 VB = acts like a Valid Bidirectional pin
 VO = a Valid Output level is driven.
 VI = need to drive a Valid Input level.
 AO = Analog Output level
 AI = Analog Input level
 * = after power fail sequence completes
 "-" = unaffected by this mode

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.



Table 14. Functional Pin Mode Behavior (Sheet 2 of 4)

| Pin | Boundary Scan High Z | Reset (End Point) | Reset (Central Resource) | Normal | 32-Bit SDRAM | PCIX_32BIT# | PCIX_PULLUP# | When only PCI-X Interface Active | When only PCI Express* Interface Active |
|------------------------|----------------------|--|---|---|--------------|-------------|--------------|----------------------------------|---|
| P_AD[63:32] | Z | Z | Z | VB | - | H | H | - | H |
| P_AD[31:0] | Z | Z | 0 | VB | - | - | - | - | H |
| P_CBE[7:4]# | Z | Z | Z | VB | - | H | H | - | H |
| P_CBE[3:0]# | Z | Z | 0 | VB | - | - | - | - | H |
| P_PAR64 | Z | Z | Z | VB | - | H | H | - | H |
| P_REQ64# | Z | VI | 0 | VB | - | - | H | - | H |
| P_ACK64# | Z | Z | Z | VB | - | - | H | - | H |
| P_PAR | Z | Z | 0 | VB | - | - | - | - | H |
| P_FRAME# | Z | VI | VO | VB | - | - | H | - | H |
| P_IRDY# | Z | VI | VO | VB | - | - | H | - | H |
| P_TRDY# | Z | VI | VO | VB | - | - | H | - | H |
| P_STOP# | Z | VI | VO | VB | - | - | H | - | H |
| P_DEVSEL# | Z | VI | VO | VB | - | - | H | - | H |
| P_SERR# | Z | Z | Z | VB | - | - | H | - | H |
| P_RSTOUT# | Z | 0 | 0 | VO | - | - | - | - | VO |
| P_PERR# | Z | VI | VO | VB | - | - | H | - | H |
| P_M66EN | - | VI | VI | VI | - | - | - | - | H |
| P_IDSEL | - | VI | VI | VI | - | - | - | - | H |
| P_GNT[0]# / P_REQ# | Z | Z _(EA) H _(IA) | Z _(EA) H _(IA) | VO | - | - | - | - | H |
| P_REQ[0]# / P_GNT# | - | VI _(EA) | VI _(EA) H _(IA) | VI _(EA) H _(IA) | - | - | - | - | H |
| P_GNT[3:1]# | Z | H | H | VO | - | - | - | - | H |
| P_REQ[3:1]# | - | H | H | H | - | - | - | - | H |
| P_CLKIN | - | VI | VI | VI | - | - | - | - | GND |
| P_CLKOUT | Z | Z | VO | VO | - | - | - | - | Z |
| P_CLKO[3:0] | Z | Z | VO | VO | - | - | - | - | Z |
| P_PCIXCAP | - | AI | AI | AI | - | - | - | - | GND |
| P_BMI | Z | VO | VO | VO | - | - | - | - | VO |
| P_CAL[2:0] | Z | AO | AO | AO | - | - | - | - | VO |
| S_CLKP0, S_CLKN0 | - | VI | VI | VI | - | - | - | - | - |
| S_TXP[7:0], S_TXN[7:0] | - | 1 | 1 | VO | - | - | - | - | - |
| S_RXP[7:0], S_RXN[7:0] | - | ID | ID | VI | - | - | - | - | - |

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 H = pulled up to V_{CC}
 PD = pull-up disabled
 L = pulled down to V_{SS}
 ODT = On Die Termination
 GND = Tie to Ground.

EA = External Arbiter mode
 IA = Internal Arbiter mode
 Z = output, pull-up/down disabled
 VB = acts like a Valid Bidirectional pin
 VO = a Valid Output level is driven.
 VI = need to drive a Valid Input level.
 AO = Analog Output level
 AI = Analog Input level
 * = after power fail sequence completes
 "-" = unaffected by this mode

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.



Table 14. Functional Pin Mode Behavior (Sheet 3 of 4)

| Pin | Boundary Scan High Z | Reset (End Point) | Reset (Central Resource) | Normal | 32-Bit SDRAM | PCIX_32BIT# | PCIX_PULLUP# | When only PCI-X Interface Active | When only PCI Express* Interface Active |
|-----------------------------------|----------------------|-------------------|--------------------------|--------|--------------|-------------|--------------|----------------------------------|---|
| RBIAS[1:0] | - | AO | AO | AO | - | - | - | - | - |
| RBIAS_SENSE[1:0] | - | AI | AI | AI | - | - | - | - | - |
| S_ACT0 / SCLOCK0 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT0 / SLOAD0 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT1 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT1 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT2 / SDATAIN0 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT2 / SDATAOUT0 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT3 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT3 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT4 / SCLOCK1 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT4 / SLOAD1 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT5 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT5 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT6 / SDATAIN1 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT6 / SDATAOUT1 | Z | Z | Z | VO | - | - | - | - | - |
| S_ACT7 | Z | Z | Z | VO | - | - | - | - | - |
| S_STAT7 | Z | Z | Z | VO | - | - | - | - | - |
| REFCLKP, REFCLKN | - | VI | VI | VI | - | - | - | GND/VI | - |
| PETP[7:0], PETN[7:0] | - | Z | Z | VO | - | - | - | Z | - |
| PERP[7:0], PERN[7:0] | - | ID | ID | VI | - | - | - | Z | - |
| PE_CALP | - | AO | AO | AO | - | - | - | Z | - |
| PE_CALN | - | AO | AO | AO | - | - | - | Z | - |
| P_INT[D:A]# / XINT[3:0]# | Z | Z/VI | Z/VI | VB | - | - | H | - | - |
| XINT[7:4]# | - | VI | VI | VI | - | - | - | - | - |
| GPIO[7:0] / XINT[15:8]# / PMONOUT | Z | VI | VI | VB | - | - | - | - | - |
| HPI# | - | VI | VI | VI | - | - | - | - | - |
| NMI0# | - | VI | VI | VI | - | - | - | - | - |
| NMI1# | - | VI | VI | VI | - | - | - | - | - |
| SCL0 | Z | Z | Z | VB | - | - | - | - | - |

Notes:

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 ID = The input is disabled.
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 L = pulled down to V_{SS}
 ODT = On Die Termination
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 VI = need to drive a Valid Input level.
 AO = Analog Output level
 AI = Analog Input level
 * = after power fail sequence completes
 "-" = unaffected by this mode

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.



Table 14. Functional Pin Mode Behavior (Sheet 4 of 4)

| Pin | Boundary Scan High Z | Reset (End Point) | Reset (Central Resource) | Normal | 32-Bit SDRAM | PCIX_32BIT# | PCIX_PULLUP# | When only PCI-X Interface Active | When only PCI Express* Interface Active |
|-----------|----------------------|-------------------|--------------------------|--------|--------------|-------------|--------------|----------------------------------|---|
| SDA0 | Z | Z | Z | VB | - | - | - | - | - |
| SCL1 | Z | Z | Z | VB | - | - | - | - | - |
| SDA1 | Z | Z | Z | VB | - | - | - | - | - |
| SCL2 | Z | Z | Z | VB | - | - | - | - | - |
| SDA2 | Z | Z | Z | VB | - | - | - | - | - |
| SMBCLK | Z | Z | Z | VB | - | - | - | - | - |
| SMBDAT | Z | Z | Z | VB | - | - | - | - | - |
| U0_RXD | - | VI | VI | VI | - | - | - | - | - |
| U0_TXD | Z | 1 | 1 | VO | - | - | - | - | - |
| U0_CTS# | - | VI | VI | VI | - | - | - | - | - |
| U0_RTS# | Z | 1 | 1 | VO | - | - | - | - | - |
| U1_RXD | - | VI | VI | VI | - | - | - | - | - |
| U1_TXD | Z | 1 | 1 | VO | - | - | - | - | - |
| U1_CTS# | - | VI | VI | VI | - | - | - | - | - |
| U1_RTS# | Z | 1 | 1 | VO | - | - | - | - | - |
| TCK | - | VI | VI | VI | - | - | - | - | - |
| TDI | - | H | H | H | - | - | - | - | - |
| TDO | - | Z | Z | VO | - | - | - | - | - |
| TRST# | - | H | H | H | - | - | - | - | - |
| TMS | - | H | H | H | - | - | - | - | - |
| P_RST# | - | VI | VI | VI | - | - | - | - | - |
| WARM_RST# | - | VI | VI | VI | - | - | - | - | - |
| NC | -/Z | Z/H | Z/H | Z/H | - | - | - | - | - |
| THERMDA | - | AI | AI | AI | - | - | - | - | - |
| THERMDC | - | AO | AO | AO | - | - | - | - | - |

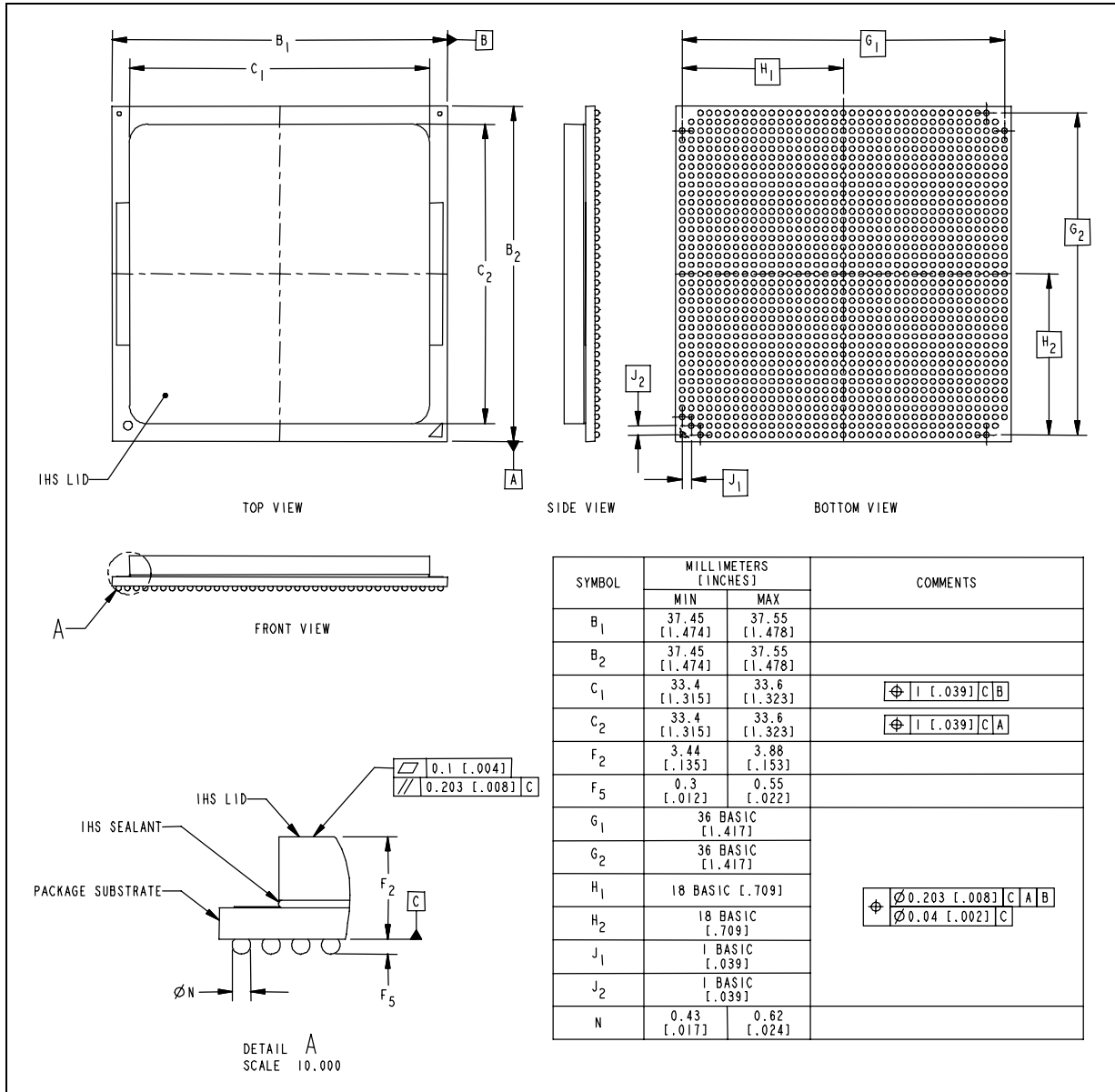
Notes:

1 = driven to V_{CC}
 0 = driven to V_{SS}
 X = driven to unknown state
 ID = The input is disabled.
 H = pulled up to V_{CC}
 PD = pull-up disabled
 L = pulled down to V_{SS}
 ODT = On Die Termination
 GND = Tie to Ground.

EA = External Arbiter mode
 IA = Internal Arbiter mode
 Z = output, pull-up/down disabled
 VB = acts like a Valid Bidirectional pin
 VO = a Valid Output level is driven.
 VI = need to drive a Valid Input level.
 AO = Analog Output level
 AI = Analog Input level
 * = after power fail sequence completes
 "-" = unaffected by this mode

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.

Figure 2. 1357-Lead FCBGA Package (Top and Bottom Views)





The following figures show the Intel® 81348 ballout diagrams:

- Figure 3, "Intel® 81348 I/O processor Ballout—Package Top (Left Side)" on page 42
- Figure 4, "Intel® 81348 I/O processor Ballout—Package Top (Right Side)" on page 43
- Figure 5, "Intel® 81348 I/O processor Ballout—Package Bottom (Left Side)" on page 44
- Figure 6, "Intel® 81348 I/O processor Ballout—Package Bottom (Right Side)" on page 45

The following tables show the Intel® 81348 ball and signal listings:

- Table 15, "Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings" on page 46
- Table 16, "Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings" on page 54



Figure 3. Intel® 81348 I/O processor Ballout—Package Top (Left Side)

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | W |
|----|-----------|------------|------------|-------------|-----------------|-----------|------------|------------|-------------|-----------|------------|-----------|-----------|------------|-----------|----------|------------|-----------|------------|
| 37 | | | vss | dq [63] | dqs [7] | dqs# [7] | dq [57] | dq [56] | dq [60] | dq [43] | dq [47] | dqs [5] | dqs# [5] | dq [41] | dq [40] | dq [44] | cb [2] | cb [6] | dqs# [8] |
| 36 | | vss | dq [59] | dq [58] | dq [62] | vss | dm [7] | dq [61] | vss | vss | dq [42] | dq [46] | vss | dm [5] | dq [45] | vss | cb [3] | cb [7] | dqs [9] |
| 35 | vss | nc | dq [51] | dq [50] | dqs [6] | dqs# [6] | dm [6] | dq [53] | dq [52] | dq [36] | dq [34] | dqs [4] | dqs# [4] | dm [4] | dq [37] | dq [36] | m_ck# [2] | vss | dm [8] |
| 34 | nc | nc | vss | dq [55] | dq [54] | vss | dq [49] | dq [48] | vss | vss | dq [39] | dq [38] | vss | dq [33] | dq [32] | vss | m_ck [2] | m_ck# [0] | m_ck [0] |
| 33 | nc | nc | ma[14] | nc | vss | odt [1] | cs# [1] | ma [13] | odt [0] | cas# | we# | vss | cs# [0] | ras# | ba [0] | ma [10] | ba [1] | ma [0] | vss |
| 32 | nc | nc | nc | nc | nc | vcc3 p3 | vcc3 p3 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 |
| 31 | nc | nc | nc | nc | nc | vcc3 p3 | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 30 | nc | vss | nc | vss | nc | nc | vcc3 p3 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 29 | nc | nc | nc | nc | nc | nc | vcc3 p3 | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | therm da |
| 28 | nc | nc | nc | nc | nc | nc | vcc3 p3 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | therm dc |
| 27 | s_act1 | vss | s_stat5 | vss | s_act4 | s_stat3 | vcc3 p3 | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 26 | s_act5 | s_stat2 | s_act0 | s_stat7 | s_stat6 | s_stat4 | vcc3 p3 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 25 | s_stat0 | s_act2 | s_act3 | s_act7 | s_stat1 | s_act6 | vcc3 p3 | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 24 | vssas | vssas | vssas | vssas | vcc1 p2as | vcc1 p2as | vcc1 p2as | vss | vcc1 p2 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 23 | s_rxp[3] | s_rxn[3] | s_txp[3] | s_txn[3] | vcc1 p2as | vcc1 p2as | vcc1 p2as | vcc1 p2 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 22 | s_rxp[1] | s_rxn[1] | s_txp[1] | s_txn[1] | vcc1 p2as | vcc1 p2as | vcc1 p2as | vss | vcc1 p2 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 21 | vssas | vssas | vssas | vssas | rbias_sense [0] | nc | nc | s_clkp0 | vsspll0 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 20 | s_rxp[0] | s_rxn[0] | s_txp[0] | s_txn[0] | rbias [0] | nc | nc | s_clkno | vcc1 p2pll0 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 19 | s_rxp[2] | s_rxn[2] | s_txp[2] | s_txn[2] | vcc1 p8s | vcc1 p8s | vcc1 p8s | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 18 | vssas | vssas | vssas | vssas | vcc1 p8s | vcc1 p8s | vcc1 p8s | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 17 | s_rxp[7] | s_rxn[7] | s_txp[7] | s_txn[7] | vcc1 p2ds | vssds | vssds | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 16 | s_rxp[5] | s_rxn[5] | s_txp[5] | s_txn[5] | rbias_sense [1] | nc | nc | vss | vsspll1 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 15 | vssas | vssas | vssas | vssas | rbias [1] | nc | nc | vss | vcc1 p2pll1 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 14 | s_rxp[4] | s_rxn[4] | s_txp[4] | s_txn[4] | vssds | vcc1 p2ds | vssds | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 13 | s_rxp[6] | s_rxn[6] | s_txp[6] | s_txn[6] | vcc1 p2ds | vssds | vcc1 p2ds | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 12 | vssas | vssas | vssas | vssas | vssds | vcc1 p2ds | vcc1 p2ds | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 11 | gpio [1] | gpio [3] | gpio [7] | gpio [6] | gpio [4] | vcc3 p3 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 10 | gpio [0] | vss | gpio [2] | vss | gpio [4] | vcc3 p3 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 9 | xint# [1] | xint# [3] | xint# [5] | xint# [4] | xint# [7] | vcc3 p3 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 8 | xint# [2] | xint# [0] | xint# [6] | nmi# | hs_led_out | vcc3 p3 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 7 | hs_enum# | vss | hpi# | vss | nmi1# | vcc3 p3 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 6 | u0_rts# | u0_rx_d | hs_tstat | hs_freq [1] | hs_freq [0] | vcc3 p3 | vcc3 p3 | vccvbio | vcc3 p3 | vcc3 p3 | vccvbio | vccvbio | vcc3 p3 | vccvbio | vcc3 p3 | vcc3 p3 | vccvbio | vcc3 p3 | vcc3 p3 |
| 5 | u0_cts# | u0_tx_d | u1_rx_d | nc | vcc3 p3 | p_cal [0] | p_gnt# [0] | vccvbio | p_gnt# [0] | p_ad [31] | vccvbio | p_ad [26] | p_idsel | vccvbio | p_ad [16] | p_trdy# | vccvbio | p_ad [13] | p_ad [9] |
| 4 | u1_cts# | u1_tx_d | u1_rts# | vss | warm_rst# | p_rst# | vss | p_req# [0] | p_gnt# [1] | vss | p_ad [30] | p_ad [24] | vss | p_ad [20] | p_frame# | vss | p_par | p_ad [11] | vss |
| 3 | vss | p_clk0 [3] | p_clk0 [2] | p_cal [2] | nc | p_cal [1] | p_req# [2] | p_gnt# [2] | nc | p_ad [27] | p_ad [29] | p_ad [23] | p_ad [22] | p_ad [18] | p_devsel# | p_stop# | p_ad [15] | p_ad [12] | p_cbe# [0] |
| 2 | | | p_clk0 [0] | p_clkout | vss | p_rst# | vss | nc | nc | vss | p_ad [25] | p_ad [21] | vss | p_cbe# [2] | p_pccxcap | vss | p_cbe# [1] | p_ad [10] | vss |
| 1 | | | vss | p_dkin | p_clk0 [1] | p_rstout# | nc | p_req# [1] | p_req# [0] | p_ad [28] | p_cbe# [3] | p_ad [19] | p_ad [17] | p_rdy# | p_perr# | p_serr# | p_ad [14] | p_m66en | vss |

a. MA[14] only needed for 4GB memory support, otherwise this pin is NC.



Figure 4. Intel® 81348 I/O processor Ballout—Package Top (Right Side)

| Y | AA | AB | AC | AD | AE | AF | AG | AH | AJ | AK | AL | AM | AN | AP | AR | AT | AU | |
|------------|-----------|------------|------------|-------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|----------|----------|------------|-----------|----------|----|
| cb [1] | cb [0] | dq [27] | dq [31] | dqs [3] | dqs# [3] | dq [25] | dq [24] | dq [28] | dq [11] | dq [15] | dqs [1] | dqs# [1] | dq [9] | dm [1] | vss | | | 37 |
| cb [5] | cb [4] | vss | dq [26] | dq [30] | vss | dm [3] | dq [29] | vss | vss | dq [10] | dq [14] | vss | dq [8] | dq [13] | dq [12] | vss | | 36 |
| vss | m_ck [1] | dq [19] | dq [18] | dqs [2] | dqs# [2] | dm [2] | dq [21] | dq [20] | dq [3] | dq [2] | dqs [0] | dqs# [0] | dm [0] | dq [5] | dq [4] | m_cal [0] | vss | 35 |
| ma [2] | m_ck# [1] | vss | dq [23] | dq [22] | vss | dq [17] | dq [16] | vss | vss | dq [7] | dq [6] | vss | dq [1] | dq [0] | vss | m_cal [1] | vss | 34 |
| ma [1] | ma [3] | ma [4] | ma [6] | vss | ma [5] | ma [9] | ma [7] | ma [9] | ma [11] | ma [12] | vss | ba [2] | cke [0] | cke [1] | m_rst# | m_vref | vss | 33 |
| vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | 32 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc3 p3 | vcc3 p3 | vss | tck | vss | trst# | 31 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc3 p3 | vcc3 p3 | vcc3 p3 | tdo | tms | tdi | 30 |
| vcc3 p3plx | vss | vcc1 p2x | vssplld | vcc1 p2plld | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc3 p3 | sd1 | sda2 | sda1 | sc10 | smbclk | 29 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc3 p3 | sd2 | vss | sda0 | vss | smbdat | 28 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | 27 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p8e | 26 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p8e | vcc1 p8e | vsse | vsse | vsse | vsse | 25 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc1 p8e | vcc1 p8e | petn [7] | petp [7] | pern [7] | perp [7] | 24 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p8e | petn [6] | petp [6] | pern [6] | perp [6] | 23 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p8e | vsse | vsse | vsse | vsse | vsse | 22 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p8e | petn [5] | petp [5] | pern [5] | perp [5] | 21 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | refclkp | nc | nc | pe_cal p | petn [4] | petp [4] | pern [4] | perp [4] | 20 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | refclkn | nc | nc | pe_cal n | vsse | vsse | vsse | vsse | 19 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p8e | petn [3] | petp [3] | pern [3] | perp [3] | 18 | |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p8e | petn [2] | petp [2] | pern [2] | perp [2] | 17 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p2e | vsse | vsse | vsse | vsse | 16 | |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2ae | vcc1 p2e | petn [1] | petp [1] | pern [1] | perp [1] | 15 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2e | vcc1 p2e | petn [0] | petp [0] | pern [0] | perp [0] | 14 | |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2e | vsse | vsse | vsse | vsse | 13 | |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | 12 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc3 p3 | pce# [1] | a [21] | a [19] | a [18] | a [22] | 11 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc3 p3 | a [20] | vss | pce# [0] | vss | a [19] | 10 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc3 p3 | nc | a [9] | a [12] | a [8] | a [14] | 9 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc3 p3 | PUR1 | a [10] | pb_rstout# | a [1] | a [6] | 8 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc3 p3 | a [11] | vss | a [15] | vss | a [2] | 7 |
| vccvio | vccvio | vcc3 p3 | vccvio | vcc3 p3 | vccvio | vccvio | vcc3 p3 | vccvio | vccvio | vcc3 p3 | vcc3 p3 | d [15] | a [16] | a [17] | a [3] | a [7] | 6 | |
| p_ad [4] | vccvio | p_cbe# [7] | p_parr#4 | vccvio | p_ad [56] | p_ad [52] | vccvio | p_ad [44] | p_ad [40] | vccvio | p_ad [32] | d [10] | vcc3 p3 | d [9] | d [4] | a [4] | a [5] | 5 |
| p_ad [6] | p_ad [0] | vss | p_cbe# [5] | p_ad [60] | vss | p_ad [54] | p_ad [48] | vss | p_ad [42] | p_ad [36] | vss | pce# [2] | d [2] | vss | d [3] | d [8] | d [1] | 4 |
| p_ad [5] | p_ad [2] | p_req#4# | p_ad [63] | p_ad [62] | p_ad [58] | p_ad [51] | p_ad [50] | p_ad [46] | p_ad [39] | p_ad [38] | p_ad [34] | pwe# [12] | d [11] | d [11] | a [20] | d [0] | vss | 3 |
| p_ad [7] | p_ad [1] | vss | p_cbe# [4] | p_ad [59] | vss | p_ad [53] | p_ad [47] | vss | p_ad [41] | p_ad [35] | vss | d [14] | d [6] | d [5] | a [0] | vss | | 2 |
| p_ad [8] | p_ad [3] | p_ack#4# | p_cbe# [6] | p_ad [61] | p_ad [57] | p_ad [55] | p_ad [49] | p_ad [45] | p_ad [43] | p_ad [37] | p_ad [33] | a [24] | d [7] | d [13] | vss | | | 1 |



Figure 5. Intel® 81348 I/O processor Ballout—Package Bottom (Left Side)

| | AU | AT | AR | AP | AN | AM | AL | AK | AJ | AH | AG | AF | AE | AD | AC | AB | AA | Y | W |
|----|----------|-----------|-------------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|------------|------------|-----------|-------------|------------|
| 37 | | | vss | dm [1] | dq [9] | dqs# [1] | dqs [1] | dq [15] | dq [11] | dq [28] | dq [24] | dq [25] | dqs# [3] | dqs [3] | dq [31] | dq [27] | cb [0] | cb [1] | dqs# [8] |
| 36 | | vss | dq [12] | dq [13] | dq [8] | vss | dq [14] | dq [10] | vss | vss | dq [29] | dm [3] | vss | dq [30] | dq [26] | vss | cb [4] | cb [5] | dqs [8] |
| 35 | vss | m_cal [0] | dq [4] | dq [5] | dm [0] | dqs# [0] | dqs [0] | dq [2] | dq [3] | dq [20] | dq [21] | dm [2] | dqs# [2] | dqs [2] | dq [18] | dq [19] | m_ck [1] | vss | dm [8] |
| 34 | vss | m_cal [1] | vss | dq [0] | dq [1] | vss | dq [6] | dq [7] | vss | vss | dq [16] | dq [17] | vss | dq [22] | dq [23] | vss | m_ck# [1] | ma [2] | m_ck [0] |
| 33 | vss | m_wrf | m_rst# | cke [1] | cke [0] | ba [2] | vss | ma [12] | ma [11] | ma [9] | ma [7] | ma [8] | ma [5] | vss | ma [6] | ma [4] | ma [3] | ma [1] | vss |
| 32 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 |
| 31 | trst# | vss | tkc | vss | vcc3 p3 | vcc3 p3 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 30 | tdi | tms | tdo | vcc3 p3 | vcc3 p3 | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc1 p2x |
| 29 | smbclk | sclo | sda1 | sda2 | sc1 | vcc3 p3 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2ppld | vssplld | vcc1 p2x | vss | vcc3 p3pplx | nc |
| 28 | smbdat | vss | sda0 | vss | sc2 | vcc3 p3 | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 27 | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 26 | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p8e | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 25 | vsse | vsse | vsse | vsse | vcc1 p8e | vcc1 p8e | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 24 | perp [7] | pern [7] | petp [7] | petn [7] | vcc1 p8e | vcc1 p2ae | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 23 | perp [6] | pern [6] | petp [6] | petn [6] | vcc1 p8e | vcc1 p2ae | vss | vcc1 p2 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss |
| 22 | vsse | vsse | vsse | vsse | vcc1 p8e | vcc1 p2ae | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x |
| 21 | perp [5] | pern [5] | petp [5] | petn [5] | vcc1 p8e | vcc1 p2ae | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 20 | perp [4] | pern [4] | petp [4] | petn [4] | pe_cal p | nc | nc | refclkp | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 19 | vsse | vsse | vsse | vsse | pe_cal n | nc | nc | refclkn | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 18 | perp [3] | pern [3] | petp [3] | petn [3] | vcc1 p8e | vcc1 p2ae | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 17 | perp [2] | pern [2] | petp [2] | petn [2] | vcc1 p8e | vcc1 p2ae | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 16 | vsse | vsse | vsse | vsse | vcc1 p2e | vcc1 p2ae | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 15 | perp [1] | pern [1] | petp [1] | petn [1] | vcc1 p2e | vcc1 p2ae | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 14 | perp [0] | pern [0] | petp [0] | petn [0] | vcc1 p2e | vcc1 p2e | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 13 | vsse | vsse | vsse | vsse | vcc1 p2e | vcc1 p2e | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 12 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 11 | a [22] | a [18] | a [19] | a [21] | pce# [1] | vcc3 p3 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 10 | a [13] | vss | pce# [0] | vss | a [20] | vcc3 p3 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 9 | a [14] | a [8] | a [12] | a [9] | nc | vcc3 p3 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 8 | a [6] | a [1] | pb_rst out# | a [10] | PUR1 | vcc3 p3 | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 |
| 7 | a [2] | vss | a [15] | vss | a [11] | vcc3 p3 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss |
| 6 | a [7] | a [3] | a [17] | a [16] | d [15] | vcc3 p3 | vcc3 p3 | vccv10 | vccv10 | vcc3 p3 | vccv10 | vccv10 | vcc3 p3 | vccv10 | vccv10 | vcc3 p3 | vccv10 | vccv10 | vcc3 p3 |
| 5 | a [5] | a [4] | d [4] | d [9] | vcc3 p3 | d [10] | p_ad [32] | vccv10 | p_ad [40] | p_ad [44] | vccv10 | p_ad [52] | p_ad [56] | vccv10 | p_ad [64] | p_cbe# [7] | vccv10 | p_ad [4] | p_ad [9] |
| 4 | d [1] | d [8] | d [3] | vss | d [2] | poer# | vss | p_ad [36] | p_ad [42] | vss | p_ad [48] | p_ad [54] | vss | p_ad [60] | p_cbe# [5] | vss | p_ad [0] | p_ad [6] | vss |
| 3 | vss | d [0] | a [23] | d [11] | d [12] | pwe# | p_ad [34] | p_ad [38] | p_ad [39] | p_ad [46] | p_ad [50] | p_ad [51] | p_ad [58] | p_ad [62] | p_ad [63] | p_req# [4] | p_ad [2] | p_ad [5] | p_cbe# [0] |
| 2 | | vss | a [0] | d [5] | d [6] | d [14] | vss | p_ad [35] | p_ad [41] | vss | p_ad [47] | p_ad [53] | vss | p_ad [59] | p_cbe# [4] | vss | p_ad [1] | p_ad [7] | vss |
| 1 | | | vss | d [13] | d [7] | a [24] | p_ad [33] | p_ad [37] | p_ad [43] | p_ad [45] | p_ad [49] | p_ad [55] | p_ad [57] | p_ad [61] | p_cbe# [6] | p_ack# [4] | p_ad [3] | p_ad [8] | vss |



Figure 6. Intel® 81348 I/O processor Ballout—Package Bottom (Right Side)

| V | U | T | R | P | N | M | L | K | J | H | G | F | E | D | C | B | A | |
|-----------|------------|----------|------------|-------------|-----------|-----------|------------|--------------|--------------|------------|------------|-----------------|-----------------|-------------|------------|------------|-----------|----|
| cb [6] | cb [2] | dq [44] | dq [40] | dq [41] | dqs# [5] | dqs [5] | dq [47] | dq [43] | dq [60] | dq [56] | dq [57] | dqs# [7] | dqs [7] | dq [63] | vss | | | 37 |
| cb [7] | cb [3] | vss | dq [45] | dm [5] | vss | dq [46] | dq [42] | vss | vss | dq [61] | dm [7] | vss | dq [62] | dq [58] | dq [59] | vss | | 36 |
| vss | m_ck# [2] | dq [36] | dq [37] | dm [4] | dqs# [4] | dqs [4] | dq [34] | dq [35] | dq [53] | dm [6] | dqs# [6] | dqs [6] | dq [50] | dq [51] | nc | vss | | 35 |
| m_ck# [0] | m_ck [2] | vss | dq [32] | dq [33] | vss | dq [38] | dq [39] | vss | vss | dq [48] | dq [49] | vss | dq [54] | dq [55] | vss | nc | nc | 34 |
| ma [0] | ba [1] | ma [10] | ba [0] | ras# | cs# [0] | vss | we# | cas# | odt [0] | ma [13] | cs# [1] | odt [1] | vss | nc | ma [14]a | nc | nc | 33 |
| vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc1 p8 | vcc3 p3 | vcc3 p3 | nc | nc | nc | nc | nc | 32 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc3 p3 | nc | nc | nc | nc | nc | nc | 31 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc3 p3 | nc | nc | vss | nc | vss | nc | 30 |
| thermda | vssplix | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc3 p3 | nc | nc | nc | nc | nc | nc | 29 |
| thermdc | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc3 p3 | nc | nc | nc | nc | nc | nc | 28 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc3 p3 | s_stat3 | s_act4 | vss | s_stat5 | vss | s_act1 | 27 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc3 p3 | s_stat4 | s_stat6 | s_stat7 | s_act0 | s_stat2 | s_act5 | 26 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vcc3 p3 | s_act6 | s_stat1 | s_act7 | s_act3 | s_act2 | s_stat0 | 25 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2 | vcc1 p2as | vcc1 p2as | vssas | vssas | vssas | vssas | | | 24 |
| vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2 | vcc1 p2as | vcc1 p2as | s_txn [3] | s_tbp [3] | s_rxn [3] | s_rxp [3] | | 23 |
| vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2x | vss | vcc1 p2 | vcc1 p2as | vcc1 p2as | vcc1 p2as | s_txn [1] | s_tbp [1] | s_rxn [1] | s_rxp [1] | | 22 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vssplls0 | s_clkp | nc | nc | rbias_sense [0] | vssas | vssas | vssas | vssas | 21 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2plls0 | s_ckn | nc | nc | rbias [0] | s_txn [0] | s_tbp [0] | s_rxn [0] | s_rxp [0] | 20 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc1 p8s | vcc1 p8s | vcc1 p8s | s_txn [2] | s_tbp [2] | s_rxn [2] | s_rxp [2] | 19 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p8s | vcc1 p8s | vcc1 p8s | vssas | vssas | vssas | vssas | 18 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vssds | vssds | vcc1 p2ds | vcc1 p2ds | s_txn [7] | s_tbp [7] | s_rxn [7] | s_rxp [7] | | 17 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vssplls1 | vss | nc | nc | rbias_sense [1] | s_txn [5] | s_tbp [5] | s_rxn [5] | s_rxp [5] | | 16 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2plls1 | vss | nc | nc | rbias [1] | vssas | vssas | vssas | vssas | | 15 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vssds | vcc1 p2ds | vssds | s_txn [4] | s_tbp [4] | s_rxn [4] | s_rxp [4] | | 14 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc1 p2ds | vssds | vcc1 p2ds | s_txn [6] | s_tbp [6] | s_rxn [6] | s_rxp [6] | 13 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc1 p2ds | vcc1 p2ds | vssds | vssas | vssas | vssas | vssas | | 12 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2pllp | vsspllp | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc3 p3 | gpio [6] | gpio [5] | gpio [7] | gpio [3] | gpio [1] | | 11 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc3 p3 | gpio [4] | vss | gpio [2] | vss | gpio [0] | 10 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc3 p3 | xint# [7] | xint# [4] | xint# [5] | xint# [3] | xint# [1] | 9 |
| vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vcc3 p3 | hs_led_out | nmio# | xin# [6] | xint# [0] | xint# [2] | 8 |
| vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc1 p2 | vss | vcc3 p3 | nmi# | vss | hpi# | vss | hs_enum# | 7 |
| vcc3 p3 | vccvlio | vcc3 p3 | vcc3 p3 | vccvlio | vcc3 p3 | vccvlio | vcc3 p3 | vcc3 p3 | vcc3 p3 | vccvlio | vcc3 p3 | vcc3 p3 | hs_freq [0] | hs_freq [1] | hs_istat | u0_rxd | u0_rts# | 6 |
| p_ad [13] | vccvlio | p_irdy# | p_ad [16] | vccvlio | p_idsel | p_ad [26] | vccvlio | p_ad [31] | p_gnt# [0] | vccvlio | p_gnt# [3] | vcc3 p3 | vcc3 p3 | nc | u1_rxd | u0_txd | u0_cts# | 5 |
| p_ad [11] | p_par | vss | p_frame# | p_ad [20] | vss | p_ad [24] | p_ad [30] | vss | p_gnt# [1] | p_req# [3] | vss | p_bmi | warm_rst# | vss | u1_rts# | u1_txd | u1_cts# | 4 |
| p_ad [12] | p_ad [15] | p_stop# | p_devsel# | p_ad [18] | p_ad [22] | p_ad [23] | p_ad [28] | nc | p_gnt# [2] | p_req# [2] | p_cal [1] | nc | nc | p_cal [2] | p_clk0 [2] | p_clk0 [3] | vss | 3 |
| p_ad [10] | p_cbe# [1] | vss | p_povcca p | p_cbe# [2] | vss | p_ad [21] | p_ad [25] | vss | nc | nc | vss | p_rst# | vss | p_clkout | p_clk0 [0] | | | 2 |
| p_m66en | p_ad [14] | p_serr# | p_perr# | p_irdy# | p_ad [17] | p_ad [19] | p_cbe# [3] | p_ad [29] | p_req# [0] | p_req# [1] | nc | p_rstout# | p_clk0 [1] | p_cikin | vss | | | 1 |

a. MA[14] is only needed for 4GB memory support, otherwise this pin remains NC.

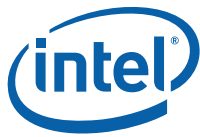


Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 1 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|----------|------|-----------|------|---------------------|------|------------|------|----------------|
| A1 | - | B1 | - | C1 | vss | D1 | p_clkln | E1 | p_clko[1] |
| A2 | - | B2 | vss | C2 | p_clko[0] | D2 | p_clkout | E2 | vss |
| A3 | vss | B3 | p_clko[3] | C3 | p_clko[2] | D3 | p_cal[2] | E3 | nc |
| A4 | u1_cts# | B4 | u1_txd | C4 | u1_rts# | D4 | vss | E4 | warm_rst# |
| A5 | u0_cts# | B5 | u0_txd | C5 | u1_rxd | D5 | nc | E5 | vcc3p3 |
| A6 | u0_rts# | B6 | u0_rxd | C6 | hs_lstat | D6 | hs_freq[1] | E6 | hs_freq[0] |
| A7 | hs_enum# | B7 | vss | C7 | hpi# | D7 | vss | E7 | nmi1# |
| A8 | xint#[2] | B8 | xint#[0] | C8 | xint#[6] | D8 | nmi0# | E8 | hs_led_out |
| A9 | xint#[1] | B9 | xint#[3] | C9 | xint#[5] | D9 | xint#[4] | E9 | xint#[7] |
| A10 | gpio[0] | B10 | vss | C10 | gpio[2] | D10 | vss | E10 | gpio[4] |
| A11 | gpio[1] | B11 | gpio[3] | C11 | gpio[7] | D11 | gpio[5] | E11 | gpio[6] |
| A12 | vssas | B12 | vssas | C12 | vssas | D12 | vssas | E12 | vssds |
| A13 | s_rxp[6] | B13 | s_rxn[6] | C13 | s_txp[6] | D13 | s_txn[6] | E13 | vcc1p2ds |
| A14 | s_rxp[4] | B14 | s_rxn[4] | C14 | s_txp[4] | D14 | s_txn[4] | E14 | vssds |
| A15 | vssas | B15 | vssas | C15 | vssas | D15 | vssas | E15 | rbias[1] |
| A16 | s_rxp[5] | B16 | s_rxn[5] | C16 | s_txp[5] | D16 | s_txn[5] | E16 | rbias_sense[1] |
| A17 | s_rxp[7] | B17 | s_rxn[7] | C17 | s_txp[7] | D17 | s_txn[7] | E17 | vcc1p2ds |
| A18 | vssas | B18 | vssas | C18 | vssas | D18 | vssas | E18 | vcc1p8s |
| A19 | s_rxp[2] | B19 | s_rxn[2] | C19 | s_txp[2] | D19 | s_txn[2] | E19 | vcc1p8s |
| A20 | s_rxp[0] | B20 | s_rxn[0] | C20 | s_txp[0] | D20 | s_txn[0] | E20 | rbias[0] |
| A21 | vssas | B21 | vssas | C21 | vssas | D21 | vssas | E21 | rbias_sense[0] |
| A22 | s_rxp[1] | B22 | s_rxn[1] | C22 | s_txp[1] | D22 | s_txn[1] | E22 | vcc1p2as |
| A23 | s_rxp[3] | B23 | s_rxn[3] | C23 | s_txp[3] | D23 | s_txn[3] | E23 | vcc1p2as |
| A24 | vssas | B24 | vssas | C24 | vssas | D24 | vssas | E24 | vcc1p2as |
| A25 | s_stat0 | B25 | s_act2 | C25 | s_act3 | D25 | s_act7 | E25 | s_stat1 |
| A26 | s_act5 | B26 | s_stat2 | C26 | s_act0 | D26 | s_stat7 | E26 | s_stat6 |
| A27 | s_act1 | B27 | vss | C27 | s_stat5 | D27 | vss | E27 | s_act4 |
| A28 | nc | B28 | nc | C28 | nc | D28 | nc | E28 | nc |
| A29 | nc | B29 | nc | C29 | nc | D29 | nc | E29 | nc |
| A30 | nc | B30 | vss | C30 | nc | D30 | vss | E30 | nc |
| A31 | nc | B31 | nc | C31 | nc | D31 | nc | E31 | nc |
| A32 | nc | B32 | nc | C32 | nc | D32 | nc | E32 | nc |
| A33 | nc | B33 | nc | C33 | ma[14] ^a | D33 | nc | E33 | vss |
| A34 | nc | B34 | nc | C34 | vss | D34 | dq[55] | E34 | dq[54] |
| A35 | vss | B35 | nc | C35 | dq[51] | D35 | dq[50] | E35 | dqs[6] |
| A36 | - | B36 | vss | C36 | dq[59] | D36 | dq[58] | E36 | dq[62] |
| A37 | - | B37 | - | C37 | vss | D37 | dq[63] | E37 | dqs[7] |



Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 2 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|-----------|------|-----------|------|-----------|------|------------|------|-----------|
| F1 | p_rstout# | G2 | vss | H3 | p_gnt#[2] | J4 | p_gnt#[1] | K5 | p_ad[31] |
| F2 | p_rst# | G3 | p_req#[2] | H4 | p_req#[3] | J5 | p_gnt#[0] | K6 | vcc3p3 |
| F3 | p_cal[1] | G4 | vss | H5 | vccvio | J6 | vcc3p3 | K7 | vcc1p2 |
| F4 | p_bmi | G5 | p_gnt#[3] | H6 | vccvio | J7 | vss | K8 | vss |
| F5 | p_cal[0] | G6 | vcc3p3 | H7 | vcc1p2 | J8 | vcc1p2 | K9 | vcc1p2 |
| F6 | vcc3p3 | G7 | vss | H8 | vss | J9 | vss | K10 | vss |
| F7 | vcc3p3 | G8 | vcc1p2 | H9 | vcc1p2 | J10 | vcc1p2 | K11 | vcc1p2 |
| F8 | vcc3p3 | G9 | vss | H10 | vss | J11 | vss | K12 | vss |
| F9 | vcc3p3 | G10 | vcc1p2 | H11 | vcc1p2 | J12 | vcc1p2 | K13 | vcc1p2 |
| F10 | vcc3p3 | G11 | vss | H12 | vss | J13 | vss | K14 | vss |
| F11 | vcc3p3 | G12 | vcc1p2ds | H13 | vcc1p2 | J14 | vcc1p2 | K15 | vcc1p2 |
| F12 | vcc1p2ds | G13 | vcc1p2ds | H14 | vss | J15 | vcc1p2p1s1 | K16 | vss |
| F13 | vssds | G14 | vssds | H15 | vss | J16 | vssp1s1 | K17 | vcc1p2 |
| F14 | vcc1p2ds | G15 | nc | H16 | vss | J17 | vss | K18 | vss |
| F15 | nc | G16 | nc | H17 | vcc1p2 | J18 | vcc1p2 | K19 | vcc1p2 |
| F16 | nc | G17 | vssds | H18 | vss | J19 | vss | K20 | vss |
| F17 | vssds | G18 | vcc1p8s | H19 | vcc1p2 | J20 | vcc1p2p1s0 | K21 | vcc1p2 |
| F18 | vcc1p8s | G19 | vcc1p8s | H20 | s_clkn0 | J21 | vssp1s0 | K22 | vss |
| F19 | vcc1p8s | G20 | nc | H21 | s_clkp0 | J22 | vcc1p2 | K23 | vcc1p2x |
| F20 | nc | G21 | nc | H22 | vss | J23 | vss | K24 | vss |
| F21 | nc | G22 | vcc1p2as | H23 | vcc1p2 | J24 | vcc1p2 | K25 | vcc1p2x |
| F22 | vcc1p2as | G23 | vcc1p2as | H24 | vss | J25 | vss | K26 | vss |
| F23 | vcc1p2as | G24 | vcc1p2as | H25 | vcc1p2x | J26 | vcc1p2x | K27 | vcc1p2x |
| F24 | vcc1p2as | G25 | vcc3p3 | H26 | vss | J27 | vss | K28 | vss |
| F25 | s_act6 | G26 | vcc3p3 | H27 | vcc1p2x | J28 | vcc1p2x | K29 | vcc1p2x |
| F26 | s_stat4 | G27 | vcc3p3 | H28 | vss | J29 | vss | K30 | vss |
| F27 | s_stat3 | G28 | vcc3p3 | H29 | vcc1p2x | J30 | vcc1p2x | K31 | vcc1p2x |
| F28 | nc | G29 | vcc3p3 | H30 | vss | J31 | vss | K32 | vcc1p8 |
| F29 | nc | G30 | vcc3p3 | H31 | vcc1p2x | J32 | vcc1p8 | K33 | cas# |
| F30 | nc | G31 | vcc3p3 | H32 | vcc1p8 | J33 | odt[0] | K34 | vss |
| F31 | nc | G32 | vcc3p3 | H33 | ma[13] | J34 | vss | K35 | dq[35] |
| F32 | vcc3p3 | G33 | cs#[1] | H34 | dq[48] | J35 | dq[52] | K36 | vss |
| F33 | odt[1] | G34 | dq[49] | H35 | dq[53] | J36 | vss | K37 | dq[43] |
| F34 | vss | G35 | dm[6] | H36 | dq[61] | J37 | dq[60] | L1 | p_cbe#[3] |
| F35 | dqs#[6] | G36 | dm[7] | H37 | dq[56] | K1 | p_ad[29] | L2 | p_ad[25] |
| F36 | vss | G37 | dq[57] | J1 | p_req#[0] | K2 | vss | L3 | p_ad[28] |
| F37 | dqs#[7] | H1 | p_req#[1] | J2 | nc | K3 | p_ad[27] | L4 | p_ad[30] |
| G1 | nc | H2 | nc | J3 | nc | K4 | vss | L5 | vccvio |



Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 3 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|----------|------|----------|------|-----------|------|-----------|------|---------|
| L6 | vccvio | M7 | vcc1p2 | N8 | vcc1p2 | P9 | vcc1p2 | R10 | vcc1p2 |
| L7 | vss | M8 | vss | N9 | vss | P10 | vss | R11 | vss |
| L8 | vcc1p2 | M9 | vcc1p2 | N10 | vcc1p2 | P11 | vcc1p2pll | R12 | vcc1p2 |
| L9 | vss | M10 | vss | N11 | vsspll | P12 | vss | R13 | vss |
| L10 | vcc1p2 | M11 | vcc1p2 | N12 | vcc1p2 | P13 | vcc1p2 | R14 | vcc1p2 |
| L11 | vss | M12 | vss | N13 | vss | P14 | vss | R15 | vss |
| L12 | vcc1p2 | M13 | vcc1p2 | N14 | vcc1p2 | P15 | vcc1p2 | R16 | vcc1p2 |
| L13 | vss | M14 | vss | N15 | vss | P16 | vss | R17 | vss |
| L14 | vcc1p2 | M15 | vcc1p2 | N16 | vcc1p2 | P17 | vcc1p2 | R18 | vcc1p2 |
| L15 | vss | M16 | vss | N17 | vss | P18 | vss | R19 | vss |
| L16 | vcc1p2 | M17 | vcc1p2 | N18 | vcc1p2 | P19 | vcc1p2 | R20 | vcc1p2 |
| L17 | vss | M18 | vss | N19 | vss | P20 | vss | R21 | vss |
| L18 | vcc1p2 | M19 | vcc1p2 | N20 | vcc1p2 | P21 | vcc1p2 | R22 | vcc1p2x |
| L19 | vss | M20 | vss | N21 | vss | P22 | vss | R23 | vss |
| L20 | vcc1p2 | M21 | vcc1p2 | N22 | vcc1p2x | P23 | vcc1p2x | R24 | vcc1p2x |
| L21 | vss | M22 | vss | N23 | vss | P24 | vss | R25 | vss |
| L22 | vcc1p2x | M23 | vcc1p2x | N24 | vcc1p2x | P25 | vcc1p2x | R26 | vcc1p2x |
| L23 | vss | M24 | vss | N25 | vss | P26 | vss | R27 | vss |
| L24 | vcc1p2x | M25 | vcc1p2x | N26 | vcc1p2x | P27 | vcc1p2x | R28 | vcc1p2x |
| L25 | vss | M26 | vss | N27 | vss | P28 | vss | R29 | vss |
| L26 | vcc1p2x | M27 | vcc1p2x | N28 | vcc1p2x | P29 | vcc1p2x | R30 | vcc1p2x |
| L27 | vss | M28 | vss | N29 | vss | P30 | vss | R31 | vss |
| L28 | vcc1p2x | M29 | vcc1p2x | N30 | vcc1p2x | P31 | vcc1p2x | R32 | vcc1p8 |
| L29 | vss | M30 | vss | N31 | vss | P32 | vcc1p8 | R33 | ba[0] |
| L30 | vcc1p2x | M31 | vcc1p2x | N32 | vcc1p8 | P33 | ras# | R34 | dq[32] |
| L31 | vss | M32 | vcc1p8 | N33 | cs#[0] | P34 | dq[33] | R35 | dq[37] |
| L32 | vcc1p8 | M33 | vss | N34 | vss | P35 | dm[4] | R36 | dq[45] |
| L33 | we# | M34 | dq[38] | N35 | dqs#[4] | P36 | dm[5] | R37 | dq[40] |
| L34 | dq[39] | M35 | dqs[4] | N36 | vss | P37 | dq[41] | T1 | p_serr# |
| L35 | dq[34] | M36 | dq[46] | N37 | dqs#[5] | R1 | p_perr# | T2 | vss |
| L36 | dq[42] | M37 | dqs[5] | P1 | p_irdy# | R2 | p_pcixcap | T3 | p_stop# |
| L37 | dq[47] | N1 | p_ad[17] | P2 | p_cbe#[2] | R3 | p_devsel# | T4 | vss |
| M1 | p_ad[19] | N2 | vss | P3 | p_ad[18] | R4 | p_frame# | T5 | p_trdy# |
| M2 | p_ad[21] | N3 | p_ad[22] | P4 | p_ad[20] | R5 | p_ad[16] | T6 | vcc3p3 |
| M3 | p_ad[23] | N4 | vss | P5 | vccvio | R6 | vcc3p3 | T7 | vcc1p2 |
| M4 | p_ad[24] | N5 | p_idsel | P6 | vccvio | R7 | vss | T8 | vss |
| M5 | p_ad[26] | N6 | vcc3p3 | P7 | vcc1p2 | R8 | vcc1p2 | T9 | vcc1p2 |
| M6 | vccvio | N7 | vss | P8 | vss | R9 | vss | T10 | vss |



Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 4 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|-----------|------|----------|------|-----------|------|---------|------|-----------|
| T11 | vcc1p2 | U12 | vcc1p2 | V13 | vcc1p2 | W14 | vcc1p2 | Y15 | vcc1p2 |
| T12 | vss | U13 | vss | V14 | vss | W15 | vss | Y16 | vss |
| T13 | vcc1p2 | U14 | vcc1p2 | V15 | vcc1p2 | W16 | vcc1p2 | Y17 | vcc1p2 |
| T14 | vss | U15 | vss | V16 | vss | W17 | vss | Y18 | vss |
| T15 | vcc1p2 | U16 | vcc1p2 | V17 | vcc1p2 | W18 | vcc1p2 | Y19 | vcc1p2 |
| T16 | vss | U17 | vss | V18 | vss | W19 | vss | Y20 | vss |
| T17 | vcc1p2 | U18 | vcc1p2 | V19 | vcc1p2 | W20 | vcc1p2 | Y21 | vcc1p2 |
| T18 | vss | U19 | vss | V20 | vss | W21 | vss | Y22 | vss |
| T19 | vcc1p2 | U20 | vcc1p2 | V21 | vcc1p2 | W22 | vcc1p2x | Y23 | vcc1p2x |
| T20 | vss | U21 | vss | V22 | vss | W23 | vss | Y24 | vss |
| T21 | vcc1p2 | U22 | vcc1p2x | V23 | vcc1p2x | W24 | vcc1p2x | Y25 | vcc1p2x |
| T22 | vss | U23 | vss | V24 | vss | W25 | vss | Y26 | vss |
| T23 | vcc1p2x | U24 | vcc1p2x | V25 | vcc1p2x | W26 | vcc1p2x | Y27 | vcc1p2x |
| T24 | vss | U25 | vss | V26 | vss | W27 | vss | Y28 | vss |
| T25 | vcc1p2x | U26 | vcc1p2x | V27 | vcc1p2x | W28 | vcc1p2x | Y29 | vcc3p3plx |
| T26 | vss | U27 | vss | V28 | thermdc | W29 | nc | Y30 | vss |
| T27 | vcc1p2x | U28 | vcc1p2x | V29 | thermda | W30 | vcc1p2x | Y31 | vcc1p2x |
| T28 | vss | U29 | vssplx | V30 | vss | W31 | vss | Y32 | vcc1p8 |
| T29 | vcc1p2x | U30 | vcc1p2x | V31 | vcc1p2x | W32 | vcc1p8 | Y33 | ma[1] |
| T30 | vss | U31 | vss | V32 | vcc1p8 | W33 | vss | Y34 | ma[2] |
| T31 | vcc1p2x | U32 | vcc1p8 | V33 | ma[0] | W34 | m_ck[0] | Y35 | vss |
| T32 | vcc1p8 | U33 | ba[1] | V34 | m_ck#[0] | W35 | dm[8] | Y36 | cb[5] |
| T33 | ma[10] | U34 | m_ck[2] | V35 | vss | W36 | dqs[8] | Y37 | cb[1] |
| T34 | vss | U35 | m_ck#[2] | V36 | cb[7] | W37 | dqs#[8] | AA1 | p_ad[3] |
| T35 | dq[36] | U36 | cb[3] | V37 | cb[6] | Y1 | p_ad[8] | AA2 | p_ad[1] |
| T36 | vss | U37 | cb[2] | W1 | vss | Y2 | p_ad[7] | AA3 | p_ad[2] |
| T37 | dq[44] | V1 | p_m66en | W2 | vss | Y3 | p_ad[5] | AA4 | p_ad[0] |
| U1 | p_ad[14] | V2 | p_ad[10] | W3 | p_cbe#[0] | Y4 | p_ad[6] | AA5 | vccvio |
| U2 | p_cbe#[1] | V3 | p_ad[12] | W4 | vss | Y5 | p_ad[4] | AA6 | vccvio |
| U3 | p_ad[15] | V4 | p_ad[11] | W5 | p_ad[9] | Y6 | vccvio | AA7 | vss |
| U4 | p_par | V5 | p_ad[13] | W6 | vcc3p3 | Y7 | vcc1p2 | AA8 | vcc1p2 |
| U5 | vccvio | V6 | vcc3p3 | W7 | vss | Y8 | vss | AA9 | vss |
| U6 | vccvio | V7 | vcc1p2 | W8 | vcc1p2 | Y9 | vcc1p2 | AA10 | vcc1p2 |
| U7 | vss | V8 | vss | W9 | vss | Y10 | vss | AA11 | vss |
| U8 | vcc1p2 | V9 | vcc1p2 | W10 | vcc1p2 | Y11 | vcc1p2 | AA12 | vcc1p2 |
| U9 | vss | V10 | vss | W11 | vss | Y12 | vss | AA13 | vss |
| U10 | vcc1p2 | V11 | vcc1p2 | W12 | vcc1p2 | Y13 | vcc1p2 | AA14 | vcc1p2 |
| U11 | vss | V12 | vss | W13 | vss | Y14 | vss | AA15 | vss |



Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 5 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|-----------|------|-----------|------|----------|------|------------|------|----------|
| AA16 | vcc1p2 | AB17 | vcc1p2 | AC18 | vcc1p2 | AD19 | vcc1p2 | AE20 | vcc1p2 |
| AA17 | vss | AB18 | vss | AC19 | vss | AD20 | vss | AE21 | vss |
| AA18 | vcc1p2 | AB19 | vcc1p2 | AC20 | vcc1p2 | AD21 | vcc1p2 | AE22 | vcc1p2x |
| AA19 | vss | AB20 | vss | AC21 | vss | AD22 | vss | AE23 | vss |
| AA20 | vcc1p2 | AB21 | vcc1p2 | AC22 | vcc1p2x | AD23 | vcc1p2x | AE24 | vcc1p2x |
| AA21 | vss | AB22 | vss | AC23 | vss | AD24 | vss | AE25 | vss |
| AA22 | vcc1p2x | AB23 | vcc1p2x | AC24 | vcc1p2x | AD25 | vcc1p2x | AE26 | vcc1p2x |
| AA23 | vss | AB24 | vss | AC25 | vss | AD26 | vss | AE27 | vss |
| AA24 | vcc1p2x | AB25 | vcc1p2x | AC26 | vcc1p2x | AD27 | vcc1p2x | AE28 | vcc1p2x |
| AA25 | vss | AB26 | vss | AC27 | vss | AD28 | vss | AE29 | vss |
| AA26 | vcc1p2x | AB27 | vcc1p2x | AC28 | vcc1p2x | AD29 | vcc1p2plld | AE30 | vcc1p2x |
| AA27 | vss | AB28 | vss | AC29 | vssplld | AD30 | vss | AE31 | vss |
| AA28 | vcc1p2x | AB29 | vcc1p2x | AC30 | vcc1p2x | AD31 | vcc1p2x | AE32 | vcc1p8 |
| AA29 | vss | AB30 | vss | AC31 | vss | AD32 | vcc1p8 | AE33 | ma[5] |
| AA30 | vcc1p2x | AB31 | vcc1p2x | AC32 | vcc1p8 | AD33 | vss | AE34 | vss |
| AA31 | vss | AB32 | vcc1p8 | AC33 | ma[6] | AD34 | dq[22] | AE35 | dqs#[2] |
| AA32 | vcc1p8 | AB33 | ma[4] | AC34 | dq[23] | AD35 | dqs[2] | AE36 | vss |
| AA33 | ma[3] | AB34 | vss | AC35 | dq[18] | AD36 | dq[30] | AE37 | dqs#[3] |
| AA34 | m_ck#[1] | AB35 | dq[19] | AC36 | dq[26] | AD37 | dqs[3] | AF1 | p_ad[55] |
| AA35 | m_ck[1] | AB36 | vss | AC37 | dq[31] | AE1 | p_ad[57] | AF2 | p_ad[53] |
| AA36 | cb[4] | AB37 | dq[27] | AD1 | p_ad[61] | AE2 | vss | AF3 | p_ad[51] |
| AA37 | cb[0] | AC1 | p_cbe#[6] | AD2 | p_ad[59] | AE3 | p_ad[58] | AF4 | p_ad[54] |
| AB1 | p_ack64# | AC2 | p_cbe#[4] | AD3 | p_ad[62] | AE4 | vss | AF5 | p_ad[52] |
| AB2 | vss | AC3 | p_ad[63] | AD4 | p_ad[60] | AE5 | p_ad[56] | AF6 | vccvio |
| AB3 | p_req64# | AC4 | p_cbe#[5] | AD5 | vccvio | AE6 | vcc3p3 | AF7 | vcc1p2 |
| AB4 | vss | AC5 | p_par64 | AD6 | vccvio | AE7 | vss | AF8 | vss |
| AB5 | p_cbe#[7] | AC6 | vccvio | AD7 | vcc1p2 | AE8 | vcc1p2 | AF9 | vcc1p2 |
| AB6 | vcc3p3 | AC7 | vss | AD8 | vss | AE9 | vss | AF10 | vss |
| AB7 | vcc1p2 | AC8 | vcc1p2 | AD9 | vcc1p2 | AE10 | vcc1p2 | AF11 | vcc1p2 |
| AB8 | vss | AC9 | vss | AD10 | vss | AE11 | vss | AF12 | vss |
| AB9 | vcc1p2 | AC10 | vcc1p2 | AD11 | vcc1p2 | AE12 | vcc1p2 | AF13 | vcc1p2 |
| AB10 | vss | AC11 | vss | AD12 | vss | AE13 | vss | AF14 | vss |
| AB11 | vcc1p2 | AC12 | vcc1p2 | AD13 | vcc1p2 | AE14 | vcc1p2 | AF15 | vcc1p2 |
| AB12 | vss | AC13 | vss | AD14 | vss | AE15 | vss | AF16 | vss |
| AB13 | vcc1p2 | AC14 | vcc1p2 | AD15 | vcc1p2 | AE16 | vcc1p2 | AF17 | vcc1p2 |
| AB14 | vss | AC15 | vss | AD16 | vss | AE17 | vss | AF18 | vss |
| AB15 | vcc1p2 | AC16 | vcc1p2 | AD17 | vcc1p2 | AE18 | vcc1p2 | AF19 | vcc1p2 |
| AB16 | vss | AC17 | vss | AD18 | vss | AE19 | vss | AF20 | vss |

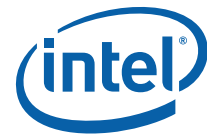


Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 6 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|----------|------|----------|------|----------|------|----------|------|----------|
| AF21 | vcc1p2 | AG22 | vcc1p2x | AH23 | vcc1p2x | AJ24 | vcc1p2x | AK25 | vcc1p2x |
| AF22 | vss | AG23 | vss | AH24 | vss | AJ25 | vss | AK26 | vss |
| AF23 | vcc1p2x | AG24 | vcc1p2x | AH25 | vcc1p2x | AJ26 | vcc1p2x | AK27 | vcc1p2x |
| AF24 | vss | AG25 | vss | AH26 | vss | AJ27 | vcc1p2x | AK28 | vss |
| AF25 | vcc1p2x | AG26 | vcc1p2x | AH27 | vcc1p2x | AJ28 | vcc1p2x | AK29 | vcc1p2x |
| AF26 | vss | AG27 | vss | AH28 | vss | AJ29 | vss | AK30 | vss |
| AF27 | vcc1p2x | AG28 | vcc1p2x | AH29 | vcc1p2x | AJ30 | vcc1p2x | AK31 | vcc1p2x |
| AF28 | vss | AG29 | vss | AH30 | vss | AJ31 | vss | AK32 | vcc1p8 |
| AF29 | vcc1p2x | AG30 | vcc1p2x | AH31 | vcc1p2x | AJ32 | vcc1p8 | AK33 | ma[12] |
| AF30 | vss | AG31 | vss | AH32 | vcc1p8 | AJ33 | ma[11] | AK34 | dq[7] |
| AF31 | vcc1p2x | AG32 | vcc1p8 | AH33 | ma[9] | AJ34 | vss | AK35 | dq[2] |
| AF32 | vcc1p8 | AG33 | ma[7] | AH34 | vss | AJ35 | dq[3] | AK36 | dq[10] |
| AF33 | ma[8] | AG34 | dq[16] | AH35 | dq[20] | AJ36 | vss | AK37 | dq[15] |
| AF34 | dq[17] | AG35 | dq[21] | AH36 | vss | AJ37 | dq[11] | AL1 | p_ad[33] |
| AF35 | dm[2] | AG36 | dq[29] | AH37 | dq[28] | AK1 | p_ad[37] | AL2 | vss |
| AF36 | dm[3] | AG37 | dq[24] | AJ1 | p_ad[43] | AK2 | p_ad[35] | AL3 | p_ad[34] |
| AF37 | dq[25] | AH1 | p_ad[45] | AJ2 | p_ad[41] | AK3 | p_ad[38] | AL4 | vss |
| AG1 | p_ad[49] | AH2 | vss | AJ3 | p_ad[39] | AK4 | p_ad[36] | AL5 | p_ad[32] |
| AG2 | p_ad[47] | AH3 | p_ad[46] | AJ4 | p_ad[42] | AK5 | vccvio | AL6 | vcc3p3 |
| AG3 | p_ad[50] | AH4 | vss | AJ5 | p_ad[40] | AK6 | vccvio | AL7 | vss |
| AG4 | p_ad[48] | AH5 | p_ad[44] | AJ6 | vccvio | AK7 | vcc1p2 | AL8 | vcc1p2 |
| AG5 | vccvio | AH6 | vcc3p3 | AJ7 | vss | AK8 | vss | AL9 | vss |
| AG6 | vccvio | AH7 | vcc1p2 | AJ8 | vcc1p2 | AK9 | vcc1p2 | AL10 | vcc1p2 |
| AG7 | vss | AH8 | vss | AJ9 | vss | AK10 | vss | AL11 | vss |
| AG8 | vcc1p2 | AH9 | vcc1p2 | AJ10 | vcc1p2 | AK11 | vcc1p2 | AL12 | vcc1p2 |
| AG9 | vss | AH10 | vss | AJ11 | vss | AK12 | vss | AL13 | vss |
| AG10 | vcc1p2 | AH11 | vcc1p2 | AJ12 | vcc1p2 | AK13 | vcc1p2 | AL14 | vcc1p2 |
| AG11 | vss | AH12 | vss | AJ13 | vss | AK14 | vss | AL15 | vss |
| AG12 | vcc1p2 | AH13 | vcc1p2 | AJ14 | vcc1p2 | AK15 | vcc1p2 | AL16 | vcc1p2 |
| AG13 | vss | AH14 | vss | AJ15 | vss | AK16 | vss | AL17 | vss |
| AG14 | vcc1p2 | AH15 | vcc1p2 | AJ16 | vcc1p2 | AK17 | vcc1p2 | AL18 | vcc1p2 |
| AG15 | vss | AH16 | vss | AJ17 | vss | AK18 | vss | AL19 | nc |
| AG16 | vcc1p2 | AH17 | vcc1p2 | AJ18 | vcc1p2 | AK19 | refclkp | AL20 | nc |
| AG17 | vss | AH18 | vss | AJ19 | vss | AK20 | refclkp | AL21 | vss |
| AG18 | vcc1p2 | AH19 | vcc1p2 | AJ20 | vcc1p2 | AK21 | vcc1p2 | AL22 | vcc1p2 |
| AG19 | vss | AH20 | vss | AJ21 | vss | AK22 | vss | AL23 | vss |
| AG20 | vcc1p2 | AH21 | vcc1p2 | AJ22 | vcc1p2 | AK23 | vcc1p2 | AL24 | vcc1p2x |
| AG21 | vss | AH22 | vss | AJ23 | vss | AK24 | vss | AL25 | vss |



Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 7 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|----------|------|---------|------|---------|------|------------|------|---------|
| AL26 | vcc1p2x | AM27 | vcc1p2x | AN28 | sci2 | AP29 | sda2 | AR30 | tdo |
| AL27 | vcc1p2x | AM28 | vcc3p3 | AN29 | sci1 | AP30 | vcc3p3 | AR31 | tck |
| AL28 | vcc1p2x | AM29 | vcc3p3 | AN30 | vcc3p3 | AP31 | vss | AR32 | vcc1p8 |
| AL29 | vss | AM30 | vcc3p3 | AN31 | vcc3p3 | AP32 | vcc1p8 | AR33 | m_rst# |
| AL30 | vcc1p2x | AM31 | vcc3p3 | AN32 | vcc1p8 | AP33 | cke[1] | AR34 | vss |
| AL31 | vss | AM32 | vcc1p8 | AN33 | cke[0] | AP34 | dq[0] | AR35 | dq[4] |
| AL32 | vcc1p8 | AM33 | ba[2] | AN34 | dq[1] | AP35 | dq[5] | AR36 | dq[12] |
| AL33 | vss | AM34 | vss | AN35 | dm[0] | AP36 | dq[13] | AR37 | vss |
| AL34 | dq[6] | AM35 | dqs#[0] | AN36 | dq[8] | AP37 | dm[1] | AT1 | - |
| AL35 | dqs[0] | AM36 | vss | AN37 | dq[9] | AR1 | vss | AT2 | vss |
| AL36 | dq[14] | AM37 | dqs#[1] | AP1 | d[13] | AR2 | a[0] | AT3 | d[0] |
| AL37 | dqs[1] | AN1 | d[7] | AP2 | d[5] | AR3 | a[23] | AT4 | d[8] |
| AM1 | a[24] | AN2 | d[6] | AP3 | d[11] | AR4 | d[3] | AT5 | a[4] |
| AM2 | d[14] | AN3 | d[12] | AP4 | vss | AR5 | d[4] | AT6 | a[3] |
| AM3 | pwe# | AN4 | d[2] | AP5 | d[9] | AR6 | a[17] | AT7 | vss |
| AM4 | poe# | AN5 | vcc3p3 | AP6 | a[16] | AR7 | a[15] | AT8 | a[1] |
| AM5 | d[10] | AN6 | d[15] | AP7 | vss | AR8 | pb_rstout# | AT9 | a[8] |
| AM6 | vcc3p3 | AN7 | a[11] | AP8 | a[10] | AR9 | a[12] | AT10 | vss |
| AM7 | vcc3p3 | AN8 | PUR1 | AP9 | a[9] | AR10 | pce#[0] | AT11 | a[18] |
| AM8 | vcc3p3 | AN9 | nc | AP10 | vss | AR11 | a[19] | AT12 | vcc1p2 |
| AM9 | vcc3p3 | AN10 | a[20] | AP11 | a[21] | AR12 | vcc1p2 | AT13 | vsse |
| AM10 | vcc3p3 | AN11 | pce#[1] | AP12 | vcc1p2 | AR13 | vsse | AT14 | pern[0] |
| AM11 | vcc3p3 | AN12 | vcc1p2 | AP13 | vsse | AR14 | petp[0] | AT15 | pern[1] |
| AM12 | vcc1p2 | AN13 | vcc1p2e | AP14 | petn[0] | AR15 | petp[1] | AT16 | vsse |
| AM13 | vcc1p2e | AN14 | vcc1p2e | AP15 | petn[1] | AR16 | vsse | AT17 | pern[2] |
| AM14 | vcc1p2e | AN15 | vcc1p2e | AP16 | vsse | AR17 | petp[2] | AT18 | pern[3] |
| AM15 | vcc1p2ae | AN16 | vcc1p2e | AP17 | petn[2] | AR18 | petp[3] | AT19 | vsse |
| AM16 | vcc1p2ae | AN17 | vcc1p8e | AP18 | petn[3] | AR19 | vsse | AT20 | pern[4] |
| AM17 | vcc1p2ae | AN18 | vcc1p8e | AP19 | vsse | AR20 | petp[4] | AT21 | pern[5] |
| AM18 | vcc1p2ae | AN19 | pe_caln | AP20 | petn[4] | AR21 | petp[5] | AT22 | vsse |
| AM19 | nc | AN20 | pe_calp | AP21 | petn[5] | AR22 | vsse | AT23 | pern[6] |
| AM20 | nc | AN21 | vcc1p8e | AP22 | vsse | AR23 | petp[6] | AT24 | pern[7] |
| AM21 | vcc1p2ae | AN22 | vcc1p8e | AP23 | petn[6] | AR24 | petp[7] | AT25 | vsse |
| AM22 | vcc1p2ae | AN23 | vcc1p8e | AP24 | petn[7] | AR25 | vsse | AT26 | vcc1p8e |
| AM23 | vcc1p2ae | AN24 | vcc1p8e | AP25 | vsse | AR26 | vcc1p8e | AT27 | vcc1p2x |
| AM24 | vcc1p2ae | AN25 | vcc1p8e | AP26 | vcc1p8e | AR27 | vcc1p2x | AT28 | vss |
| AM25 | vcc1p8e | AN26 | vcc1p8e | AP27 | vcc1p2x | AR28 | sda0 | AT29 | sci0 |
| AM26 | vcc1p8e | AN27 | vcc1p2x | AP28 | vss | AR29 | sda1 | AT30 | tms |



Table 15. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Ball Listings (Sheet 8 of 8)

| Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal |
|------|----------|------|--------|------|---------|------|---------|------|--------|
| AT31 | vss | AU3 | vss | AU12 | vcc1p2 | AU21 | perp[5] | AU30 | tdi |
| AT32 | vcc1p8 | AU4 | d[1] | AU13 | vsse | AU22 | vsse | AU31 | trst# |
| AT33 | m_vref | AU5 | a[5] | AU14 | perp[0] | AU23 | perp[6] | AU32 | vcc1p8 |
| AT34 | m_cal[1] | AU6 | a[7] | AU15 | perp[1] | AU24 | perp[7] | AU33 | vss |
| AT35 | m_cal[0] | AU7 | a[2] | AU16 | vsse | AU25 | vsse | AU34 | vss |
| AT36 | vss | AU8 | a[6] | AU17 | perp[2] | AU26 | vcc1p8e | AU35 | vss |
| AT37 | - | AU9 | a[14] | AU18 | perp[3] | AU27 | vcc1p2x | AU36 | - |
| AU1 | - | AU10 | a[13] | AU19 | vsse | AU28 | smbdat | AU37 | - |
| AU2 | - | AU11 | a[22] | AU20 | perp[4] | AU29 | smbclk | | |

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 1 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|--------|------|--------|------|--------|------|---------|------|------------|------|
| - | A1 | ba[0] | R33 | dm[5] | P36 | dq[33] | P34 | dqs#[6] | F35 |
| - | A2 | ba[1] | U33 | dm[6] | G35 | dq[34] | L35 | dqs#[7] | F37 |
| - | A36 | ba[2] | AM33 | dm[7] | G36 | dq[35] | K35 | dqs#[8] | W37 |
| - | A37 | cas# | K33 | dm[8] | W35 | dq[36] | T35 | dqs[0] | AL35 |
| - | B1 | cb[0] | AA37 | dq[0] | AP34 | dq[37] | R35 | dqs[1] | AL37 |
| - | B37 | cb[1] | Y37 | dq[1] | AN34 | dq[38] | M34 | dqs[2] | AD35 |
| - | AT1 | cb[2] | U37 | dq[2] | AK35 | dq[39] | L34 | dqs[3] | AD37 |
| - | AT37 | cb[3] | U36 | dq[3] | AJ35 | dq[40] | R37 | dqs[4] | M35 |
| - | AU1 | cb[4] | AA36 | dq[4] | AR35 | dq[41] | P37 | dqs[5] | M37 |
| - | AU2 | cb[5] | Y36 | dq[5] | AP35 | dq[42] | L36 | dqs[6] | E35 |
| - | AU36 | cb[6] | V37 | dq[6] | AL34 | dq[43] | K37 | dqs[7] | E37 |
| - | AU37 | cb[7] | V36 | dq[7] | AK34 | dq[44] | T37 | dqs[8] | W36 |
| a[0] | AR2 | cke[0] | AN33 | dq[8] | AN36 | dq[45] | R36 | gpio[0] | A10 |
| a[1] | AT8 | cke[1] | AP33 | dq[9] | AN37 | dq[46] | M36 | gpio[1] | A11 |
| a[2] | AU7 | cs#[0] | N33 | dq[10] | AK36 | dq[47] | L37 | gpio[2] | C10 |
| a[3] | AT6 | cs#[1] | G33 | dq[11] | AJ37 | dq[48] | H34 | gpio[3] | B11 |
| a[4] | AT5 | d[0] | AT3 | dq[12] | AR36 | dq[49] | G34 | gpio[4] | E10 |
| a[5] | AU5 | d[1] | AU4 | dq[13] | AP36 | dq[50] | D35 | gpio[5] | D11 |
| a[6] | AU8 | d[2] | AN4 | dq[14] | AL36 | dq[51] | C35 | gpio[6] | E11 |
| a[7] | AU6 | d[3] | AR4 | dq[15] | AK37 | dq[52] | J35 | gpio[7] | C11 |
| a[8] | AT9 | d[4] | AR5 | dq[16] | AG34 | dq[53] | H35 | hpi# | C7 |
| a[9] | AP9 | d[5] | AP2 | dq[17] | AF34 | dq[54] | E34 | hs_enum# | A7 |
| a[10] | AP8 | d[6] | AN2 | dq[18] | AC35 | dq[55] | D34 | hs_freq[0] | E6 |
| a[11] | AN7 | d[7] | AN1 | dq[19] | AB35 | dq[56] | H37 | hs_freq[1] | D6 |
| a[12] | AR9 | d[8] | AT4 | dq[20] | AH35 | dq[57] | G37 | hs_led_out | E8 |
| a[13] | AU10 | d[9] | AP5 | dq[21] | AG35 | dq[58] | D36 | hs_lstat | C6 |
| a[14] | AU9 | d[10] | AM5 | dq[22] | AD34 | dq[59] | C36 | m_cal[0] | AT35 |
| a[15] | AR7 | d[11] | AP3 | dq[23] | AC34 | dq[60] | J37 | m_cal[1] | AT34 |
| a[16] | AP6 | d[12] | AN3 | dq[24] | AG37 | dq[61] | H36 | m_ck#[0] | V34 |
| a[17] | AR6 | d[13] | AP1 | dq[25] | AF37 | dq[62] | E36 | m_ck#[1] | AA34 |
| a[18] | AT11 | d[14] | AM2 | dq[26] | AC36 | dq[63] | D37 | m_ck#[2] | U35 |
| a[19] | AR11 | d[15] | AN6 | dq[27] | AB37 | dqs#[0] | AM35 | m_ck[0] | W34 |
| a[20] | AN10 | dm[0] | AN35 | dq[28] | AH37 | dqs#[1] | AM37 | m_ck[1] | AA35 |
| a[21] | AP11 | dm[1] | AP37 | dq[29] | AG36 | dqs#[2] | AE35 | m_ck[2] | U34 |
| a[22] | AU11 | dm[2] | AF35 | dq[30] | AD36 | dqs#[3] | AE37 | m_rst# | AR33 |
| a[23] | AR3 | dm[3] | AF36 | dq[31] | AC37 | dqs#[4] | N35 | m_vref | AT33 |
| a[24] | AM1 | dm[4] | P35 | dq[32] | R34 | dqs#[5] | N37 | ma[0] | V33 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 2 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|---------------------|------|----------|------|----------|------|-----------|------|------------|------|
| ma[1] | Y33 | nc | D33 | p_ad[4] | Y5 | p_ad[42] | AJ4 | p_clk[3] | B3 |
| ma[2] | Y34 | nc | E3 | p_ad[5] | Y3 | p_ad[43] | AJ1 | p_clkout | D2 |
| ma[3] | AA33 | nc | E28 | p_ad[6] | Y4 | p_ad[44] | AH5 | p_devsel# | R3 |
| ma[4] | AB33 | nc | E29 | p_ad[7] | Y2 | p_ad[45] | AH1 | p_frame# | R4 |
| ma[5] | AE33 | nc | E30 | p_ad[8] | Y1 | p_ad[46] | AH3 | p_gnt#[0] | J5 |
| ma[6] | AC33 | nc | E31 | p_ad[9] | W5 | p_ad[47] | AG2 | p_gnt#[1] | J4 |
| ma[7] | AG33 | nc | E32 | p_ad[10] | V2 | p_ad[48] | AG4 | p_gnt#[2] | H3 |
| ma[8] | AF33 | nc | F15 | p_ad[11] | V4 | p_ad[49] | AG1 | p_gnt#[3] | G5 |
| ma[9] | AH33 | nc | F16 | p_ad[12] | V3 | p_ad[50] | AG3 | p_idsel | N5 |
| ma[10] | T33 | nc | F20 | p_ad[13] | V5 | p_ad[51] | AF3 | p_irdy# | P1 |
| ma[11] | AJ33 | nc | F21 | p_ad[14] | U1 | p_ad[52] | AF5 | p_m66en | V1 |
| ma[12] | AK33 | nc | F28 | p_ad[15] | U3 | p_ad[53] | AF2 | p_par | U4 |
| ma[13] | H33 | nc | F29 | p_ad[16] | R5 | p_ad[54] | AF4 | p_par64 | AC5 |
| nc | A28 | nc | F30 | p_ad[17] | N1 | p_ad[55] | AF1 | p_pciicap | R2 |
| nc | A29 | nc | F31 | p_ad[18] | P3 | p_ad[56] | AE5 | p_perr# | R1 |
| nc | A30 | nc | G1 | p_ad[19] | M1 | p_ad[57] | AE1 | p_req#[0] | J1 |
| nc | A31 | nc | G15 | p_ad[20] | P4 | p_ad[58] | AE3 | p_req#[1] | H1 |
| nc | A32 | nc | G16 | p_ad[21] | M2 | p_ad[59] | AD2 | p_req#[2] | G3 |
| nc | A33 | nc | G20 | p_ad[22] | N3 | p_ad[60] | AD4 | p_req#[3] | H4 |
| nc | A34 | nc | G21 | p_ad[23] | M3 | p_ad[61] | AD1 | p_req64# | AB3 |
| nc | B28 | nc | H2 | p_ad[24] | M4 | p_ad[62] | AD3 | p_rst# | F2 |
| nc | B29 | nc | J2 | p_ad[25] | L2 | p_ad[63] | AC3 | p_rstout# | F1 |
| nc | B31 | nc | J3 | p_ad[26] | M5 | p_bmi | F4 | p_serr# | T1 |
| nc | B32 | nc | W29 | p_ad[27] | K3 | p_cal[0] | F5 | p_stop# | T3 |
| nc | B33 | nc | AL19 | p_ad[28] | L3 | p_cal[1] | F3 | p_trdy# | T5 |
| nc | B34 | nc | AL20 | p_ad[29] | K1 | p_cal[2] | D3 | pb_rstout# | AR8 |
| nc | B35 | nc | AM19 | p_ad[30] | L4 | p_cbe#[0] | W3 | pce#[0] | AR10 |
| nc | C28 | nc | AM20 | p_ad[31] | K5 | p_cbe#[1] | U2 | pce#[1] | AN11 |
| nc | C29 | nc | AN9 | p_ad[32] | AL5 | p_cbe#[2] | P2 | pe_caln | AN19 |
| nc | C30 | nmi0# | D8 | p_ad[33] | AL1 | p_cbe#[3] | L1 | pe_calp | AN20 |
| nc | C31 | nmi1# | E7 | p_ad[34] | AL3 | p_cbe#[4] | AC2 | pern[0] | AT14 |
| nc | C32 | odt[0] | J33 | p_ad[35] | AK2 | p_cbe#[5] | AC4 | pern[1] | AT15 |
| ma[14] ^a | C33 | odt[1] | F33 | p_ad[36] | AK4 | p_cbe#[6] | AC1 | pern[2] | AT17 |
| nc | D5 | p_ack64# | AB1 | p_ad[37] | AK1 | p_cbe#[7] | AB5 | pern[3] | AT18 |
| nc | D28 | p_ad[0] | AA4 | p_ad[38] | AK3 | p_clk[4] | D1 | pern[4] | AT20 |
| nc | D29 | p_ad[1] | AA2 | p_ad[39] | AJ3 | p_clk[0] | C2 | pern[5] | AT21 |
| nc | D31 | p_ad[2] | AA3 | p_ad[40] | AJ5 | p_clk[1] | E1 | pern[6] | AT23 |
| nc | D32 | p_ad[3] | AA1 | p_ad[41] | AJ2 | p_clk[2] | C3 | pern[7] | AT24 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 3 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|----------------|------|----------|------|----------|------|--------|------|--------|------|
| perp[0] | AU14 | s_act5 | A26 | s_txp[1] | C22 | vcc1p2 | H23 | vcc1p2 | P7 |
| perp[1] | AU15 | s_act6 | F25 | s_txp[2] | C19 | vcc1p2 | J8 | vcc1p2 | P9 |
| perp[2] | AU17 | s_act7 | D25 | s_txp[3] | C23 | vcc1p2 | J10 | vcc1p2 | P13 |
| perp[3] | AU18 | s_clkn0 | H20 | s_txp[4] | C14 | vcc1p2 | J12 | vcc1p2 | P15 |
| perp[4] | AU20 | s_clkp0 | H21 | s_txp[5] | C16 | vcc1p2 | J14 | vcc1p2 | P17 |
| perp[5] | AU21 | s_rxn[0] | B20 | s_txp[6] | C13 | vcc1p2 | J18 | vcc1p2 | P19 |
| perp[6] | AU23 | s_rxn[1] | B22 | s_txp[7] | C17 | vcc1p2 | J22 | vcc1p2 | P21 |
| perp[7] | AU24 | s_rxn[2] | B19 | scl0 | AT29 | vcc1p2 | J24 | vcc1p2 | R8 |
| petn[0] | AP14 | s_rxn[3] | B23 | scl1 | AN29 | vcc1p2 | K7 | vcc1p2 | R10 |
| petn[1] | AP15 | s_rxn[4] | B14 | scl2 | AN28 | vcc1p2 | K9 | vcc1p2 | R12 |
| petn[2] | AP17 | s_rxn[5] | B16 | sda0 | AR28 | vcc1p2 | K11 | vcc1p2 | R14 |
| petn[3] | AP18 | s_rxn[6] | B13 | sda1 | AR29 | vcc1p2 | K13 | vcc1p2 | R16 |
| petn[4] | AP20 | s_rxn[7] | B17 | sda2 | AP29 | vcc1p2 | K15 | vcc1p2 | R18 |
| petn[5] | AP21 | s_rxp[0] | A20 | smbclk | AU29 | vcc1p2 | K17 | vcc1p2 | R20 |
| petn[6] | AP23 | s_rxp[1] | A22 | smbdat | AU28 | vcc1p2 | K19 | vcc1p2 | T7 |
| petn[7] | AP24 | s_rxp[2] | A19 | tck | AR31 | vcc1p2 | K21 | vcc1p2 | T9 |
| petp[0] | AR14 | s_rxp[3] | A23 | tdi | AU30 | vcc1p2 | L8 | vcc1p2 | T11 |
| petp[1] | AR15 | s_rxp[4] | A14 | tdo | AR30 | vcc1p2 | L10 | vcc1p2 | T13 |
| petp[2] | AR17 | s_rxp[5] | A16 | thermda | V29 | vcc1p2 | L12 | vcc1p2 | T15 |
| petp[3] | AR18 | s_rxp[6] | A13 | thermdc | V28 | vcc1p2 | L14 | vcc1p2 | T17 |
| petp[4] | AR20 | s_rxp[7] | A17 | tms | AT30 | vcc1p2 | L16 | vcc1p2 | T19 |
| petp[5] | AR21 | s_stat0 | A25 | trst# | AU31 | vcc1p2 | L18 | vcc1p2 | T21 |
| petp[6] | AR23 | s_stat1 | E25 | u0_cts# | A5 | vcc1p2 | L20 | vcc1p2 | U8 |
| petp[7] | AR24 | s_stat2 | B26 | u0_rts# | A6 | vcc1p2 | M7 | vcc1p2 | U10 |
| poe# | AM4 | s_stat3 | F27 | u0_rxd | B6 | vcc1p2 | M9 | vcc1p2 | U12 |
| pwe# | AM3 | s_stat4 | F26 | u0_txd | B5 | vcc1p2 | M11 | vcc1p2 | U14 |
| ras# | P33 | s_stat5 | C27 | u1_cts# | A4 | vcc1p2 | M13 | vcc1p2 | U16 |
| rbias[0] | E20 | s_stat6 | E26 | u1_rts# | C4 | vcc1p2 | M15 | vcc1p2 | U18 |
| rbias[1] | E15 | s_stat7 | D26 | u1_rxd | C5 | vcc1p2 | M17 | vcc1p2 | U20 |
| rbias_sense[0] | E21 | s_txn[0] | D20 | u1_txd | B4 | vcc1p2 | M19 | vcc1p2 | V7 |
| rbias_sense[1] | E16 | s_txn[1] | D22 | vcc1p2 | G8 | vcc1p2 | M21 | vcc1p2 | V9 |
| refclkn | AK19 | s_txn[2] | D19 | vcc1p2 | G10 | vcc1p2 | N8 | vcc1p2 | V11 |
| refclkp | AK20 | s_txn[3] | D23 | vcc1p2 | H7 | vcc1p2 | N10 | vcc1p2 | V13 |
| s_act0 | C26 | s_txn[4] | D14 | vcc1p2 | H9 | vcc1p2 | N12 | vcc1p2 | V15 |
| s_act1 | A27 | s_txn[5] | D16 | vcc1p2 | H11 | vcc1p2 | N14 | vcc1p2 | V17 |
| s_act2 | B25 | s_txn[6] | D13 | vcc1p2 | H13 | vcc1p2 | N16 | vcc1p2 | V19 |
| s_act3 | C25 | s_txn[7] | D17 | vcc1p2 | H17 | vcc1p2 | N18 | vcc1p2 | V21 |
| s_act4 | E27 | s_txp[0] | C20 | vcc1p2 | H19 | vcc1p2 | N20 | vcc1p2 | W8 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 4 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|--------|------|--------|------|----------|------|-------------|------|---------|------|
| vcc1p2 | W10 | vcc1p2 | AD11 | vcc1p2 | AJ12 | vcc1p2as | F22 | vcc1p2x | L30 |
| vcc1p2 | W12 | vcc1p2 | AD13 | vcc1p2 | AJ14 | vcc1p2as | F23 | vcc1p2x | M23 |
| vcc1p2 | W14 | vcc1p2 | AD15 | vcc1p2 | AJ16 | vcc1p2as | F24 | vcc1p2x | M25 |
| vcc1p2 | W16 | vcc1p2 | AD17 | vcc1p2 | AJ18 | vcc1p2as | G22 | vcc1p2x | M27 |
| vcc1p2 | W18 | vcc1p2 | AD19 | vcc1p2 | AJ20 | vcc1p2as | G23 | vcc1p2x | M29 |
| vcc1p2 | W20 | vcc1p2 | AD21 | vcc1p2 | AJ22 | vcc1p2as | G24 | vcc1p2x | M31 |
| vcc1p2 | Y7 | vcc1p2 | AE8 | vcc1p2 | AK7 | vcc1p2ds | E13 | vcc1p2x | N22 |
| vcc1p2 | Y9 | vcc1p2 | AE10 | vcc1p2 | AK9 | vcc1p2ds | E17 | vcc1p2x | N24 |
| vcc1p2 | Y11 | vcc1p2 | AE12 | vcc1p2 | AK11 | vcc1p2ds | F12 | vcc1p2x | N26 |
| vcc1p2 | Y13 | vcc1p2 | AE14 | vcc1p2 | AK13 | vcc1p2ds | F14 | vcc1p2x | N28 |
| vcc1p2 | Y15 | vcc1p2 | AE16 | vcc1p2 | AK15 | vcc1p2ds | G12 | vcc1p2x | N30 |
| vcc1p2 | Y17 | vcc1p2 | AE18 | vcc1p2 | AK17 | vcc1p2ds | G13 | vcc1p2x | P23 |
| vcc1p2 | Y19 | vcc1p2 | AE20 | vcc1p2 | AK21 | vcc1p2e | AM13 | vcc1p2x | P25 |
| vcc1p2 | Y21 | vcc1p2 | AF7 | vcc1p2 | AK23 | vcc1p2e | AM14 | vcc1p2x | P27 |
| vcc1p2 | AA8 | vcc1p2 | AF9 | vcc1p2 | AL8 | vcc1p2e | AN13 | vcc1p2x | P29 |
| vcc1p2 | AA10 | vcc1p2 | AF11 | vcc1p2 | AL10 | vcc1p2e | AN14 | vcc1p2x | P31 |
| vcc1p2 | AA12 | vcc1p2 | AF13 | vcc1p2 | AL12 | vcc1p2e | AN15 | vcc1p2x | R22 |
| vcc1p2 | AA14 | vcc1p2 | AF15 | vcc1p2 | AL14 | vcc1p2e | AN16 | vcc1p2x | R24 |
| vcc1p2 | AA16 | vcc1p2 | AF17 | vcc1p2 | AL16 | vcc1p2plld | AD29 | vcc1p2x | R26 |
| vcc1p2 | AA18 | vcc1p2 | AF19 | vcc1p2 | AL18 | vcc1p2pllp | P11 | vcc1p2x | R28 |
| vcc1p2 | AA20 | vcc1p2 | AF21 | vcc1p2 | AL22 | vcc1p2plls0 | J20 | vcc1p2x | R30 |
| vcc1p2 | AB7 | vcc1p2 | AG8 | vcc1p2 | AM12 | vcc1p2plls1 | J15 | vcc1p2x | T23 |
| vcc1p2 | AB9 | vcc1p2 | AG10 | vcc1p2 | AN12 | vcc1p2x | H25 | vcc1p2x | T25 |
| vcc1p2 | AB11 | vcc1p2 | AG12 | vcc1p2 | AP12 | vcc1p2x | H27 | vcc1p2x | T27 |
| vcc1p2 | AB13 | vcc1p2 | AG14 | vcc1p2 | AR12 | vcc1p2x | H29 | vcc1p2x | T29 |
| vcc1p2 | AB15 | vcc1p2 | AG16 | vcc1p2 | AT12 | vcc1p2x | H31 | vcc1p2x | T31 |
| vcc1p2 | AB17 | vcc1p2 | AG18 | vcc1p2 | AU12 | vcc1p2x | J26 | vcc1p2x | U22 |
| vcc1p2 | AB19 | vcc1p2 | AG20 | vcc1p2ae | AM15 | vcc1p2x | J28 | vcc1p2x | U24 |
| vcc1p2 | AB21 | vcc1p2 | AH7 | vcc1p2ae | AM16 | vcc1p2x | J30 | vcc1p2x | U26 |
| vcc1p2 | AC8 | vcc1p2 | AH9 | vcc1p2ae | AM17 | vcc1p2x | K23 | vcc1p2x | U28 |
| vcc1p2 | AC10 | vcc1p2 | AH11 | vcc1p2ae | AM18 | vcc1p2x | K25 | vcc1p2x | U30 |
| vcc1p2 | AC12 | vcc1p2 | AH13 | vcc1p2ae | AM21 | vcc1p2x | K27 | vcc1p2x | V23 |
| vcc1p2 | AC14 | vcc1p2 | AH15 | vcc1p2ae | AM22 | vcc1p2x | K29 | vcc1p2x | V25 |
| vcc1p2 | AC16 | vcc1p2 | AH17 | vcc1p2ae | AM23 | vcc1p2x | K31 | vcc1p2x | V27 |
| vcc1p2 | AC18 | vcc1p2 | AH19 | vcc1p2ae | AM24 | vcc1p2x | L22 | vcc1p2x | V31 |
| vcc1p2 | AC20 | vcc1p2 | AH21 | vcc1p2as | E22 | vcc1p2x | L24 | vcc1p2x | W22 |
| vcc1p2 | AD7 | vcc1p2 | AJ8 | vcc1p2as | E23 | vcc1p2x | L26 | vcc1p2x | W24 |
| vcc1p2 | AD9 | vcc1p2 | AJ10 | vcc1p2as | E24 | vcc1p2x | L28 | vcc1p2x | W26 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 5 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|---------|------|---------|------|---------|------|---------|------|-----------|------|
| vcc1p2x | W28 | vcc1p2x | AG28 | vcc1p8 | W32 | vcc1p8s | G19 | vcc3p3 | AM31 |
| vcc1p2x | W30 | vcc1p2x | AG30 | vcc1p8 | Y32 | vcc3p3 | E5 | vcc3p3 | AN5 |
| vcc1p2x | Y23 | vcc1p2x | AH23 | vcc1p8 | AA32 | vcc3p3 | F6 | PUR1 | AN8 |
| vcc1p2x | Y25 | vcc1p2x | AH25 | vcc1p8 | AB32 | vcc3p3 | F7 | vcc3p3 | AN30 |
| vcc1p2x | Y27 | vcc1p2x | AH27 | vcc1p8 | AC32 | vcc3p3 | F8 | vcc3p3 | AN31 |
| vcc1p2x | Y31 | vcc1p2x | AH29 | vcc1p8 | AD32 | vcc3p3 | F9 | vcc3p3 | AP30 |
| vcc1p2x | AA22 | vcc1p2x | AH31 | vcc1p8 | AE32 | vcc3p3 | F10 | vcc3p3pll | Y29 |
| vcc1p2x | AA24 | vcc1p2x | AJ24 | vcc1p8 | AF32 | vcc3p3 | F11 | vccvio | H5 |
| vcc1p2x | AA26 | vcc1p2x | AJ26 | vcc1p8 | AG32 | vcc3p3 | F32 | vccvio | H6 |
| vcc1p2x | AA28 | vcc1p2x | AJ27 | vcc1p8 | AH32 | vcc3p3 | G6 | vccvio | L5 |
| vcc1p2x | AA30 | vcc1p2x | AJ28 | vcc1p8 | AJ32 | vcc3p3 | G25 | vccvio | L6 |
| vcc1p2x | AB23 | vcc1p2x | AJ30 | vcc1p8 | AK32 | vcc3p3 | G26 | vccvio | M6 |
| vcc1p2x | AB25 | vcc1p2x | AK25 | vcc1p8 | AL32 | vcc3p3 | G27 | vccvio | P5 |
| vcc1p2x | AB27 | vcc1p2x | AK27 | vcc1p8 | AM32 | vcc3p3 | G28 | vccvio | P6 |
| vcc1p2x | AB29 | vcc1p2x | AK29 | vcc1p8 | AN32 | vcc3p3 | G29 | vccvio | U5 |
| vcc1p2x | AB31 | vcc1p2x | AK31 | vcc1p8 | AP32 | vcc3p3 | G30 | vccvio | U6 |
| vcc1p2x | AC22 | vcc1p2x | AL24 | vcc1p8 | AR32 | vcc3p3 | G31 | vccvio | Y6 |
| vcc1p2x | AC24 | vcc1p2x | AL26 | vcc1p8 | AT32 | vcc3p3 | G32 | vccvio | AA5 |
| vcc1p2x | AC26 | vcc1p2x | AL27 | vcc1p8 | AU32 | vcc3p3 | J6 | vccvio | AA6 |
| vcc1p2x | AC28 | vcc1p2x | AL28 | vcc1p8e | AM25 | vcc3p3 | K6 | vccvio | AC6 |
| vcc1p2x | AC30 | vcc1p2x | AL30 | vcc1p8e | AM26 | vcc3p3 | N6 | vccvio | AD5 |
| vcc1p2x | AD23 | vcc1p2x | AM27 | vcc1p8e | AN17 | vcc3p3 | R6 | vccvio | AD6 |
| vcc1p2x | AD25 | vcc1p2x | AN27 | vcc1p8e | AN18 | vcc3p3 | T6 | vccvio | AF6 |
| vcc1p2x | AD27 | vcc1p2x | AP27 | vcc1p8e | AN21 | vcc3p3 | V6 | vccvio | AG5 |
| vcc1p2x | AD31 | vcc1p2x | AR27 | vcc1p8e | AN22 | vcc3p3 | W6 | vccvio | AG6 |
| vcc1p2x | AE22 | vcc1p2x | AT27 | vcc1p8e | AN23 | vcc3p3 | AB6 | vccvio | AJ6 |
| vcc1p2x | AE24 | vcc1p2x | AU27 | vcc1p8e | AN24 | vcc3p3 | AE6 | vccvio | AK5 |
| vcc1p2x | AE26 | vcc1p8 | H32 | vcc1p8e | AN25 | vcc3p3 | AH6 | vccvio | AK6 |
| vcc1p2x | AE28 | vcc1p8 | J32 | vcc1p8e | AN26 | vcc3p3 | AL6 | vss | A3 |
| vcc1p2x | AE30 | vcc1p8 | K32 | vcc1p8e | AP26 | vcc3p3 | AM6 | vss | A35 |
| vcc1p2x | AF23 | vcc1p8 | L32 | vcc1p8e | AR26 | vcc3p3 | AM7 | vss | B2 |
| vcc1p2x | AF25 | vcc1p8 | M32 | vcc1p8e | AT26 | vcc3p3 | AM8 | vss | B7 |
| vcc1p2x | AF27 | vcc1p8 | N32 | vcc1p8e | AU26 | vcc3p3 | AM9 | vss | B10 |
| vcc1p2x | AF29 | vcc1p8 | P32 | vcc1p8s | E18 | vcc3p3 | AM10 | vss | B27 |
| vcc1p2x | AF31 | vcc1p8 | R32 | vcc1p8s | E19 | vcc3p3 | AM11 | vss | B30 |
| vcc1p2x | AG22 | vcc1p8 | T32 | vcc1p8s | F18 | vcc3p3 | AM28 | vss | B36 |
| vcc1p2x | AG24 | vcc1p8 | U32 | vcc1p8s | F19 | vcc3p3 | AM29 | vss | C1 |
| vcc1p2x | AG26 | vcc1p8 | V32 | vcc1p8s | G18 | vcc3p3 | AM30 | vss | C34 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 6 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|--------|------|--------|------|--------|------|--------|------|--------|------|
| vss | C37 | vss | J34 | vss | M22 | vss | R15 | vss | V10 |
| vss | D4 | vss | J36 | vss | M24 | vss | R17 | vss | V12 |
| vss | D7 | vss | K2 | vss | M26 | vss | R19 | vss | V14 |
| vss | D10 | vss | K4 | vss | M28 | vss | R2 1 | vss | V16 |
| vss | D27 | vss | K8 | vss | M30 | vss | R2 3 | vss | V18 |
| vss | D30 | vss | K10 | vss | M33 | vss | R2 5 | vss | V20 |
| vss | E2 | vss | K12 | vss | N2 | vss | R2 7 | vss | V22 |
| vss | E33 | vss | K14 | vss | N4 | vss | R2 9 | vss | V24 |
| vss | F34 | vss | K16 | vss | N7 | vss | R3 1 | vss | V26 |
| vss | F36 | vss | K18 | vss | N9 | vss | T2 | vss | V30 |
| vss | G2 | vss | K20 | vss | N13 | vss | T4 | vss | V35 |
| vss | G4 | vss | K22 | vss | N15 | vss | T8 | vss | W1 |
| vss | G7 | vss | K24 | vss | N17 | vss | T10 | vss | W2 |
| vss | G9 | vss | K26 | vss | N19 | vss | T12 | vss | W4 |
| vss | G11 | vss | K28 | vss | N21 | vss | T14 | vss | W7 |
| vss | H8 | vss | K30 | vss | N23 | vss | T16 | vss | W9 |
| vss | H10 | vss | K34 | vss | N25 | vss | T18 | vss | W11 |
| vss | H12 | vss | K36 | vss | N27 | vss | T20 | vss | W13 |
| vss | H14 | vss | L7 | vss | N29 | vss | T22 | vss | W15 |
| vss | H15 | vss | L9 | vss | N31 | vss | T24 | vss | W17 |
| vss | H16 | vss | L11 | vss | N34 | vss | T26 | vss | W19 |
| vss | H18 | vss | L13 | vss | N36 | vss | T28 | vss | W2 1 |
| vss | H22 | vss | L15 | vss | P8 | vss | T30 | vss | W2 3 |
| vss | H24 | vss | L17 | vss | P10 | vss | T34 | vss | W2 5 |
| vss | H26 | vss | L19 | vss | P12 | vss | T36 | vss | W2 7 |
| vss | H28 | vss | L21 | vss | P14 | vss | U7 | vss | W3 1 |
| vss | H30 | vss | L23 | vss | P16 | vss | U9 | vss | W3 3 |
| vss | J7 | vss | L25 | vss | P18 | vss | U11 | vss | Y8 |
| vss | J9 | vss | L27 | vss | P20 | vss | U13 | vss | Y10 |
| vss | J11 | vss | L29 | vss | P22 | vss | U15 | vss | Y12 |
| vss | J13 | vss | L31 | vss | P24 | vss | U17 | vss | Y14 |
| vss | J17 | vss | M8 | vss | P26 | vss | U19 | vss | Y16 |
| vss | J19 | vss | M10 | vss | P28 | vss | U21 | vss | Y18 |
| vss | J23 | vss | M12 | vss | P30 | vss | U23 | vss | Y20 |
| vss | J25 | vss | M14 | vss | R7 | vss | U25 | vss | Y22 |
| vss | J27 | vss | M16 | vss | R9 | vss | U27 | vss | Y24 |
| vss | J29 | vss | M18 | vss | R11 | vss | U31 | vss | Y26 |
| vss | J31 | vss | M20 | vss | R13 | vss | V8 | vss | Y28 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 7 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|--------|------|--------|------|--------|------|--------|------|--------|------|
| vss | Y30 | vss | AC21 | vss | AF14 | vss | AJ7 | vss | AL33 |
| vss | Y35 | vss | AC23 | vss | AF16 | vss | AJ9 | vss | AM34 |
| vss | AA7 | vss | AC25 | vss | AF18 | vss | AJ11 | vss | AM36 |
| vss | AA9 | vss | AC27 | vss | AF20 | vss | AJ13 | vss | AP4 |
| vss | AA11 | vss | AC31 | vss | AF22 | vss | AJ15 | vss | AP7 |
| vss | AA13 | vss | AD8 | vss | AF24 | vss | AJ17 | vss | AP10 |
| vss | AA15 | vss | AD10 | vss | AF26 | vss | AJ19 | vss | AP28 |
| vss | AA17 | vss | AD12 | vss | AF28 | vss | AJ21 | vss | AP31 |
| vss | AA19 | vss | AD14 | vss | AF30 | vss | AJ23 | vss | AR1 |
| vss | AA21 | vss | AD16 | vss | AG7 | vss | AJ25 | vss | AR34 |
| vss | AA23 | vss | AD18 | vss | AG9 | vss | AJ29 | vss | AR37 |
| vss | AA25 | vss | AD20 | vss | AG11 | vss | AJ31 | vss | AT2 |
| vss | AA27 | vss | AD22 | vss | AG13 | vss | AJ34 | vss | AT7 |
| vss | AA29 | vss | AD24 | vss | AG15 | vss | AJ36 | vss | AT10 |
| vss | AA31 | vss | AD26 | vss | AG17 | vss | AK8 | vss | AT28 |
| vss | AB2 | vss | AD28 | vss | AG19 | vss | AK10 | vss | AT31 |
| vss | AB4 | vss | AD30 | vss | AG21 | vss | AK12 | vss | AT36 |
| vss | AB8 | vss | AD33 | vss | AG23 | vss | AK14 | vss | AU3 |
| vss | AB10 | vss | AE2 | vss | AG25 | vss | AK16 | vss | AU33 |
| vss | AB12 | vss | AE4 | vss | AG27 | vss | AK18 | vss | AU34 |
| vss | AB14 | vss | AE7 | vss | AG29 | vss | AK22 | vss | AU35 |
| vss | AB16 | vss | AE9 | vss | AG31 | vss | AK24 | vssa s | A12 |
| vss | AB18 | vss | AE11 | vss | AH2 | vss | AK26 | vssa s | A15 |
| vss | AB20 | vss | AE13 | vss | AH4 | vss | AK28 | vssa s | A18 |
| vss | AB22 | vss | AE15 | vss | AH8 | vss | AK30 | vssa s | A21 |
| vss | AB24 | vss | AE17 | vss | AH10 | vss | AL2 | vssa s | A24 |
| vss | AB26 | vss | AE19 | vss | AH12 | vss | AL4 | vssa s | B12 |
| vss | AB28 | vss | AE21 | vss | AH14 | vss | AL7 | vssa s | B15 |
| vss | AB30 | vss | AE23 | vss | AH16 | vss | AL9 | vssa s | B18 |
| vss | AB34 | vss | AE25 | vss | AH18 | vss | AL11 | vssa s | B21 |
| vss | AB36 | vss | AE27 | vss | AH20 | vss | AL13 | vssa s | B24 |
| vss | AC7 | vss | AE29 | vss | AH22 | vss | AL15 | vssa s | C12 |
| vss | AC9 | vss | AE31 | vss | AH24 | vss | AL17 | vssa s | C15 |
| vss | AC11 | vss | AE34 | vss | AH26 | vss | AL21 | vssa s | C18 |
| vss | AC13 | vss | AE36 | vss | AH28 | vss | AL23 | vssa s | C21 |
| vss | AC15 | vss | AF8 | vss | AH30 | vss | AL25 | vssa s | C24 |
| vss | AC17 | vss | AF10 | vss | AH34 | vss | AL29 | vssa s | D12 |
| vss | AC19 | vss | AF12 | vss | AH36 | vss | AL31 | vssa s | D15 |



Table 16. Intel® 81348 I/O processor 1357-Lead Package—Alphabetical Signal Listings (Sheet 8 of 8)

| Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball | Signal | Ball |
|--------|------|--------|------|--------|------|-----------|------|----------|------|
| vssas | D18 | vsse | AP13 | vsse | AR25 | vsse | AU22 | xint#[0] | B8 |
| vssas | D21 | vsse | AP16 | vsse | AT13 | vsse | AU25 | xint#[1] | A9 |
| vssas | D24 | vsse | AP19 | vsse | AT16 | vssp d | AC29 | xint#[2] | A8 |
| vssds | E12 | vsse | AP22 | vsse | AT19 | vssp p | N11 | xint#[3] | B9 |
| vssds | E14 | vsse | AP25 | vsse | AT22 | vssp s0 | J21 | xint#[4] | D9 |
| vssds | F13 | vsse | AR13 | vsse | AT25 | vssp s1 | J16 | xint#[5] | C9 |
| vssds | F17 | vsse | AR16 | vsse | AU13 | vssp x | U29 | xint#[6] | C8 |
| vssds | G14 | vsse | AR19 | vsse | AU16 | warm_rst# | E4 | xint#[7] | E9 |
| vssds | G17 | vsse | AR22 | vsse | AU19 | we# | L33 | | |

a. MA[14] is only needed for 4GB memory support. When 4GB memory is not used this pin is NC.



4.0 Electrical Specifications

Table 17. Absolute Maximum Ratings

| Parameter | Maximum Rating |
|--|-----------------------------|
| Storage temperature | -10°C to +45°C |
| Supply voltage V_{CC3P3} wrt. V_{SS} | -0.5 V to +4.1 V |
| Supply voltage V_{CC1P8S} wrt. V_{SSAS} | -0.5 V to +2.5 V |
| Supply voltage V_{CC1P8E} wrt. V_{SSE} | -0.5 V to +2.5 V |
| Supply voltage V_{CC1P8} wrt. V_{SS} | -0.5 V to +2.5 V |
| Supply voltage V_{CCVIO} wrt. V_{SS} | -0.5 V to +4.1 V |
| Supply voltage V_{CC1P2X} wrt. V_{SS} | -0.5 V to +1.8 V |
| Supply voltage V_{CC1P2} wrt. V_{SS} | -0.5 V to +1.8 V |
| Supply voltage $V_{CC1P2AE}$ wrt. V_{SSE} | -0.5 V to +1.8 V |
| Supply voltage V_{CC1P2E} wrt. V_{SSE} | -0.5 V to +1.8 V |
| Supply voltage $V_{CC1P2AS}$ wrt. V_{SSAS} | -0.5 V to +1.8 V |
| Supply voltage $V_{CC1P2DS}$ wrt. V_{SSDS} | -0.5 V to +1.8 V |
| Voltage on any ball wrt. V_{SS} | -0.5 V to $V_{CCP} + 0.5$ V |

Notice: This data sheet contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

†WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

**Table 18. Operating Conditions**

| Symbol | Parameter | Minimum | Maximum | Units | Notes |
|------------------|--|-----------------|-----------------|-------|-------|
| V_{CC3P3} | 3.3 V supply voltage for PCI-X category 2 signals and general purpose I/Os | 3.0 | 3.6 | V | |
| V_{CC1P8S} | 1.8 V supply voltage for storage interface | 1.71 | 1.89 | V | |
| V_{CC1P8E} | 1.8 V supply voltage for PCI Express* interface | 1.71 | 1.89 | V | |
| V_{CC1P8} | 1.8 V supply voltage for DDR2 SDRAM memory interface I/Os | 1.71 | 1.89 | V | |
| V_{CCVIO} | 3.3 V supply voltage for PCI-X category 1 signals | 3.0 | 3.6 | V | |
| V_{CC1P2X} | 1.2 V supply voltage for Intel XScale® processors | 1.164 | 1.236 | V | |
| V_{CC1P2} | 1.2 V supply voltage for most digital logic | 1.164 | 1.236 | V | |
| V_{CC1P2E} | 1.2 V supply voltage for PCI Express* interface digital logic | 1.164 | 1.236 | V | |
| $V_{CC1P2AE}$ | 1.2 V supply voltage for PCI Express* interface analog logic | 1.164 | 1.236 | V | |
| $V_{CC1P2AS}$ | 1.2 V supply voltage for storage interface analog logic | 1.164 | 1.236 | V | |
| $V_{CC1P2DS}$ | 1.2 V supply voltage for storage interface digital logic | 1.164 | 1.236 | V | |
| $V_{CC1P2PLLS0}$ | 1.2 V supply voltage for storage PLL 0 | 1.164 | 1.236 | V | |
| $V_{CC1P2PLLS1}$ | 1.2 V supply voltage for storage PLL 1 | 1.164 | 1.236 | V | |
| $V_{CC1P2PLLP}$ | 1.2 V supply voltage for PCI-X PLL | 1.164 | 1.236 | V | |
| $V_{CC1P2PLLD}$ | 1.2 V supply voltage for DDR2 SDRAM PLL processor logic PLL | 1.164 | 1.236 | V | |
| $V_{CC3P3PLLX}$ | 3.3 V supply voltage for processor logic PLL | 3.0 | 3.6 | V | |
| M_VREF | Memory I/O reference voltage | $0.49V_{CC1P8}$ | $0.51V_{CC1P8}$ | V | |
| T_C | Case temperature under bias | 0 | 100 | °C | |

4.1 V_{CC}PLL Pin Requirements

To reduce clock jitter, the **V_{CC1P2PLLD}**, **V_{CC1P2PLL}**, and **V_{CC3P3PLLX}**, **V_{CC1P2PLLS0}** and **V_{CC1P2PLLS1}** balls for the phase-lock loop (PLL) circuits are isolated on the package. The low-pass filters, as shown in the following figures, reduce noise-induced clock jitter and its effects on timing relationships in system design.

This paragraph pertains to the **V_{CC1P2PLLD}**, **V_{CC1P2PLL}**, **V_{CC3P3PLLX}** filters. The filter components must be able to handle a DC current of 30 mA. Use a shielded type inductor to minimize magnetic pickup. The total series resistance from the board VCC plane (before the filter) to the VCCPLL ball must be less than 1.5 ohm (including component and trace resistance). The total series resistance from the board VCC plane (before the filter) to the top plate of the capacitor must be greater than 0.35 ohm (including component and trace resistance). The nodes connecting VCCPLL and VSSPLL to the capacitor must be as short as possible (less than 0.1 W). VCCPLL and VSSPLL must be routed close to each other to minimize loop area. The VSSPLL balls must be connected to the filter only and not to any other ground, as shown in [Figure 7](#) and [Figure 9](#). The inductor and capacitor must be placed close to each other. Any discrete resistor must be placed between the VCC board plane and the inductor. If the trace and component resistance is high enough, a discrete resistor might not be required.

This paragraph pertains to the **V_{CC1P2PLLS0}**, **V_{CC1P2PLLS1}** filters. The recommended filter for the PLL supplies is shown in [Figure 8](#). The purpose of this filter is to achieve at least 10 dB rejection of frequencies between 1 and 20 MHz. The current draw for the IC is less than 85 mA. The board's supply distribution system must ensure that the minimum voltage into the filter is equal to or greater than 1.14 V. The filter components are selected to achieve a corner frequency of 100 KHz. The series resistance keeps the Q of this resonant circuit safely below unity for all component variations.

The bypass capacitor must be placed as close to the supply pins as possible. The series impedances to both the supply pin and the PCB analog ground plane must be an order of magnitude lower than the ESR and ESL specified for the capacitor. The S0/S1 PLLs have dedicated internal supplies, so the VSSPLLS0/S1 pins must be soldered directly to the analog ground plane of the PCB.

Figure 7. V_{CC3P3PLLX} Low-Pass Filter

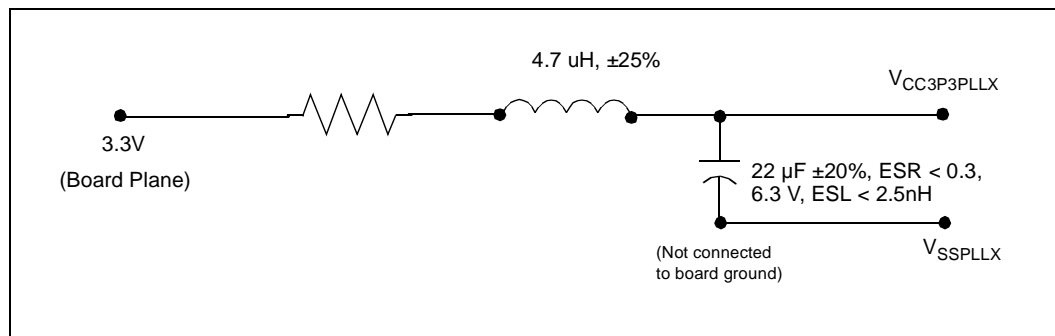




Figure 8. $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Low-Pass Filter

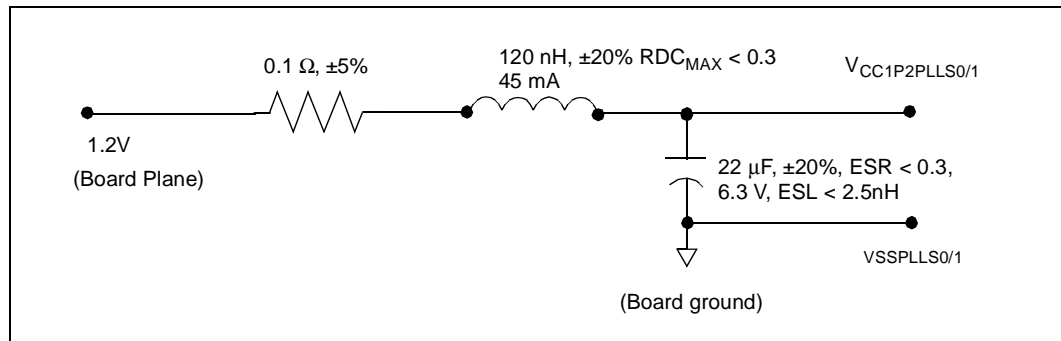
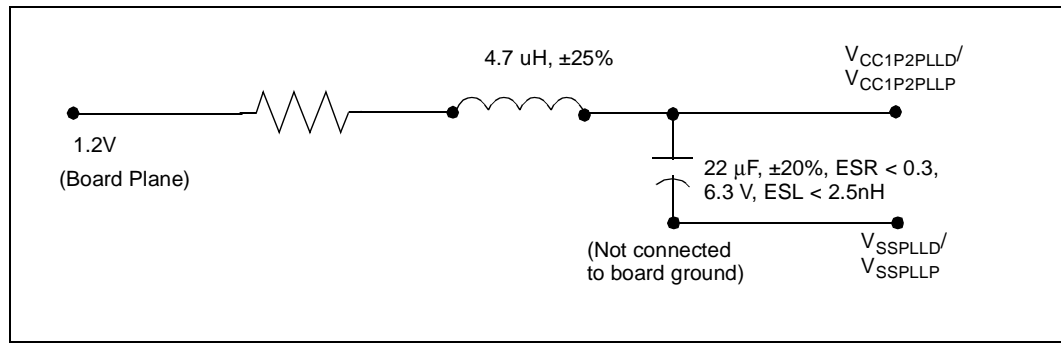


Figure 9. $V_{CC1P2PLLD}$, $V_{CC1P2PLL}$ Low-Pass Filter





4.2 Targeted DC Specifications

Table 19. DC Characteristics

| Symbol | Parameter | Minimum | Maximum | Units | Notes |
|-------------------|---|-----------------------|--------------------------|-------|---|
| V _{IL1} | Input Low Voltage (General Purpose). | -0.3 | 0.3V _{CC3P3} | V | 2 |
| V _{IH1} | Input High Voltage (General Purpose). | 2.0 | V _{CC3P3} + 0.3 | V | 2 |
| V _{IL2} | Input Low Voltage (PCI). | -0.5 | 0.3V _{CC3P3} | V | |
| V _{IL3} | Input Low Voltage (PCI-X). | -0.5 | 0.35V _{CC3P3} | V | |
| V _{IH3} | Input High Voltage (PCI-X/PCI). | 0.5V _{CC3P3} | V _{CC3P3} + 0.5 | V | |
| V _{IL4} | Input Low Voltage (DDR2 SDRAM). | -0.3 | M_VREF - 0.125 | V | |
| V _{IH4} | Input High Voltage (DDR2 SDRAM). | M_VREF + 0.125 | V _{CC1P8} + 0.3 | V | |
| V _{OL1} | Output Low Voltage (General Purpose). | - | 0.4 | V | I _{OL} = 10 mA 2 |
| V _{OH1} | Output High Voltage (General Purpose). | 2.6 | - | V | I _{OH} = -10 mA 2 |
| V _{OL2} | Output Low Voltage (PCI-X). | - | 0.1V _{CC3P3} | V | I _{OL} = 1.50 mA |
| V _{OH2} | Output High Voltage (PCI-X). | 0.9V _{CC3P3} | - | V | I _{OH} = -0.50 mA |
| V _{OL3} | Output Low Voltage (DDR2 SDRAM driver set to 21Ω). | | 0.28 | V | I _{OL} = 11 mA |
| V _{OH3} | Output High Voltage (DDR2 SDRAM driver set to 21Ω). | 1.42 | | V | I _{OH} = -11 mA |
| V _{OL4} | Output Low Voltage (DDR2 SDRAM driver set to 50Ω). | | 0.28 | V | I _{OL} = 5 mA |
| V _{OH4} | Output High Voltage (DDR2 SDRAM driver set to 50Ω). | 1.42 | | V | I _{OH} = -5 mA |
| I _{LI1} | Input Leakage Current for General Purpose pins when internal pull up resistors are not enabled. | | ±5 | μA | 0 ≤ V _{IN} ≤ V _{CC3P3} 3 |
| I _{LI2} | Input Leakage Current for PCI-X pins when internal pull up resistors are not enabled. | | ±10 | μA | 0 ≤ V _{IN} ≤ V _{CC3P3} (Cat. 2) 0 ≤ V _{IN} ≤ V _{CCVIO} (Cat. 1) 3 |
| I _{LI3} | Input Leakage Current for DDR2 pins when internal pull up resistors are not enabled. | | ±2 | μA | 0 ≤ V _{IN} ≤ V _{CC1P8} 3 |
| R _{GP} | Internal pull up resistor value for General Purpose pins. | 28.5 | 38.7 | KΩ | 1 |
| R _{PCIX} | Internal pull up resistor value for PCI-X pins. | 5.9 | 8.1 | KΩ | 1 |
| C _{GP} | General Purpose pin Capacitance. | 1 | 4.5 | pF | 1 |
| C _{PCIX} | PCI-X pin Capacitance. | 1 | 4.5 | pF | 1 |
| C _{DDR2} | DDR2 pin Capacitance. | 1 | 4.5 | pF | 1 |
| L _{PIN} | Ball Inductance. | 1 | 12 | nH | 1 |

Notes:

1. Not tested, guaranteed by design.
2. General Purpose signals include all signals that are not part of the DDR2, PCI-X and PCI-Express interfaces or the Storage Tx/Rx pairs and analog pins.
3. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

**Table 20. I_{CC} Characteristics**

| Symbol | Parameter | Typ | Max | Units | Notes |
|---|--|--------------|--------------|-------|---------|
| I _{CC12} Active (Power Supply) | Power Supply Current: Storage PHY, PCI Express, Intel XScale® microarchitecture: <ul style="list-style-type: none"> • 800MHz • 1200MHz | | 7.83 8.39 | A | 1, 2, 4 |
| I _{CC18} Active (Power Supply) | Power Supply Current: Storage PHY I/Os, PCI Express I/Os, DDR-II (533) | | 1.71 | A | 1, 2, 4 |
| I _{CC33} Active (Power Supply) | Power Supply Current: PCI, PBI, GPIO, PCI-X I/Os | | 0.69 | A | 1, 2 |
| I _{CC12} Active (Thermal) | Thermal Current: Storage PHY, PCI Express, Intel XScale® microarchitecture: <ul style="list-style-type: none"> • 800MHz • 1200MHz | 5.55 6.81 | | A | 1, 3, 4 |
| I _{CC18} Active (Thermal) | Thermal Current: Storage PHY I/Os, PCI Express I/Os, DDR-II (533) | 1.40 | | A | 1, 3, 4 |
| I _{CC33} Active (Thermal) | Thermal Current: PCI, PBI, GPIO, PCI-X I/Os | 0.60 | | A | 1, 3 |

Notes:

1. Measured with the device operating and outputs loaded to the test condition in [Figure 17, “AC Test Load for all Signals Except PCI, PCI-Express and DDR2 and Storage PHY” on page 82](#).
2. I_{CC} Active (Power Supply) value is provided for selecting the system power supply. This is based on the worst case data patterns and skew material at the following worst case voltages: V_{CC33} = 3.63 V, V_{CC18} = 1.89 V, V_{CC12} = 1.24 V and ambient temperature = 55C.
3. I_{CC} Active (Thermal) value is provided for selecting the system thermal design power (TDP). This is based on the following typical voltages: V_{CC33} = 3.3 V, V_{CC18} = 1.8V, V_{CC12} = 1.2 V and ambient temperature = 55C.
4. The Customer Reference Boards use a 1.2 V switching regulator for all the 1.2 V supplies (V_{CC1p2}, V_{CC1p2x}, V_{CC1p2e}, V_{CC1p2ds}, V_{CC1p2ae}, V_{CC1p2as}) and a 1.8 V switching regulator for all 1.8 V supplies: (V_{CC1p8}, V_{CC1p8e}, V_{CC1p8s}).



4.3 Targeted AC Specifications

4.3.1 Clock Signal Timings

Table 21. PCI Clock Timings

| Symbol | Parameter | PCI-X 133 | | PCI-X 100 | | PCI-X 66 | | PCI 66 | | PCI 33 | | Units | Notes |
|---|-------------------------------------|-----------|------|-----------|------|----------|------|--------|------|--------|------|-------|-------|
| | | Min. | Max | Min. | Max | Min. | Max | Min. | Max | Min. | Max | | |
| T _{C1} | PCI Clock Cycle Time Jitter Class 1 | 7.5 | 11 | 10 | 15 | 15 | 22 | 15 | 25 | 30 | 50 | ns | 1 |
| T _{C2} | PCI Clock Cycle Time Jitter Class 2 | 7.375 | 11 | 9.875 | 15 | 14.8 | 22 | 14.8 | 25 | 29.7 | 50 | | 1 |
| T _{CH1} | PCI clock High Time | 2.5 | | 3 | | 5.5 | | 5.5 | | 10 | | ns | |
| T _{CL1} | PCI clock Low Time | 2.5 | | 3 | | 5.5 | | 5.5 | | 10 | | ns | |
| | PCI clock Period Jitter | 125 | -125 | 125 | -125 | 200 | -200 | 200 | -200 | 300 | -300 | ps | 3 |
| TSR1 | PCI clock Slew Rate | 1.5 | 4 | 1.5 | 4 | 1.5 | 4 | 1.5 | 4 | 1 | 4 | V/ns | 2 |
| PCI Spread Spectrum Requirements | | | | | | | | | | | | | |
| f _{mod} | PCI clock modulation frequency | 30 | 33 | 30 | 33 | 30 | 33 | 30 | 33 | | | KHz | |
| f _{spread} | PCI clock frequency spread | -1 | 0 | -1 | 0 | -1 | 0 | -1 | 0 | | | % | |
| PCI Output Clocks | | | | | | | | | | | | | |
| | PCI output clock skew | | 250 | | 350 | | 350 | | 350 | | 350 | ps | |
| | PCI output clock period jitter | 100 | -100 | 150 | -150 | 150 | -150 | 150 | -150 | 150 | -150 | ps | 4, 5 |

Notes:

1. The clock frequency may not change beyond the spread-spectrum limits except while **P_RST#** or **WARM_RST#** is asserted.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform.
3. Period jitter is the deviation between any single period of the clock and the average period of the clock.
4. If a jitter class 2 input clock is used, output clocks can not support jitter class 1.
5. The deviation between any single period of the clock and the average period of the clock.



Table 22. PCI Express Clock Timings

| Symbol | Parameter | Min. | Nom. | Max. | Units | Notes |
|--------|--------------------------------------|-------|------|---------|-------|---------------|
| TF2 | PCI Express* Clock Frequency | | 100 | | MHz | 4 |
| TC2 | PCI Express* Clock Cycle Time | 9.872 | | | ns | |
| DF0 | Frequency Variation | -300 | | 300 | ppm | |
| TCCJ | Cycle to Cycle Jitter | | | 125 | ps | |
| TPPJ | Peak to Peak Jitter (5-50 MHz) | | | 50 | ps | |
| Dc | Clock Duty Cycle | 45 | | 55 | % | |
| Trise | REFCLK Rise Time | 175 | | 350 | ps | 1, 2, 6 |
| Tfall | REFCLK Fall Time | 175 | | 350 | ps | 1, 2, 6 |
| Tvrise | REFCLK Rise Time Variation | | | 125 | ps | |
| Tvfall | REFCLK Fall Time Variation | | | 125 | ps | |
| | Rise-Fall Matching | | | 20 | % | |
| Vca | Absolute Cross Point | 0.25 | | 0.55 | V | 1, 3, 7, 13 |
| Vcr | Relative Cross Point | Calc | | Calc | | 5, 12 |
| Tvc | Total Variation of Vc over all edges | | | 0.14 | V | 13 |
| | Rising Edge Ringback | 0.56 | | | V | Absolute Min. |
| | Falling Edge Ringback | | | 0.25 | V | Absolute Max. |
| Vhi | High Level Voltage | 0.66 | 0.71 | 0.85 | V | 7, 8 |
| Vli | Low Level Voltage | -0.15 | 0 | 0.15 | V | 7, 9 |
| Vrb | Ringback Voltage | | | 0.10 | V | 7 |
| Vovs | Maximum Overshoot | | | Vhi+0.3 | V | 7, 10 |
| Vuds | Minimum Undershoot | | | -0.30 | V | 7, 11 |

Notes:

1. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK equals the falling edge of REFCLK#.
2. Measured from $V_{OL} = 0.175$ V to $V_{OH} = 0.525$ V. Valid only for rising REFCLK and falling REFCLK#. Signal must be monotonic through the V_{OL} to V_{OH} region for T_{RISE} and T_{FALL} .
3. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.
4. The average period over any 1 μ s period of time must be greater than the minimum specified period.
5. $V_{CROSS}(rel)$ Min and Max are derived using the following:
 $V_{CROSS}(rel) \text{ Min} = 0.5 (V_{havg} - 0.710) + 0.250$
 $V_{CROSS}(rel) \text{ Max} = 0.5 (V_{havg} - 0.710) + 0.550$
6. Measurement taken from single-ended waveform.
7. Measurement taken from differential waveform.
8. V_{HIGH} is defined as the statistical average High value as obtained by using the Oscilloscope V_{HIGH} Math function.
9. V_{LOW} is defined as the statistical average Low value as obtained by using the Oscilloscope V_{LOW} Math function.
10. Overshoot is defined as the absolute value of the maximum voltage.
11. Undershoot is defined as the absolute value of the minimum voltage.
12. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
13. ΔV_{CROSS} is defined as the total variation of all crossing voltages of Rising REFCLK and Falling REFCLK#. This is the maximum allowed variance in V_{CROSS} for any particular system.
14. Refer to Section 4.3.2.1 in the *PCI Express Base Specification* for information regarding PPM considerations.



Table 23. DDR2 Output Clock Timings

| Symbol | Parameter | DDR2-400 | | DDR2-533 | | Units | Notes |
|--------------------|---|----------|------|----------|------|-------|-------|
| | | Min. | Max | Min. | Max | | |
| T _{CC2} | DDR2 SDRAM clock Cycle Time Average | 5.00 | | 3.75 | | ns | |
| T _{CH2} | DDR2 SDRAM clock High Time | 2.25 | | 1.69 | | ns | |
| T _{CL2} | DDR2 SDRAM clock LowTime | 2.25 | | 1.69 | | ns | |
| T _{CS2} | DDR2 SDRAM clock Period Jitter | 100 | -100 | 100 | -100 | ps | |
| T _{skew2} | DDR2 SDRAM clock skew for any differential clock pair to any other clock pair | | 250 | | 250 | ps | |
| T _{skew3} | DDR2 SDRAM clock skew for any clock pair to any system memory strobe | | 250 | | 250 | ps | |
| Notes: | | | | | | | |
| 1. Not tested | | | | | | | |



4.3.2 DDR2 SDRAM Interface Signal Timings

Table 24. DDR2 SDRAM Signal Timings

| Symbol | Parameter | Min. | Max | Units | Notes |
|--------|--|--------|-------|-------|-------|
| Tvb1 | DQ, CB and DM write output valid time before DQS | 0.530 | | ns | 1, 3 |
| Tva1 | DQ, CB and DM write output valid time after DQS | 0.530 | | ns | 1, 3 |
| Tvb2 | DQS write output valid time before M_CLK (DQS early) | | 0.200 | ns | 1, 3 |
| Tva2 | DQS write output valid time after M_CLK (DQS late) | | 0.530 | ns | 1, 3 |
| Tvb3 | MA, BA, RAS#, CAS#, WE# write output valid before M_CLK rising edge. | 4.900 | | ns | 1, 3 |
| Tva3 | MA, BA, RAS#, CAS#, WE# write output valid after M_CLK rising edge. | 1.530 | | ns | 1, 3 |
| Tvb4 | CS#, CKE, ODT write output valid before M_CLK rising edge. Unbuffered mode | 2.090 | | ns | 1, 3 |
| Tva4 | CS#, CKE, ODT write output valid after M_CLK rising edge. Unbuffered mode | 0.590 | | ns | 1, 3 |
| Tvb5 | CS#, CKE, ODT write output valid before M_CLK rising edge. Registered mode | 1.150 | | ns | 1, 3 |
| Tva5 | CS#, CKE, ODT write output valid after M_CLK rising edge. Registered mode | 1.530 | | ns | 1, 3 |
| Tis6 | DQ, CB read input setup time before DQS rising or falling edges. | -0.670 | | ns | 2 |
| Tih6 | DQ, CB read input hold time after DQS rising or falling edges. | 1.250 | | ns | 2 |
| Tov7 | M_CLK[2:0] output valid from P_CLKIN or REFCLK | 0.460 | 1.930 | ns | |

Notes:

1. See Figure 14, "DDR2 SDRAM Write Timings" on page 81.
2. See Figure 16, "DDR2 SDRAM Read Timings" on page 82. Timings valid when the DQS delay is programmed for the default 90 degree phase shift.
3. See Figure 18, "AC Test Load for DDR2 SDRAM Signals" on page 82.



4.3.3 Peripheral Bus Interface Signal Timings

Table 25. Peripheral Bus Interface Signal Timings

| Symbol | Parameter | Min. | Nom. | Max. | Units |
|--------|--|---------|--|----------|--------|
| A2D | Address to Data wait-states | 4 | - | 20 | clks |
| D2D | Data to Data wait-states | 4 | - | 20 | clks |
| REC | Recovery wait-states | 1 | - | 20 | clks |
| N | Number of Data phases | 1 | - | 4 | phases |
| Tasc | Address setup to CE# | 25 | 30 | - | ns |
| Taso | Address setup to OE# | 10 | 15 | - | ns |
| Tasw | Address setup to WE# | 25 | 30 | - | ns |
| Tah | Address hold from CE#,OE# | Nom - 5 | REC × 15 | - | ns |
| Tahw | Address hold from WE# | Nom - 5 | (REC+1) × 15 | - | ns |
| Twce | CE# pulse width | Nom - 5 | $(A2D + 2 + ((N - 1)(D2D + 2))) \times 15$ | - | ns |
| Twoe | OE# pulse width | Nom - 5 | $(A2D + 3 + ((N - 1)(D2D + 2))) \times 15$ | - | ns |
| Twwe | WE# pulse width | Nom - 5 | $(A2D + 1) \times 15$ | - | ns |
| Tdsw | Write Data setup to WE# | Nom - 5 | $(A2D + 1) \times 15$ | - | ns |
| Tdhw | Write Data hold from WE# | 10 | 15 | 20 | ns |
| Tad1 | 1st Read Data access time from Address | - | $(A2D + 4) \times 15$ | Nom - 11 | ns |
| TadN | Nth Read Data access time from Address | - | $(D2D + 2) \times 15$ | Nom - 11 | ns |
| Tcd | Read Data access time from CE# | - | $(A2D + 2) \times 15$ | Nom - 11 | ns |
| Toe | Read Data access time from OE# | 0 | $(A2D + 3) \times 15$ | Nom - 11 | ns |
| Tdh | Read Data hold time from Address, CE#, OE# | 0 | $(REC + 2) \times 15$ | Nom - 5 | ns |

Notes:

1. See Figure 25, "PBI Output Timings" on page 85 and Figure 26, "PBI External Device Timings (Flash)" on page 86.



4.3.4 I²C/SMBus Interface Signal Timings

Table 26. I²C/SMBus Signal Timings

| Symbol | Parameter | Std. Mode | | Fast Mode | | Units | Notes |
|--------------------|--|-----------|------|------------------------|-----|-------|-------|
| | | Min. | Max | Min. | Max | | |
| F _{SCL} | SCL Clock Frequency | 0 | 100 | 0 | 400 | KHz | |
| T _{BUF} | Bus Free Time Between STOP and START Condition | 4.7 | | 1.3 | | μs | (1) |
| T _{HDSTA} | Hold Time (repeated) START Condition | 4 | | 0.6 | | μs | (1,3) |
| T _{LOW} | SCL Clock Low Time | 4.7 | | 1.3 | | μs | (1,2) |
| T _{HIGH} | SCL Clock High Time | 4 | | 0.6 | | μs | (1,2) |
| T _{SUSTA} | Setup Time for a Repeated START Condition | 4.7 | | 0.6 | | μs | (1) |
| T _{HDDAT} | Data Hold Time | 0 | 3.45 | 0 | 0.9 | μs | (1) |
| T _{SUDAT} | Data Setup Time | 250 | | 100 | | ns | (1) |
| T _{SR} | SCL and SDA Rise Time | | 1000 | 20 + 0.1C _b | 300 | ns | (1,4) |
| T _{SF} | SCL and SDA Fall Time | | 300 | 20 + 0.1C _b | 300 | ns | (1,4) |
| T _{SUSTO} | Setup Time for STOP Condition | 4 | | 0.6 | | μs | (1) |

Notes:

1. See Figure 13, "I²C Interface Signal Timings" on page 80.
2. Not tested.
3. After this period, the first clock pulse is generated.
4. C_b = the total capacitance of one bus line, in pF.
5. Std Mode I²C signal timings apply for SMBus timing.



4.3.5 PCI Bus Interface Signal Timings

Table 27. PCI Signal Timings

| Symbol | Parameter | PCI-X 133 PCI-X 100 | | PCI-X 66 | | PCI 66 | | PCI 33 | | Units | Notes |
|------------------|--|------------------------|-----|----------|-----|--------|-----|--------|-----|--------|-------|
| | | Min. | Max | Min. | Max | Min. | Max | Min. | Max | | |
| T _{OV1} | Clock to Output Valid Delay | 0.7 | 3.7 | 0.7 | 3.7 | 1 | 6 | 2 | 11 | ns | 1, 3 |
| T _{OF} | Clock to Output Float Delay | | 7 | | 7 | | 14 | | 28 | ns | 1, 4 |
| T _{IS1} | Input Setup to clock | 1.2 | | 1.7 | | 3 | | 7 | | ns | 2 |
| T _{IH1} | Input Hold time from clock | 0.5 | | 0.5 | | 0 | | 0 | | ns | 2 |
| T _{RST} | Reset Active Time | 1 | | 1 | | 1 | | 1 | | ms | |
| T _{RF} | Reset Active to output float delay | | 40 | | 40 | | 40 | | 40 | ns | |
| T _{IS3} | REQ64# to Reset setup time | 10 | | 10 | | 10 | | 10 | | clocks | |
| T _{IH2} | Reset to REQ64# hold time | 0 | 50 | 0 | 50 | 0 | 50 | 0 | 50 | ns | |
| T _{IS4} | PCI-X initialization pattern to Reset setup time | 10 | | 10 | | | | | | clocks | |
| T _{IH3} | Reset to PCI-X initialization pattern hold time | 0 | 50 | 0 | 50 | | | | | ns | |

Notes:

1. See the timing measurement conditions in; [Figure 11, "Output Timing Measurement Waveforms" on page 79.](#)
2. See the timing measurement conditions in; [Figure 12, "Input Timing Measurement Waveforms" on page 80.](#)
3. See [Figure 19, "PCI/PCI-X TOV\(max\) Rising Edge AC Test Load" on page 83,](#) [Figure 20, "PCI/PCI-X TOV\(max\) Falling Edge AC Test Load" on page 83,](#) [Figure 21, "PCI/PCI-X TOV\(min\) AC Test Load" on page 83.](#)
4. For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.



4.3.6 PCI Express Differential Transmitter (Tx) Output Specifications

Table 28. PCI Express* Rx Input Specifications

| Symbol | Parameter | Min. | Nom | Max | Units | Notes |
|-------------------|----------------------------------|-------|-----|-------|-------|-------|
| $V_{DIFFp-p}$ | Differential input voltage | 0.175 | | 1.200 | V | 1 |
| J_{TOTAL} | Total output jitter | | | 0.65 | UI | 2 |
| V_{CM-AC} | AC common mode | | | 100 | mV | 3 |
| T_{Reye} | Receiver eye opening | 0.35 | | | UI | 4 |
| $RL-Diff_{RX}$ | Differential return loss | 12 | | | dB | 5 |
| $RL-CM_{TX}$ | Common mode return loss | 6 | | | dB | 5 |
| $Z_{RX-OUT-DC}$ | DC differential output impedance | 90 | 100 | 110 | Ohm | 6 |
| $Z_{RX-Match-DC}$ | D+/D- impedance matching | -5 | | +5 | % | 7 |
| $V_{RX-SQUELCH}$ | Squelch detect threshold | 75 | | 175 | mV | 8 |
| $C_{in_{RX}}$ | AC coupled | 75 | | | nf | 9 |
| $L_{SKEW-RX}$ | Lane to lane skew at Rx | | | 20 | UI | 10 |

Notes:

1. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 \times V_{RMAX}$. Measured at the package pins of the receiver. See [Figure 12](#).
2. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
3. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
4. See [Figure 24, "Receiver Eye Opening \(Differential\)"](#) on page 84.
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e. as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω . Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 $\Omega \pm 10\%$ tolerance.
7. DC impedance matching between two lanes of a port.
8. Peak-to-Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
9. All receivers shall be AC coupled to the media.
10. Lane skew at the Receiver that must be tolerated.



Table 29. PCI Express* Tx Output Specifications

| Symbol | Parameter | Min. | Nom | Max | Units | Notes |
|--|--|-------|-----|-------|-------|-------|
| UI | Unit Interval | | 400 | | ps | 1 |
| V _{DIFFP-P} | Differential output voltage | 0.800 | | 1.200 | V | 2 |
| T _{riser} , T _{fall} | Driver Rise/Fall Time | 0.2 | | 0.4 | UI | 3 |
| V _{TX-CM-AC} | AC Common Mode | | | 20 | mV | 4 |
| V _{TX-CM-DC} delta | Common Mode Active to Sleep mode delta | -50 | | +50 | mV | |
| RL-Diff _{TX} | Differential Return Loss | 15 | | | dB | 5 |
| RL-CM _{TX} | Common Mode Return Loss | 6 | | | dB | 5 |
| Z _{TX-OUT-DC} | DC Differential Output Impedance | 90 | 100 | 110 | Ω | 6 |
| Z _{TX-Match-DC} | D+/D- impedance matching | -5 | | +5 | % | 7 |
| L _{SKREW-TX} | Lane to Lane Skew at Tx | | | 500 | ps | 8 |
| J _{TOTAL} | Total Output Jitter. | | | 0.35 | UI | 9 |
| T _{Deye} | Minimum Transmitter eye opening. | 0.65 | | | UI | 10 |
| I _{TX-SHORT} | Short circuit Current | -100 | | 100 | mA | 11 |
| V _{TX-IDLE} | Sleep mode Voltage Output | 0 | 0 | 20 | mV | 12 |

Notes:

- ±300 ppm. UI does not account for SSC dictated variations. No test load is necessarily associated with this value. This UI specification is a “before transmission” specification and represents the nominal time of each bit transmission or width.
- Peak-Peak differential voltage. $V_{DIFFP-P} = 2 \times V_{D_{MAX}}$. Specified at the package pins into a 100 Ω test load as shown in Figure 22, “Transmitter Test Load (100 Ω diff Load)” on page 83. Max level set by maximum single ended voltage after a reflection from an open. This value is for the first bit after a transition on the data lines. Subsequent bits of the same polarity shall have an amplitude of 6 dB (±0.5 db) less as measured differentially peak to peak than the specified value.
- 20–80% at transmitter. Slower rise/fall times are better.
- Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
- 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e. as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω. Applicable during active (L0) and Align states only.
- DC Differential Mode Impedance 100 Ω ±10% tolerance. All devices shall employ on-chip adaptive impedance matching circuits to ensure the best possible termination/Zout for its Transmitters (as well as receivers).
- DC impedance matching between two lanes of a port.
- Between any two lanes within a single transmitter.
- Clock source PPM mismatch is in addition to this value. Measured over 250 UI.
- See Figure 23, “Transmitter Eye Diagram” on page 84.
- Between any voltage from max supply to gnd with power on or off.
- Squelch condition. Both signals brought to $V_{CM-DC-|VD+ - VD-|}$



4.3.7 PCI Express* Differential Receiver (Rx) Input Specifications

Table 30. PCI Express* Rx Input Specifications

| Symbol | Parameter | Min. | Nom | Max | Units | Notes |
|-------------------|----------------------------------|-------|-----|-------|----------|-------|
| $V_{DIFFp-p}$ | Differential input voltage | 0.175 | | 1.200 | V | 1 |
| J_{TOTAL} | Total Output Jitter. | | | 0.65 | UI | 2 |
| V_{CM-AC} | AC Common Mode | | | 100 | mV | 3 |
| T_{Reye} | Receiver eye opening. | 0.35 | | | UI | 4 |
| $RL-Diff_{RX}$ | Differential Return Loss | 15 | | | dB | 5 |
| $RL-CM_{TX}$ | Common Mode Return Loss | 6 | | | dB | 5 |
| $Z_{RX-OUT-DC}$ | DC Differential Output Impedance | 90 | 100 | 110 | Ω | 6 |
| $Z_{RX-Match-DC}$ | D+/D- impedance matching | 0-5 | | +5 | % | 7 |
| $V_{RX-SQUELCH}$ | Squelch detect threshold | 75 | | 175 | mV | 8 |
| $C_{in_{RX}}$ | AC coupled | 400 | | | pf | 9 |
| $L_{SKEW-RX}$ | Lane to Lane Skew at Rx | | | 20 | UI | 10 |

Notes:

1. Peak-Peak differential voltage. $V_{DIFFp-p} = 2 * V_{RMAX}$. Measured at the package pins of the receiver. See Figure 12.
2. Max Jitter tolerated by Rx. This is the nominal value tolerated at the package pin of the receiver device. A receiver must therefore tolerate any additional jitter generated by the package to the die.
3. Peak common mode value. $|V_{D+} + V_{D-}|/2 - V_{CM-DC(avg)}$
4. See Figure 24, "Receiver Eye Opening (Differential)" on page 84.
5. 50 MHz to 1.6 GHz. The driver output impedance shall result in a differential return loss greater than or equal to 15 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.8 GHz. This output impedance requirement applies to all valid output levels. The reference impedance for return loss measurements is 100 Ω for differential return loss and 25 Ω for common mode (i.e. as measured by a Vector Network Analyzer with 100 Ω differential probes). Note this is based on a nominal PCI Express* interconnect differential characteristic impedance of 100 Ω . Applicable during active (L0) and Align states only.
6. DC Differential Mode Impedance 100 $\Omega \pm 10\%$ tolerance.
7. DC impedance matching between two lanes of a port.
8. Peak to Peak value. Measured at the pin of the receiver. Differential signal below this level will indicate a squelch condition.
9. All receivers shall be AC coupled to the media.
10. Lane skew at the Receiver that must be tolerated.



4.3.8 Boundary Scan Test Signal Timings

Table 31. Boundary Scan Test Signal Timings

| Symbol | Parameter | Min. | Max | Units | Notes |
|--------------------|------------------------------|------|-------|-------|-------------------------------------|
| T _{JTF} | TCK Frequency | 0 | 66 | MHz | |
| T _{JTCH} | TCK High Time | 7.0 | | ns | Measured at 1.5 V (1) |
| T _{JTCL} | TCK Low Time | 7.0 | | ns | Measured at 1.5 V (1) |
| T _{JTCR} | TCK Rise Time | | 5 | ns | 0.8 V to 2.0 V (1) |
| T _{JTCF} | TCK Fall Time | | 5 | ns | 2.0 V to 0.8 V (1) |
| T _{JTIS1} | Input Setup to TCK—TDI, TMS | 3.0 | | ns | (3) |
| T _{JTIH1} | Input Hold from TCK—TDI, TMS | 2.0 | | ns | (3) |
| T _{JTOV1} | TDO Output Valid Delay | 4.25 | 13.25 | ns | Relative to falling edge of TCK (2) |
| T _{OF1} | TDO Float Delay | 4.25 | 13.25 | ns | Relative to falling edge of TCK (4) |

Notes:

1. Not tested.
2. See Figure 11, "Output Timing Measurement Waveforms" on page 79.
3. See Figure 12, "Input Timing Measurement Waveforms" on page 80.
4. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested. See Figure 11, "Output Timing Measurement Waveforms" on page 79.



4.4 AC Timing Waveforms

Figure 10. Clock Timing Measurement Waveforms

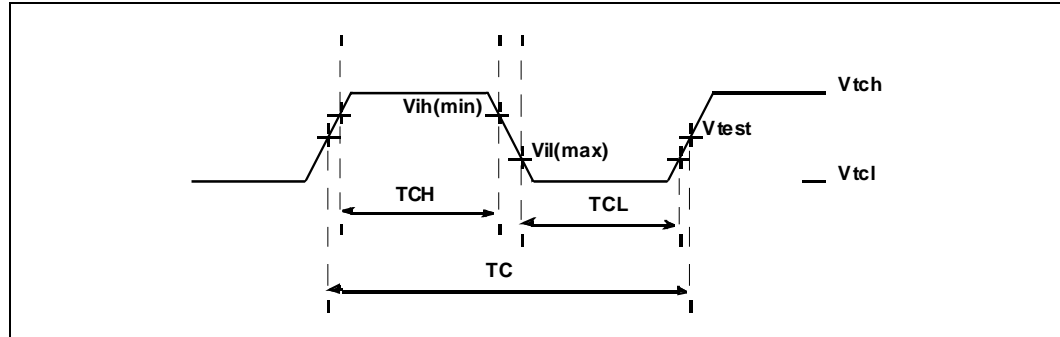


Figure 11. Output Timing Measurement Waveforms

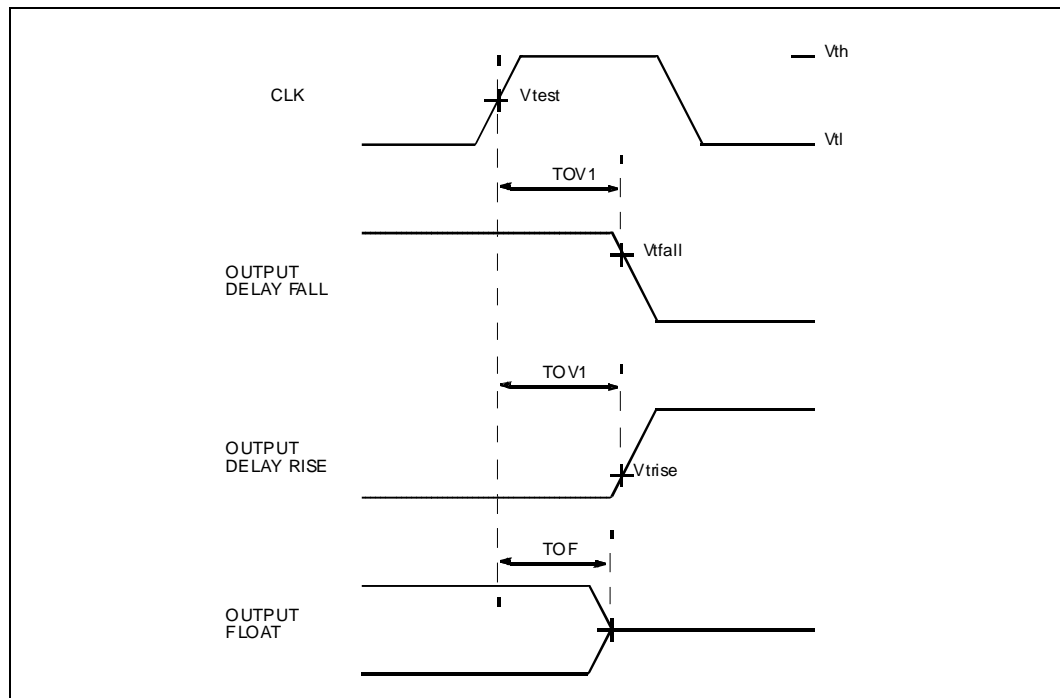


Figure 12. Input Timing Measurement Waveforms

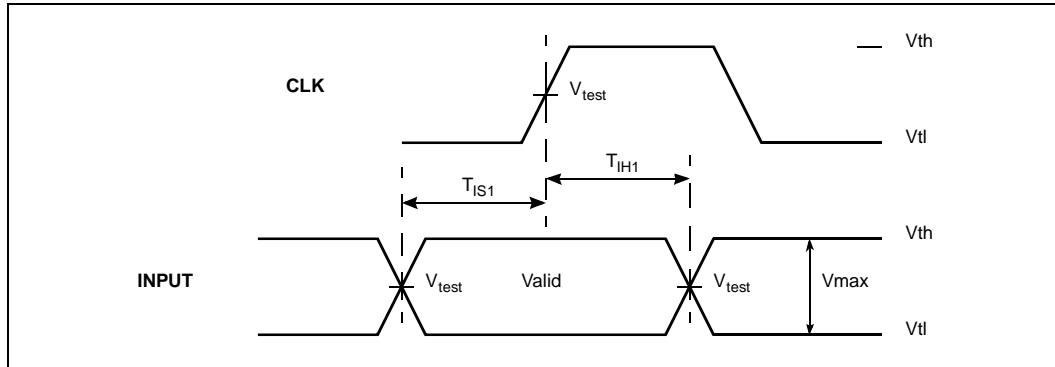


Figure 13. I²C Interface Signal Timings

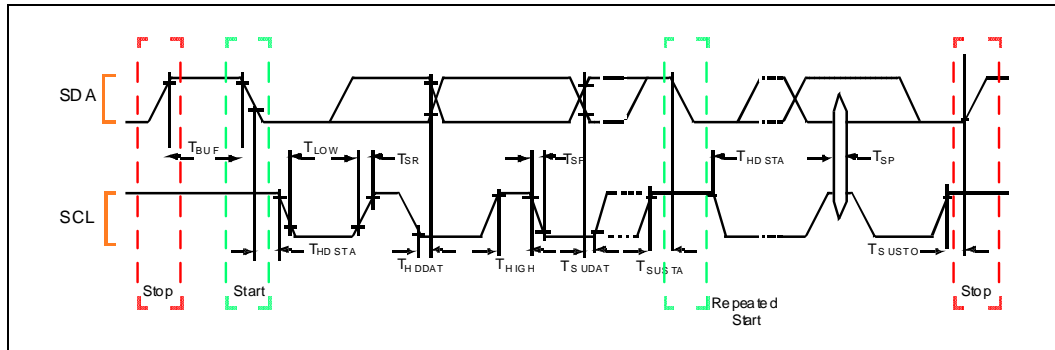




Figure 14. DDR2 SDRAM Write Timings

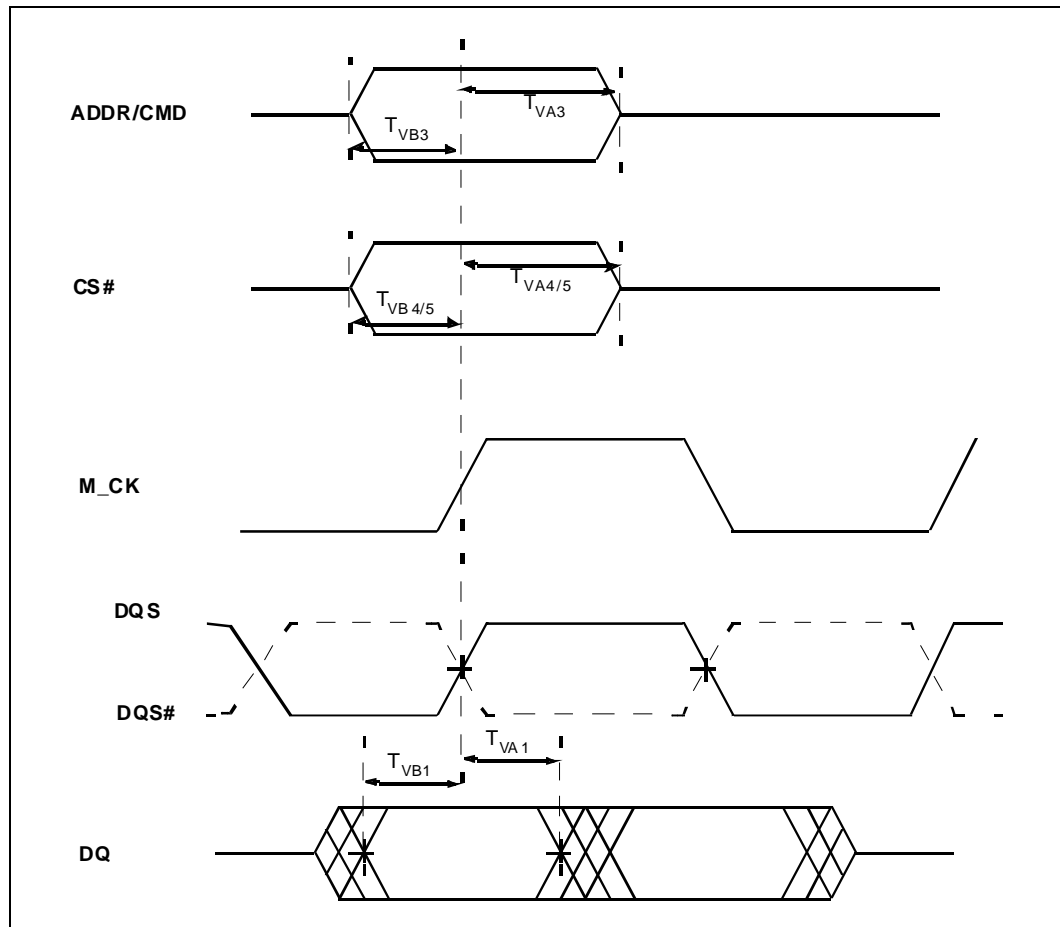


Figure 15. DQS Falling Edge Output Access Time to/from M_CK Rising Edge

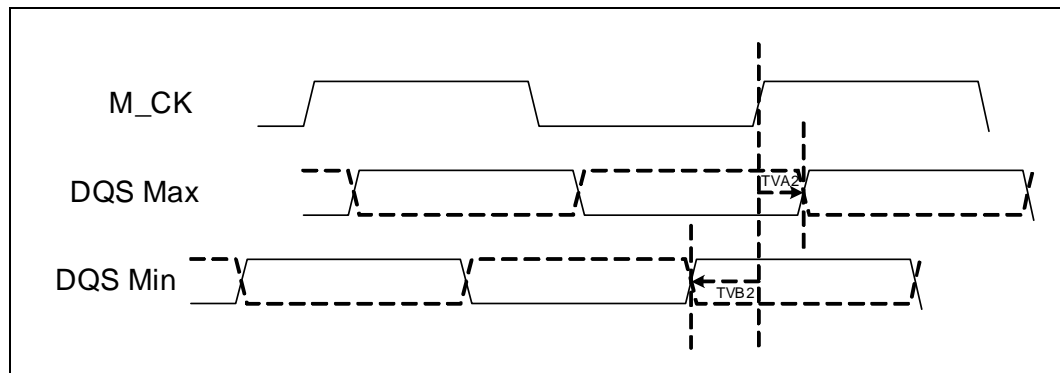


Figure 16. DDR2 SDRAM Read Timings

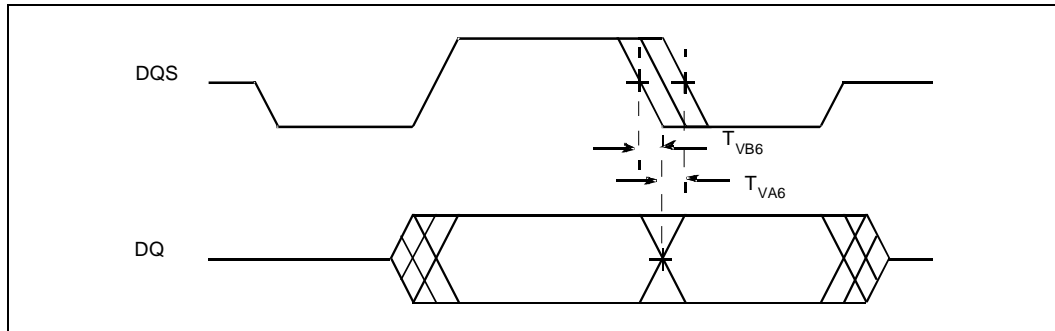


Table 32. AC Measurement Conditions

| Symbol | PCI-X | PCI | DDR2 | PBI | Units | Notes |
|-------------|------------------|------------------|-----------------|-----|-------|-------|
| V_{th} | $0.6V_{CC3P3}$ | $0.6V_{CC3P3}$ | $M_VREF+0.250$ | 2.0 | V | |
| V_{tl} | $0.25V_{CC3P3}$ | $0.2V_{CC3P3}$ | $M_VREF-0.250$ | 0.8 | V | |
| V_{test} | $0.4V_{CC3P3}$ | $0.4V_{CC3P3}$ | $0.5V_{CC1P8}$ | 1.5 | V | |
| V_{trise} | $0.285V_{CC3P3}$ | $0.285V_{CC3P3}$ | $0.5V_{CC1P8}$ | 1.5 | V | |
| V_{tfall} | $0.615V_{CC3P3}$ | $0.615V_{CC3P3}$ | $0.5V_{CC1P8}$ | 1.5 | V | |
| V_{max} | $0.35V_{CC3P3}$ | $0.4V_{CC3P3}$ | 1.0 | 1.2 | V | |
| Slew Rate | 1.5 | 1.5 | 1.0 | 1.0 | V/nS | 1 |

Notes:

1. Input signal slew rate is measured between V_{il} and V_{ih}

Figure 17. AC Test Load for all Signals Except PCI, PCI-Express and DDR2 and Storage PHY

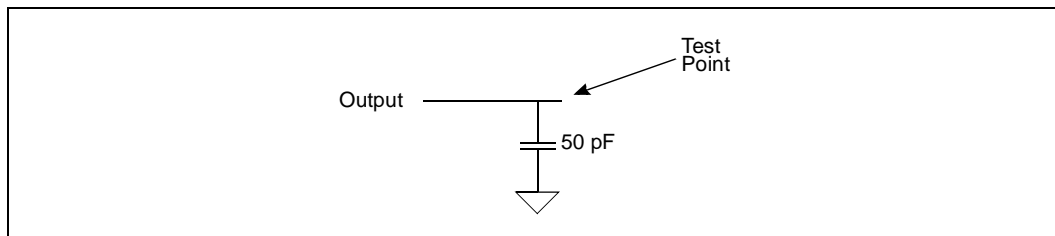


Figure 18. AC Test Load for DDR2 SDRAM Signals

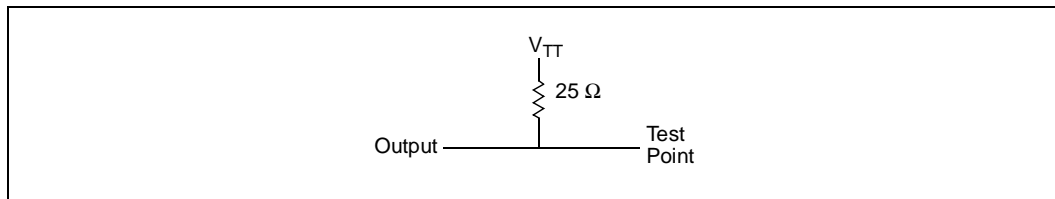




Figure 19. PCI/PCI-X $T_{OV(max)}$ Rising Edge AC Test Load

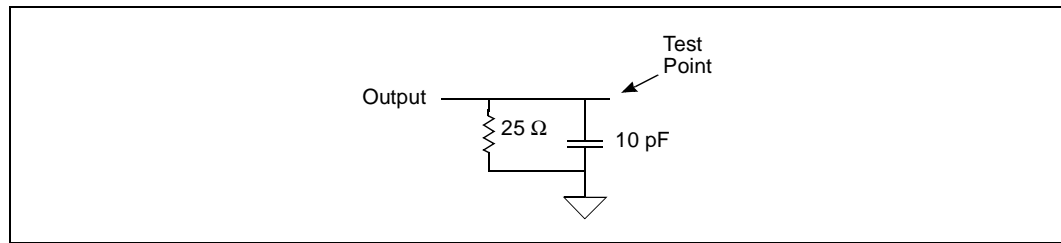


Figure 20. PCI/PCI-X $T_{OV(max)}$ Falling Edge AC Test Load

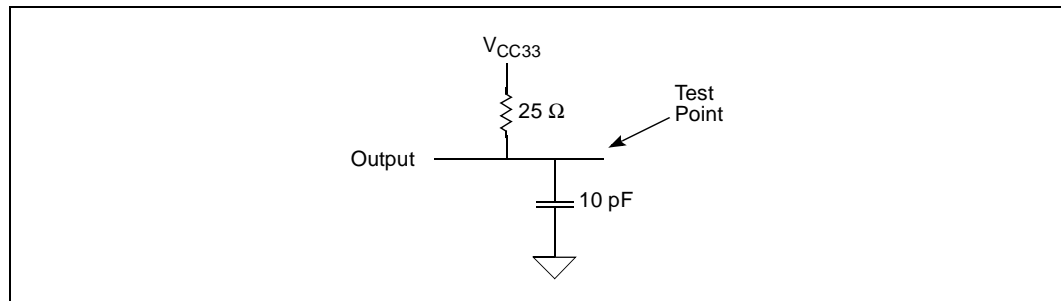


Figure 21. PCI/PCI-X $T_{OV(min)}$ AC Test Load

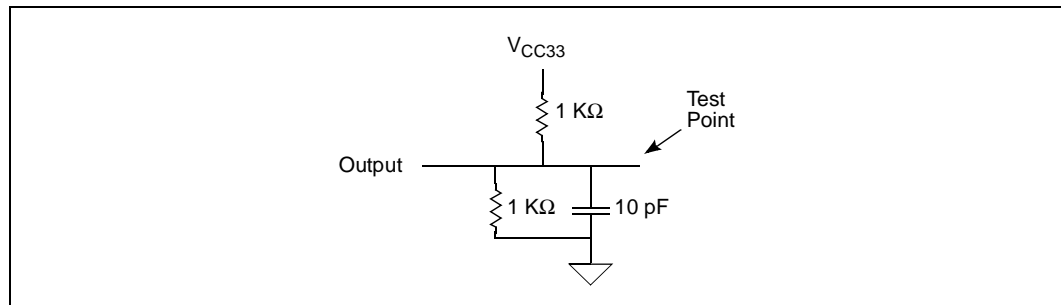


Figure 22. Transmitter Test Load (100 ohm diff Load)

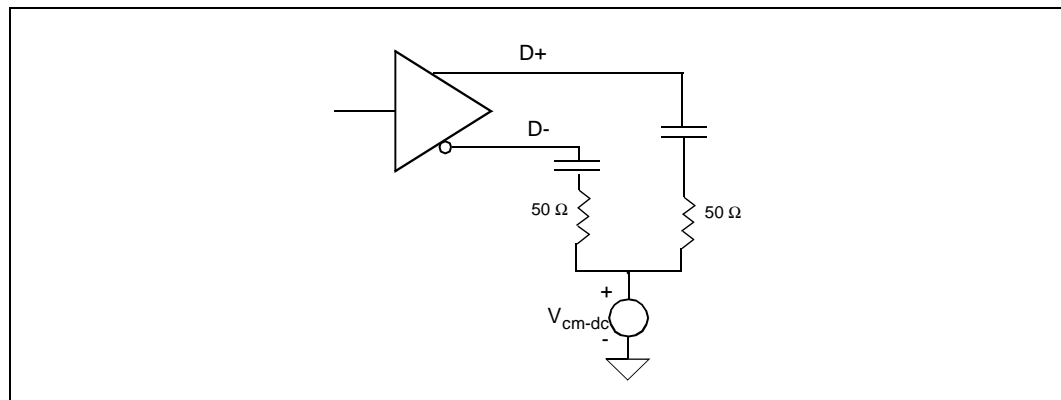


Figure 23. Transmitter Eye Diagram

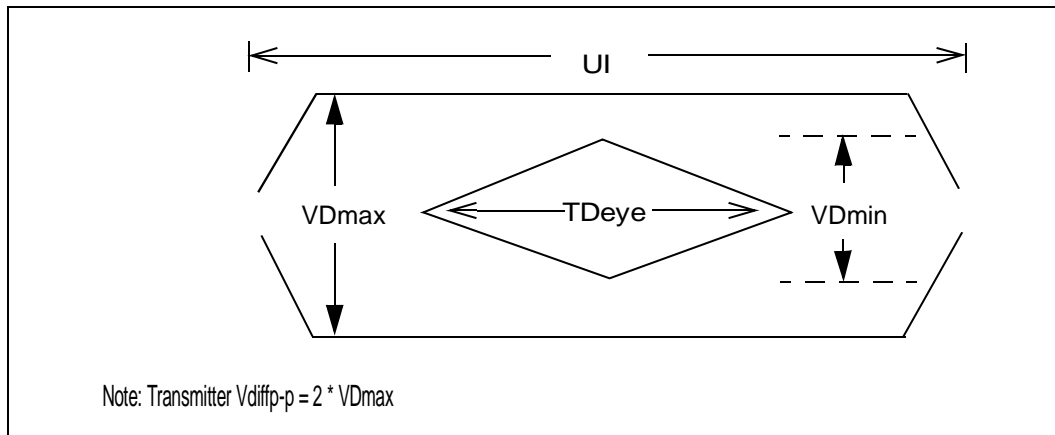


Figure 24. Receiver Eye Opening (Differential)

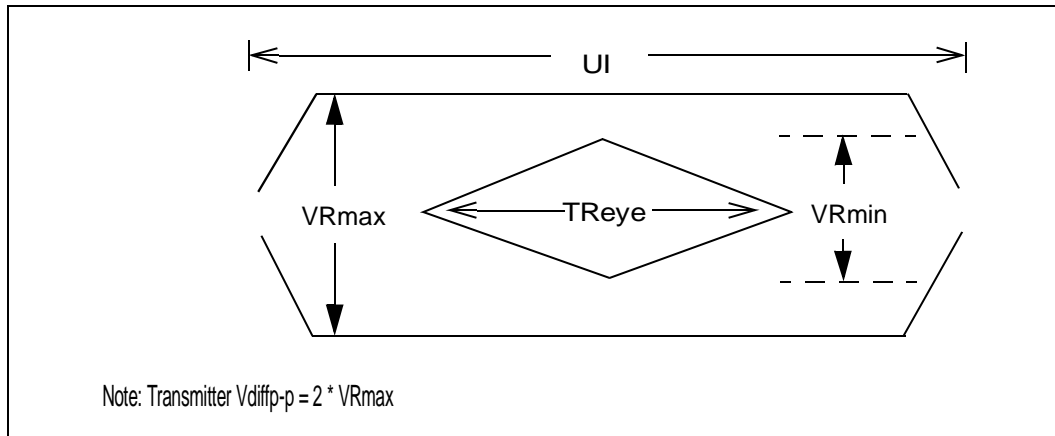




Figure 25. PBI Output Timings

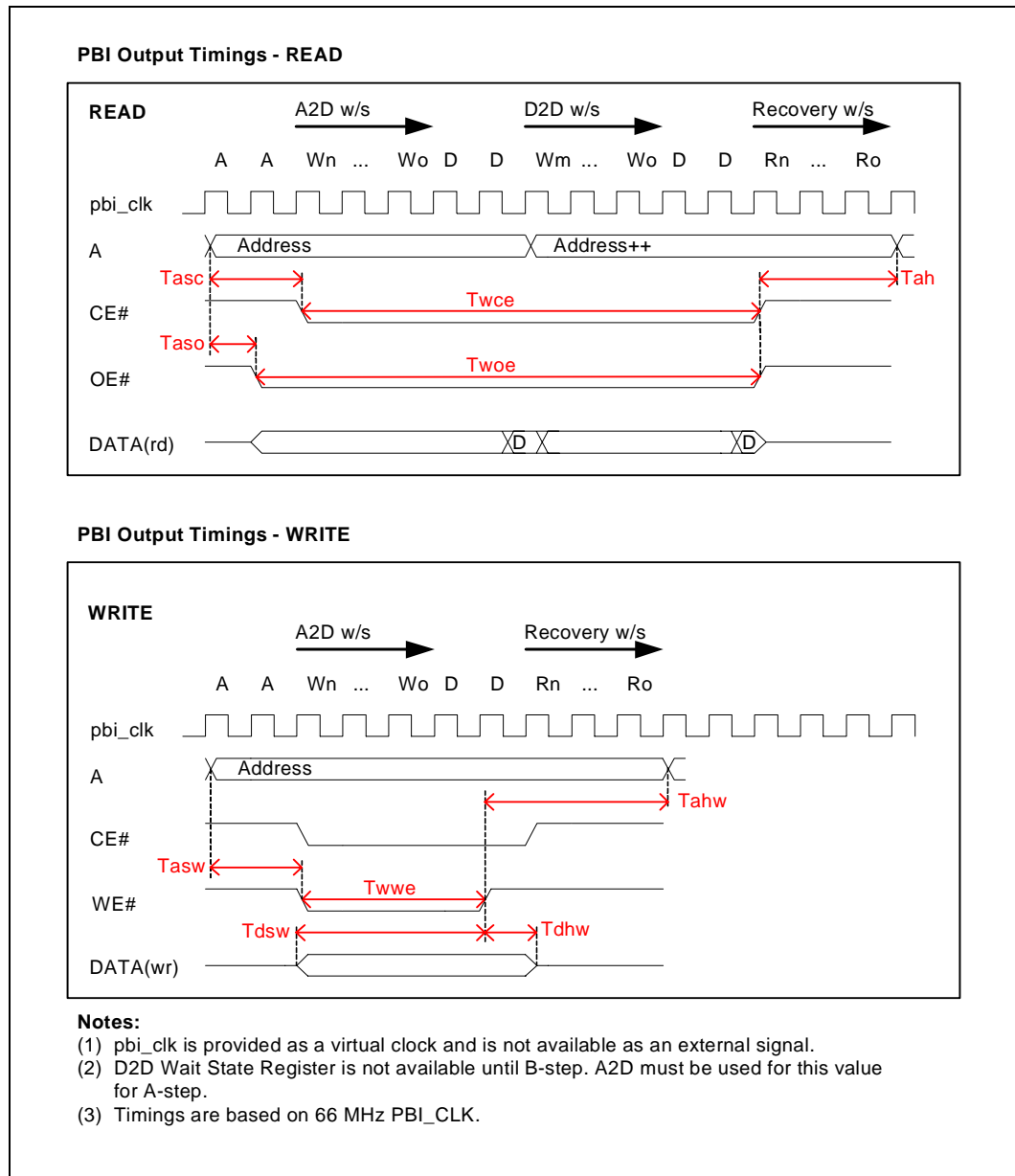
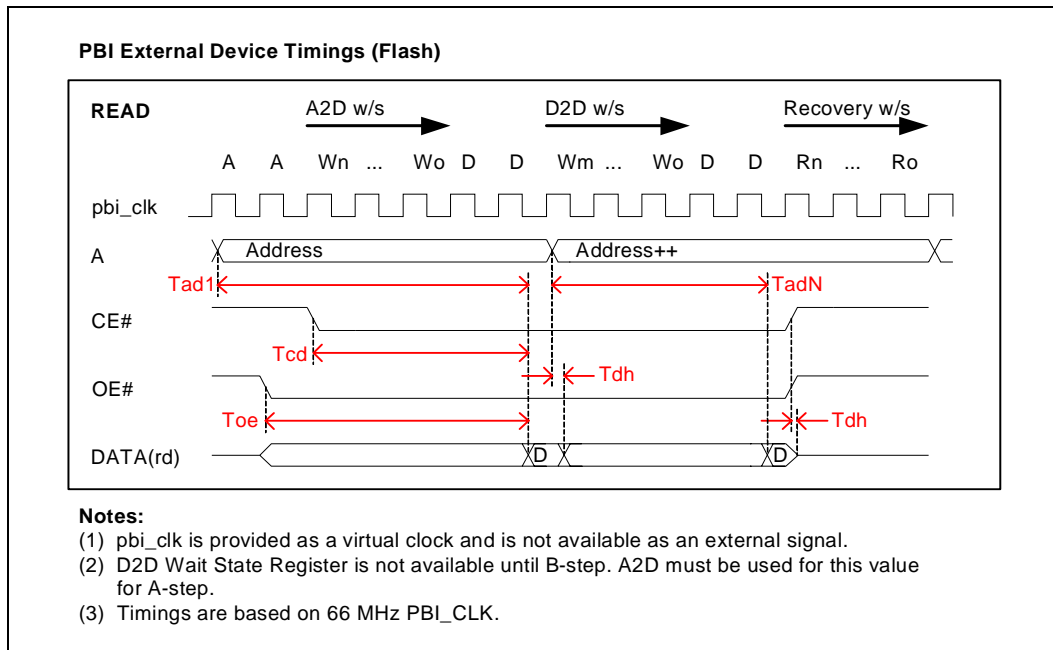


Figure 26. PBI External Device Timings (Flash)





4.5 Storage Interface Electrical Specifications

Table 33. Storage Interface Reference Clock Electrical Characteristics [S_CLKP0/S_CLKN0]

| Parameter | Limit | | | Unit | Condition |
|--|---------------------------|-------------------------|---------------------------|---------------|--|
| | Min. | Typ. | Max. | | |
| S_CLKP0/S_CLKN0 Differential Input voltage | 250 | 350 | 1000 | mV diff-pk | |
| S_CLKP0/S_CLKN0 Input Common Mode Voltage | $V_{CC1P8S} \times 0.665$ | $V_{CC1P8S} \times 0.7$ | $V_{CC1P8S} \times 0.735$ | V | |
| S_CLKP0/S_CLKN0 Input Bias Voltage | $V_{CC1P8S}/2 - 100$ mV | $V_{CC1P8S}/2$ | $V_{CC1P8S}/2 + 100$ mV | V | This is the voltage to which both S_CLKP0/S_CLKN0 are internally biased. |
| S_CLKP0/S_CLKN0 Input Clock Frequency | 150 - 100 ppm | 150 | 150 + 100 ppm | MHz | 1.5G, 3G |
| | 125 - 100 ppm | 125 | 125 + 100 ppm | | 1G, 1.5G, 2G, 3G, 4G |
| S_CLKP0/S_CLKN0 Duty Cycle | 45 | | 55 | % | |
| S_CLKP0/S_CLKN0 Rise and Fall Ttime | | 0.35 | 0.55 | nS | 20% to 80% |
| S_CLKP0/S_CLKN0 Input Jitter | | | 2 | pS rms | 10 KHz–20 MHz bandwidth |
| S_CLKP0/S_CLKN0 Differential Input Resistance | 80 | 100 | 120 | Ω | |
| S_CLKP0/S_CLKN0 Differential Input Capacitance | | 1.5 | | pF | |

Notes:

1. S_CLKP0/S_CLKN0 are AC coupled with a 100 nF capacitor.
2. S_CLKP0/S_CLKN0 are driven from $100 \pm 5\% \Omega$ differential source

Table 34. Storage Interface Transmitter Output Electrical Characteristics [S_TXP[7:0] S_TXN[7:0]]

| Parameter | Limit | | | Unit | Condition |
|--|-------|------|------|-------------|---------------------------|
| | Min. | Typ. | Max. | | |
| S_TXP [7:0] S_TXN [7:0] Differential Output Voltage | 400 | 500 | 600 | mV pk-pk | SATA Gen 1i, Gen 1m |
| | 800 | | 1600 | | SATA Gen 1x, Gen 2x |
| | 400 | | 700 | | SATA Gen 2i, Gen 2m |
| | 400 | | 1600 | | SAS (including emphasis) |
| S_TXP [7:0] S_TXN [7:0] De-emphasis | 0 | | 44 | % | See Figure 27 on page 88. |
| S_TXP [7:0] S_TXN [7:0] Differential Output Rise & Fall Time | 47 | | 130 | pS | |
| S_TXP [7:0] S_TXN [7:0] Differential Output Impedance | 85 | 100 | 115 | Ω | |
| S_TXP [7:0] S_TXN [7:0] Singled Ended Impedance | | 40 | | Ω | |

Notes:

1. Transmitter outputs are AC coupled with a 10 nF capacitor.

Figure 27. Maximum Amplitude

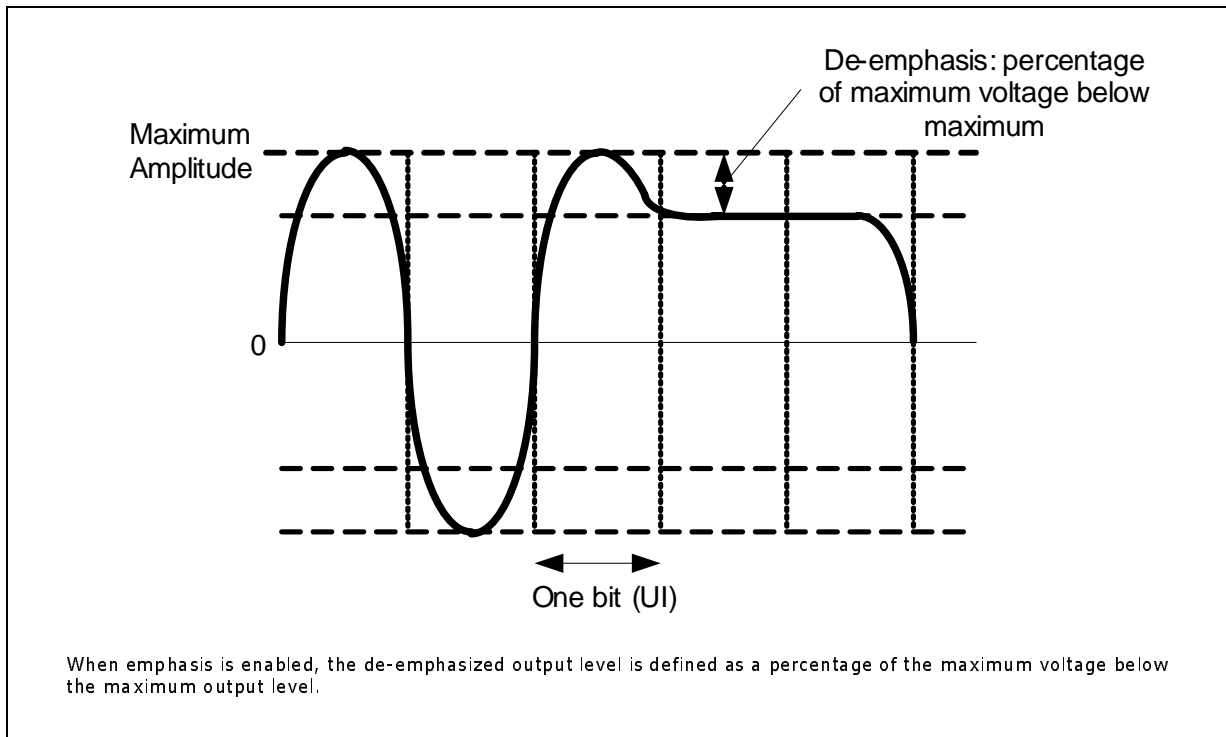




Table 35. Storage Interface Receiver Input Electrical Characteristics [S_RXP[7:0] S_RXN[7:0]]

| Parameter | Limit | | | Unit | Condition |
|--|-------|------|------|-------------|--------------------------|
| | Min. | Typ. | Max. | | |
| S_RXP [7:0] S_RXN [7:0] Differential Input Voltage | 325 | | 600 | mV pk-pk | SATA Gen 1i |
| | 240 | | 600 | | SATA Gen 1m |
| | 275 | | 1600 | | SATA Gen 1x, 2x |
| | 275 | | 750 | | SATA Gen 2i |
| | 240 | | 750 | | SATA Gen 2m |
| | 275 | | 1600 | | SAS (including emphasis) |
| S_RXP [7:0] S_RXN [7:0] Differential Input Impedance | 85 | 100 | 115 | Ω | |
| S_RXP [7:0] S_RXN [7:0] Common Mode Impedance | 20 | 30 | 40 | Ω | |

Notes:

- Receiver inputs are AC coupled with a 10 nF capacitor.

Figure 28. Intel® 81348 I/O Processor Storage PHY 1.2 V/1.8 V Power Sequencing System Requirements

