REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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REV																								
SHEET	22	23	24	25	26	27	28	29	30	31	32	33												
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY

CHECKED BY

APPROVED BY

DRAWING APPROVAL DATE
16 AUGUST 1989

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, BUS CONTROLLER REMOTE TERMINAL MULTI-PROTOCOL, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89501

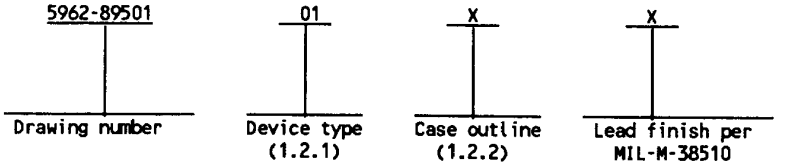
SHEET 1

DESC FORM 193
SEP 87

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT1553 BCRTMP	Bus controller remote terminal multi-protocol

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	P-AG (145-pin, 1.480" x 1.480" x .345"), pin grid array package
Y	See figure 1 (132-terminal, .965" x .965" x .105"), leaded chip carrrier package with unformed leads

1.3 Absolute maximum ratings.

Supply voltage range	-0.3 V to +7.0 V
DC input/dc output voltage range (V_{IN})	-0.3 V to (VDD +0.3 V)
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	300 mW
Maximum junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (O_{JC}):	
Case X	See MIL-M-38510, appendix C
Case Y	12°C/W
Latchup immunity (I_{LU})	±150 mA

1.4 Recommended operating conditions.

Supply voltage (VDD)	4.5 V to 5.5 V
DC input voltage	0 V to VDD
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le VDD \le 5.5\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A sub-groups	Limits		Unit
				Min	Max	
Low level input voltage TTL inputs	V_{IL}		1,2,3		0.8	V
High level input voltage TTL inputs	V_{IH}		1,2,3,	2.0		V
Input leakage current TTL inputs Inputs with pull up resistors Inputs with pull up resistors	I_{IN}	V_{IN} = VDD or VSS V_{IN} = VDD V_{IN} = VSS	1,2,3	-1 -1 -550	1 1 -80	µA µA µA
Low level output voltage TTL outputs	V_{OL}	I_{OL} = 3.2 mA	1,2,3		0.4	V
High level output voltage TTL outputs	V_{OH}	I_{OH} = -400 µA	1,2,3	2.4		V
Three-state output leakage current TTL outputs	I_{OZ}	V_{OH} = VDD or VSS	1,2,3		±10	µA
Short circuit output current 1/ 2/	I_{OS}	VDD = 5.5 V, V_O = VDD VDD = 5.5 V, V_O = 0 V	1,2,3	 -100	100	mA mA
Average operating current 1/	I_{DD}	F = 12 MHz, C_L = 50 pF 4/	1,2,3		3/ 50	mA
Quiescent current 4/	Q_{IDD}		1,2,3		3	mA
Input capacitance	C_{IN}	See 4.3.1c	4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c	4		15	pF
Bidirectional capacitance	C_{IO}	See 4.3.1c	4		20	pF
Functional tests		See 4.3.1d	7,8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ VDD ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A sub-groups	Limits		Unit
				Min	Max	
$\overline{DMACK}$(L) to $\overline{DMAR}$ high impedance 1/	t_{SHL1}	See figure 4 Burst DMA timing	9,10,11	0	10	ns
$\overline{DMAG}$(L) to $\overline{DMACK}$(L) 5/	t_{PHL1}		9,10,11	0	45	ns
$\overline{DMAG}$(L) to $\overline{TSCTL}$(L) 1/	t_{PHL2}		9,10,11	6/ 2xMCLK	6/ 4xMCLK	ns
$\overline{TSCTL}$(L) to address valid 1/	t_{PZL1}		9,10,11	0	40	ns
$\overline{RWR}$/$\overline{RRD}$(H) to $\overline{DMACK}$(H)1/	t_{HLH2}		9,10,11	7/ THMC1-10	7/ THMC1+10	ns
$\overline{TSCTL}$(L) to $\overline{RWR}$/$\overline{RRD}$(L)1/	t_{PHL3}		9,10,11	6/ MCLK-20	6/ MCLK+20	ns
$\overline{DMAG}$(L) to $\overline{DMAG}$(H) 1/	t_{PW2}		9,10,11	6/ MCLK	6/ 6xMCLK	ns
$\overline{DMAR}$(L) to BURST(H) 1/ 8/	t_{OOZL1}		9,10,11	0	10	ns
$\overline{DMAR}$(L) to $\overline{DMAG}$(L) 1/	t_{PHL4}		9,10,11	0 9/ 0 10/	3.5 (1.9) 1.9 (0.8)	µs µs
Address valid to $\overline{RRD}$(L) (Address setup) 1/	t_{SHL1}	See figure 4 DMA read timing	9,10,11	11/ THMC2-20	11/ THMC2	ns
$\overline{RRD}$(L) to $\overline{RRD}$(H) 1/	t_{PW1}		9,10,11	6/ MCLK-5	6/ MCLK+5	ns
$\overline{RRD}$(H) to address high impedance 1/ (address hold)	t_{HLZ2}		9,10,11	7/ THMC1-10	7/ THMC1	ns
$\overline{RRD}$(H) to data high impedance 1/ (data hold)	t_{HLZ1}		9,10,11	5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le VDD \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A sub-groups	Limits		Unit
				Min	Max	
Data valid to $\overline{RRD}$(H) (data setup) 1/	t_{SLH1}	See figure 4 DMA read timing	9,10,11	40		ns
MCLK(H) to MCLKD2(H)	t_{PLH1}		9,10,11	0	40	ns
MCLK(H) to TSCTL/MEMSCO(L) 1/	t_{PLH2}		9,10,11	0	40	ns
MCLK(H) to $\overline{RRD}$(L)	t_{IOHL1}		9,10,11	0	60	ns
Address valid to $\overline{RWR}$(L) (address setup) 1/	t_{SHL1}	See figure 4 DMA write timing	9,10,11	11/ THMC2-20	11/ THMC2	ns
$\overline{RWR}$(L) to data valid	t_{OOZL1}		9,10,11	0	30	ns
$\overline{RWR}$(H) to data high 1/ impedance (data hold)	t_{HLZ1}		9,10,11	7/ THMC1-20	7/ THMC1	ns
$\overline{RWR}$(H) to address high impedance 1/ (address hold)	t_{HLZ2}		9,10,11	7/ THMC1-20	7/ THMC1	ns
$\overline{RWR}$(L) to $\overline{RWR}$(H) 1/	t_{PW1}		9,10,11	6/ MCLK-5	6/ MCLK+5	ns
MCLK(H) to MCLKD2(H)	t_{PLH1}		9,10,11	0	40	ns
MCLK(H) to TSCTL/MEMCSO(L) 1/	t_{PLH2}		9,10,11	0	40	ns
MCLK(H) to $\overline{RWR}$(L)	t_{IOHL1}		9,10,11	0	60	ns
Address valid to data valid 1/ 12/	t_{OOZH2}	See figure 4 Register read timing	9,10,11		80	ns
$\overline{RD}$+$\overline{CS}$(H) to data high impedance 1/ (data hold)	t_{HLH2}		9,10,11	5	50	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ VDD ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{RD}$+$\overline{CS}$(L) to data valid (data access) 12/	t_{OOZH1}	See figure 4 Register read timing	9,10,11		60	ns
$\overline{RD}$+$\overline{CS}$(H) to address 1/ invalid (address hold)	t_{HLH1}		9,10,11	5		ns
$\overline{RD}$+$\overline{CS}$(L) to $\overline{RD}$+$\overline{CS}$(H) 1/	t_{PW1}		9,10,11	60		ns
$\overline{RD}$+$\overline{CS}$(H) to $\overline{RD}$+$\overline{CS}$(L) 1/	t_{PW2}		9,10,11	80		ns
Address valid to $\overline{WR}$+$\overline{CS}$(L) (address setup) 1/	t_{SHL1}	See figure 4 Register write timing	9,10,11	60		ns
Data valid to $\overline{WR}$+$\overline{CS}$(H) (data setup) 1/ 13/	t_{SLH1}		9,10,11	60		ns
$\overline{WR}$+$\overline{CS}$(L) to $\overline{WR}$+$\overline{CS}$(H) 1/	t_{PW1}		9,10,11	60		ns
$\overline{WR}$+$\overline{CS}$(H) to data invalid (data hold) 1/	t_{HLH1}		9,10,11	10		ns
$\overline{WR}$+$\overline{CS}$(H) to address 1/ invalid (address hold)	t_{HLH2}		9,10,11	10		ns
$\overline{WR}$+$\overline{CS}$(H) to $\overline{WR}$+$\overline{CS}$(L) 1/	t_{PW2}		9,10,11	80		ns
$\overline{RD}$(L) to $\overline{RRD}$(L)	t_{PLH1}	See figure 4 Dual port interface timing	9,10,11	0	30	ns
$\overline{WR}$(L) to $\overline{RWR}$(L)	t_{PLH2}		9,10,11	0	30	ns
$\overline{MEMCSI}$(L) to $\overline{MEMCSO}$(L)	t_{PLH3}		9,10,11	0	30	ns
$\overline{MEMWIN}$(H) to DMA activity 1/ 14/ 15/	t_{OOLH1}	See figure 4 Memory window timing	9,10,11	9		µs

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{DD} \le 5.5\ V$, $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{MEMWIN}$(L) to $\overline{MEMWIN}$(H) 1/	t_{PW1}	See figure 4 Memory window timing	9,10,11	0	16/	µs
Data word to DMA activity 1/ 14/ 15/	t_{PZL1}		9,10,11	0	4	µs
$\overline{DMAG}$(L) to $\overline{DMAGO}$(L) 1/ 17/	t_{PHL1}	See figure 4 Arbitration when $\overline{DMAG}$ is asserted before arbitration timing	9,10,11	0	30	ns
$\overline{DMACK}$(L) to $\overline{DMAR}$ high 1/ impedance	t_{SHL1}		9,10,11	0	10	ns
MCLK(H) to MCLKD2(H)	t_{PLH2}		9,10,11	0	40	ns
$\overline{LGLEN}$(L) to $\overline{LGLEN}$(H) 1/	t_{PW1}	See figure 4 Legalization bus timing	9,10,11	750		ns
$\overline{LGLEN}$(L) to legalization bus valid 1/	t_{HLH1}		9,10,11		200	ns
LGCMD(H) to $\overline{LGLEN}$(H) (setup time) 1/	t_{SLH1}		9,10,11		100	ns
$\overline{LGLEN}$(H) to LGLCMD invalid (hold time) 1/	t_{HLZ1}		9,10,11	0		
Legalization bus valid to LGLCMD(H) 1/ (setup time)	t_{HLH2}		9,10,11		450	
$\overline{MEMWIN}$(H) to $\overline{DMAR}$(L) 1/	t_{OOLH2}	See figure 4 Interrupt log list entry operation timing	9,10,11	9		µs
$\overline{TSCTL}$(H) to $\overline{STDINTL}$(L) 1/	t_{OOLH1}		9,10,11		1	µs
$\overline{STDINTP}$(L) to $\overline{STDINTP}$(H) 1/	t_{PW1}		9,10,11	320	340	ns
$\overline{DMACK}$(L) to $\overline{RWR}$(L) 1/	t_{OOHL1}		9,10,11	6/ 3xMCLK-10	6/ 5xMCLK	ns
$\overline{DMAG}$(L) to $\overline{STDINTL}$(L) 1/	t_{OOHL2}		9,10,11	6/ 8xMCLK+0.5	6/ 10xMCLK+1	µs

See footnotes on next page.

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1/ Guaranteed to the limits specified in table I, if not tested.

2/ Not more than one output may be shorted at a time for a maximum duration of one second.

3/ Includes current through input pull up. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to to handle a large current surge.

4/ All inputs with internal pull ups should be left floating. All other inputs should be tied high or low.

5/ $\overline{\text{DMAG}}$ must be asserted at least 45ns prior to the rising edge of MCLKD2 in order to be recognized for the next MCLKD2 cycle. If $\overline{\text{DMAG}}$ is not asserted at least 45ns prior to the rising edge of MCLKD2, $\overline{\text{DMAG}}$ is not recognized until the following MCLKD2 cycle.

6/ MCLK = period of the memory clock cycle.

7/ THMC1 is equivalent to the positive phase of MCLK.

8/ BURST signal is for multiple-word DMA accesses.

9/ Provided MCLK = 12MHz. Number in parentheses indicates the longest $\overline{\text{DMAR}}$(L) to $\overline{\text{DMAG}}$(L) allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT response time. The number not in parentheses applies to all other circumstances.

10/ Provided MCLK = 6MHz. Number in parentheses indicates the longest $\overline{\text{DMAR}}$(L) to $\overline{\text{DMAG}}$(L) allowed during worst-case bus switching conditions in order to meet MIL-STD-1553B RT response time. The number not in parentheses applies to all other circumstances.

11/ THMC2 is equivalent to the negative phase of MCLK.

12/ User must adhere to both t_{OOZH1} and t_{OOZH2} timing constraints to ensure valid data.

13/ The data setup time when writing to register 4 (accessed by $A_3 = 0$, $A_2 = 1$, $A_1 = 0$, $A_0 = 0$) must be 15 ns with respect to the falling edge of WR + CS, instead of 60 ns with respect to the rising edge of WR + CS.

14/ DMA may occur as soon as 9 μs after $\overline{\text{MEMWIN}}$ is deasserted.

15/ If bit-time 11 in the data word occurs before DMA activity is complete (i.e. $\overline{\text{DMAR}}$(L) to $\overline{\text{DMACK}}$(H), MEMWIN signal is not generated.

16/ The pulse width = (11 μs - t_{DMA} - t_{PZL1}) where t_{DMA} is the time to complete DMA activity

17/ When $\overline{\text{DMAG}}$ is asserted before $\overline{\text{DMAR}}$, the $\overline{\text{DMAG}}$ signal passes through the device as $\overline{\text{DMAGO}}$.

Case Y

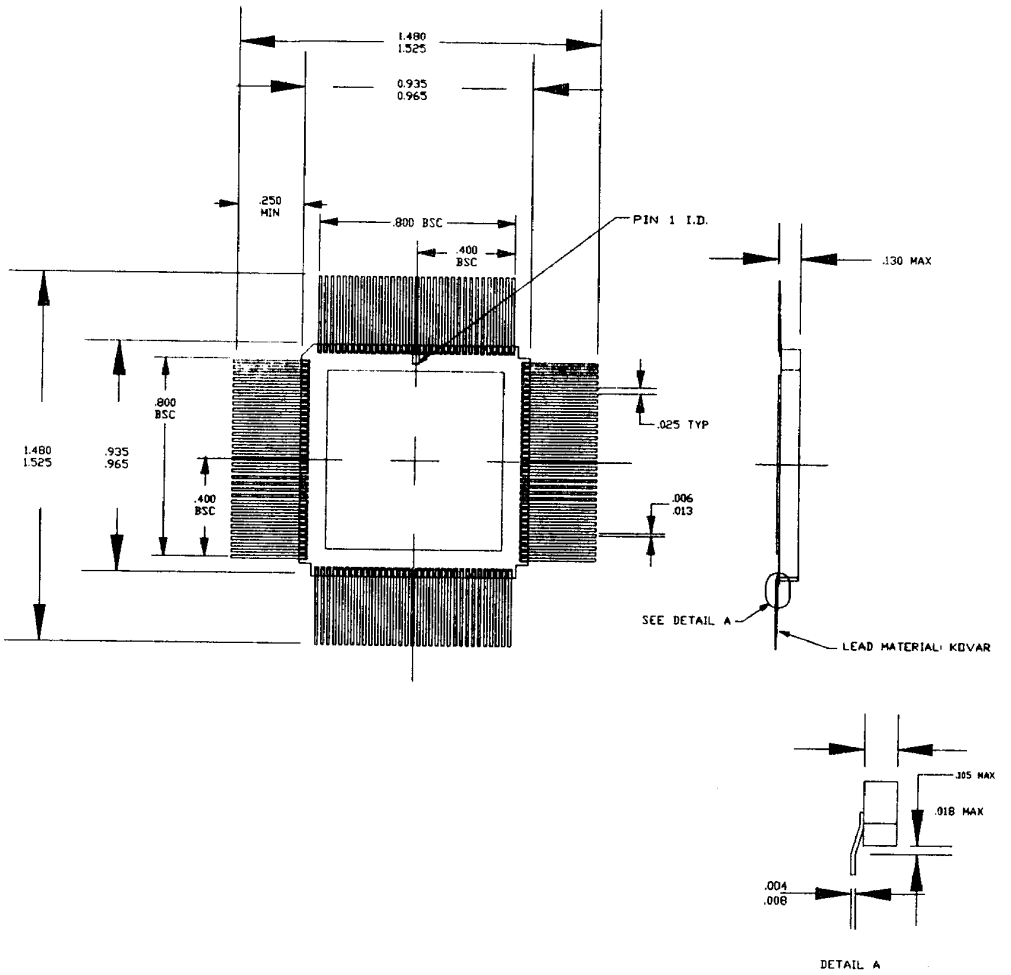

FIGURE 1. Dimensions and configurations.

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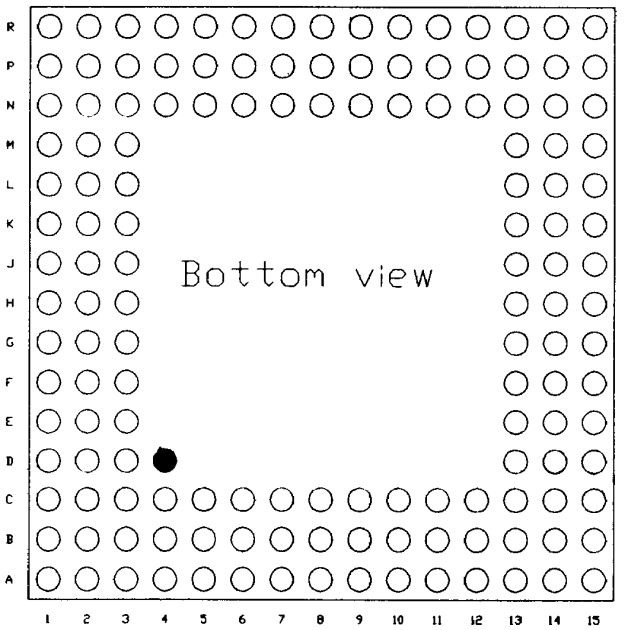
Case X



A1 - NC	B1 - NC	C1 - LGL9	N1 - MD02	P1 - MD06	R1 - NC	D1 - BRDCAST
A2 - LGL2	B2 - LGL5	C2 - LGL6	N2 - MD05	P2 - MD1	R2 - NC	D2 - LGL7
A3 - D14	B3 - LGL1	C3 - LGL4	N3 - MD0	P3 - MD2	R3 - MD5	D3 - NC
A4 - D13	B4 - D15	C4 - LGL3	N4 - NC	P4 - MD3	R4 - MD7	D4 - NC --Alignment pin
A5 - D12	B5 - NC	C5 - LGL0	N5 - MD4	P5 - MD6	R5 - NC	D13 - ACTIVE
A6 - D8	B6 - D10	C6 - D11	N6 - A0	P6 - A1	R6 - A4	D14 - BURST
A7 - D7	B7 - D9	C7 - VDD	N7 - A3	P7 - A2	R7 - A5	D15 - DMACK
A8 - D6	B8 - D5	C8 - VSS	N8 - VSS	P8 - A6	R8 - A7	E1 - NC
A9 - D4	B9 - D1	C9 - D2	N9 - VDD	P9 - A10	R9 - A8	E2 - LGL10
A10 - D3	B10 - D0	C10 - CONSTR	N10 - A12	P10 - A11	R10 - A9	E3 - LGL8
A11 - NC	B11 - EXTOVR	C11 - TIMRONB	N11 - RTA1	P11 - NC	R11 - A13	E13 - DMAGO
A12 - CHA/B	B12 - TIMRONA	C12 - NC	N12 - RTA4	P12 - RTA0	R12 - A14	E14 - NC
A13 - BCRTSEL	B13 - APINT	C13 - STDINTC	N13 - RTPTY	P13 - RTA2	R13 - A15	E15 - MCLKD2
A14 - NC	B14 - STDINTP	C14 - FBUSY	N14 - RAZ	P14 - RA0	R14 - RTA3	
A15 - NC	B15 - BUSYACK	C15 - TSCTL	N15 - RBD	P15 - NC	R15 - NC	

F1 - LGLEN	G1 - SSYSF	H1 - NC	J1 - CLK	K1 - ALTWRAP	L1 - MD00	M1 - MD01
F2 - LGLCMD	G2 - ERR	H2 - BCRTF	J2 - WRAPF	K2 - WRAPEN	L2 - NC	M2 - MD03
F3 - MC	G3 - DOMC	H3 - VDD	J3 - VSS	K3 - MRST	L3 - MD04	M3 - LOCK
F13 - DMAG	G13 - VDD	H13 - VSS	J13 - AEN	K13 - TBZ	L13 - TAZ	M13 - NC
F14 - DMAR	G14 - RWR	H14 - WR	J14 - MEMWIN	K14 - MCLK	L14 - RBZ	M14 - TA0
F15 - RRD	G15 - MEMCS0	H15 - MEMCS1	J15 - RD	K15 - CS	L15 - NC	M15 - TB0

FIGURE 2. Terminal connections.

Case Y

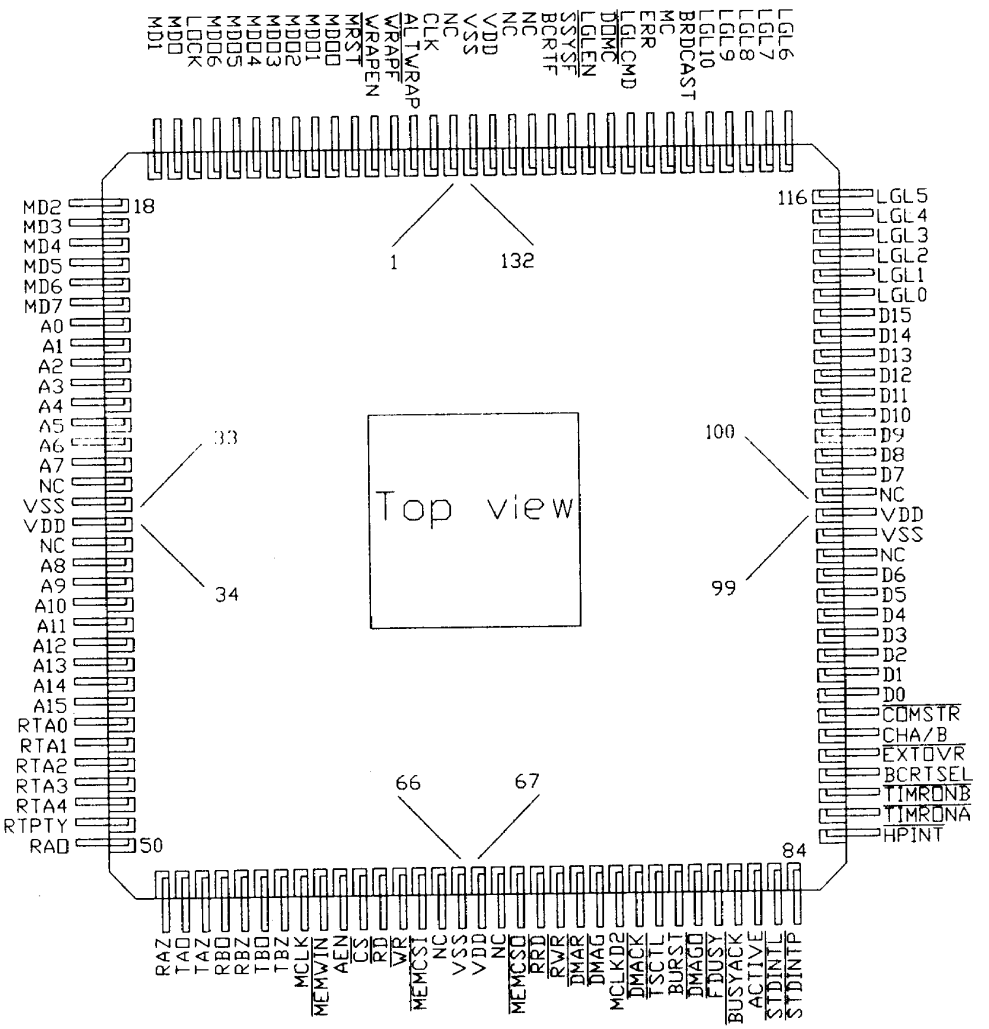


FIGURE 2. Terminal connections - Continued.

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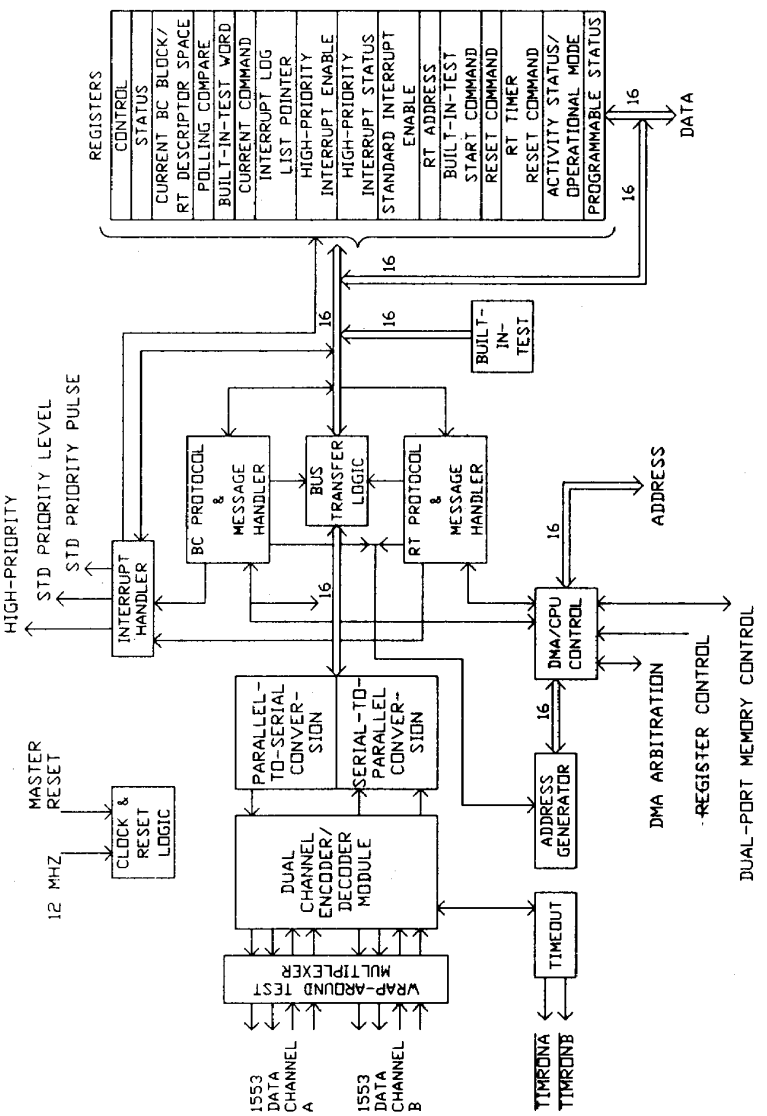

FIGURE 3. Functional block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-89501
		REVISION LEVEL	SHEET 13

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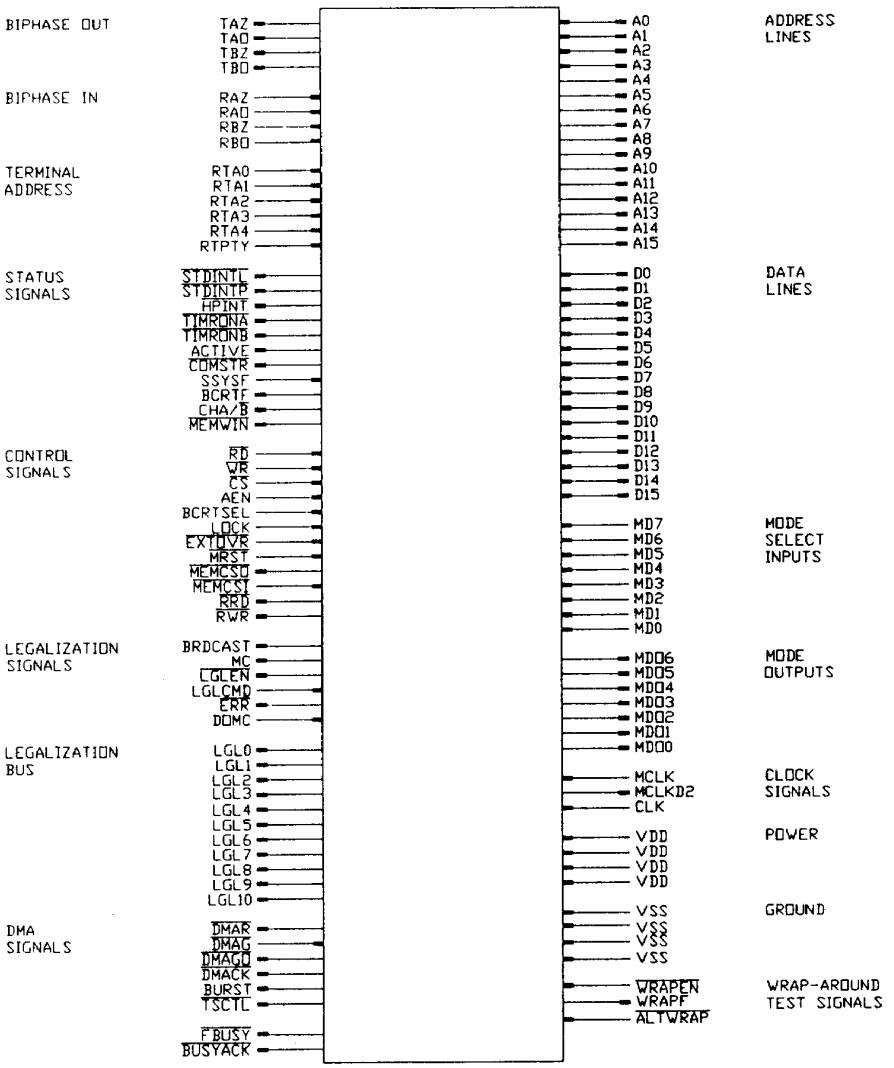
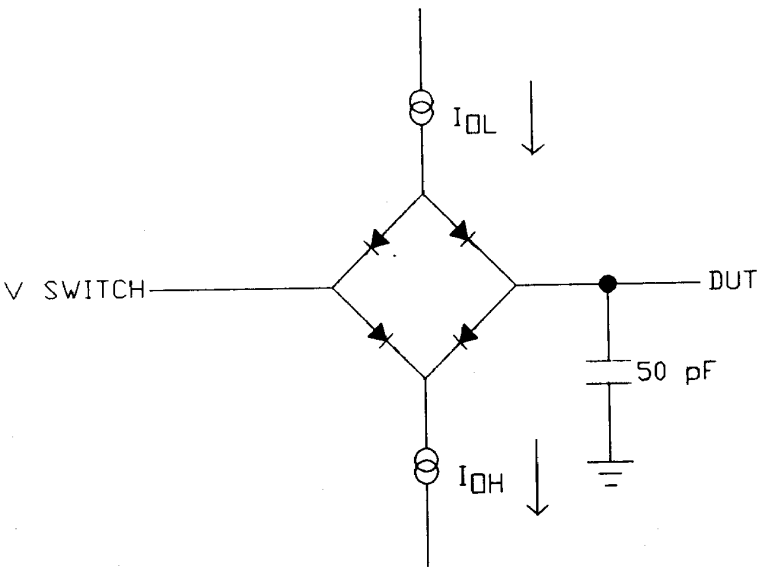


FIGURE 3. Functional block diagram - Continued.



NOTE: V switch = (V_{OL} max + V_{OH} min)/2

FIGURE 4. Switching test circuit and waveforms.

Burst DMA timing

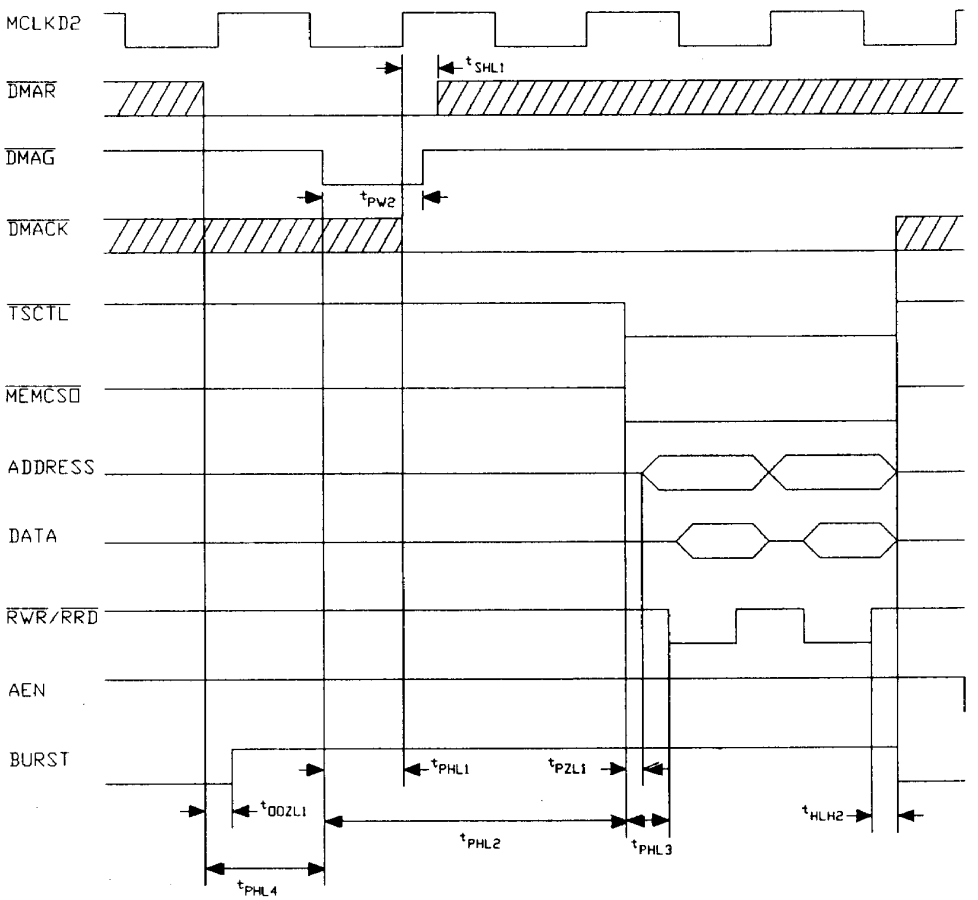


FIGURE 4. Switching test circuit and waveforms - Continued.

DMA read timing

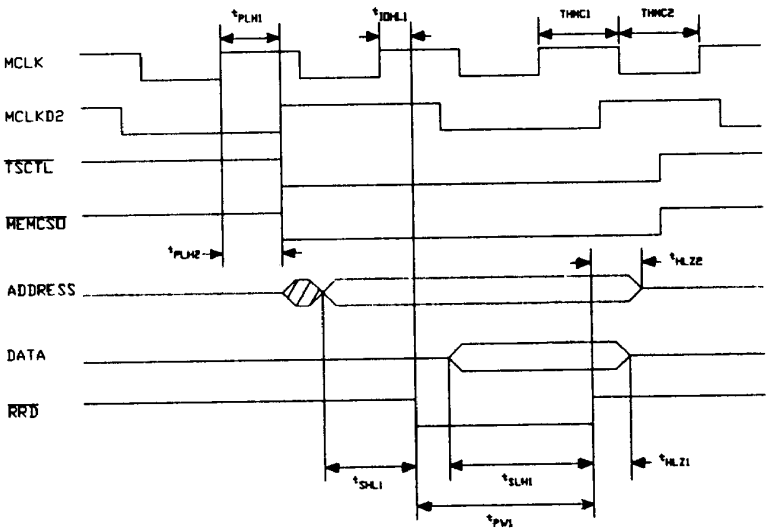


FIGURE 4. Switching test circuit and waveforms - Continued.

DMA write timing

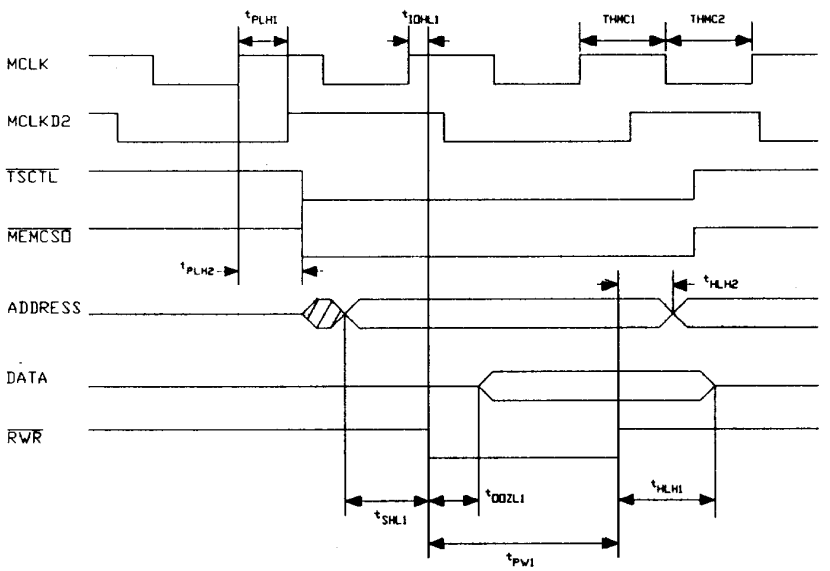
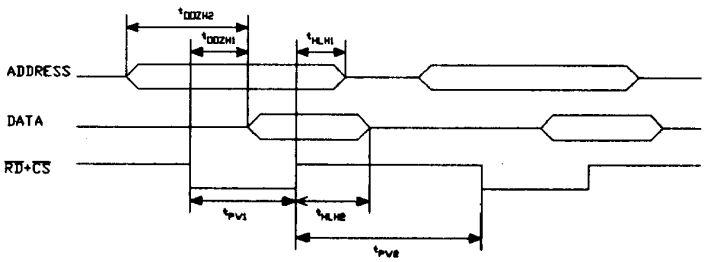


FIGURE 4. Switching test circuit and waveforms - Continued.

Register read timing



Register write timing

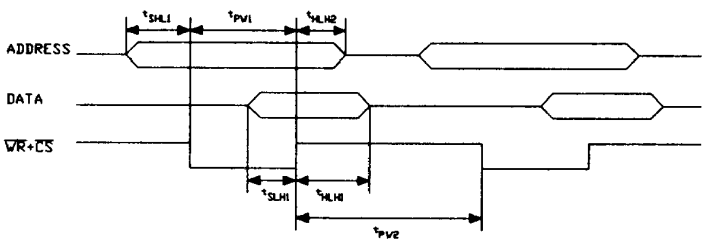


FIGURE 4. Switching test circuit and waveforms - Continued.

Dual port interface timing

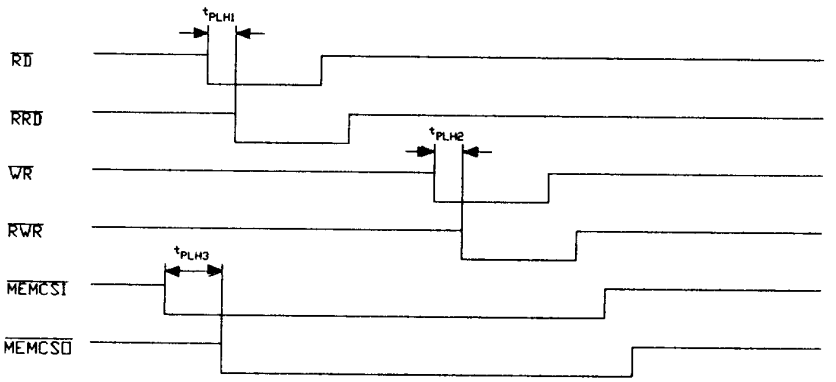


FIGURE 4. Switching test circuit and waveforms - Continued.

Memory window (RT) mode

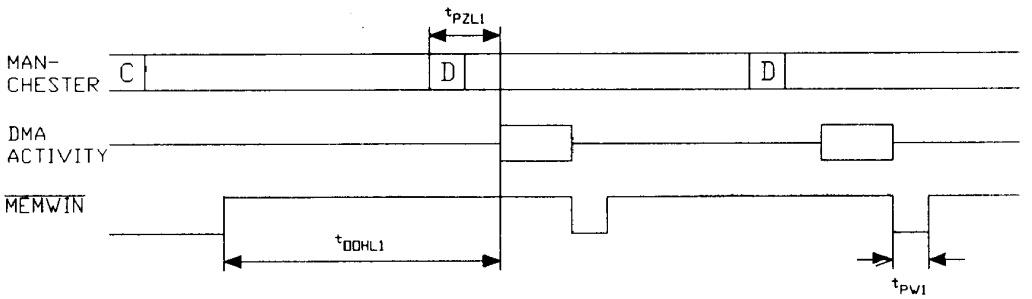


FIGURE 4. Switching test circuit and waveforms - Continued.

Arbitration when $\overline{\text{DMAG}}$ is asserted before arbitration

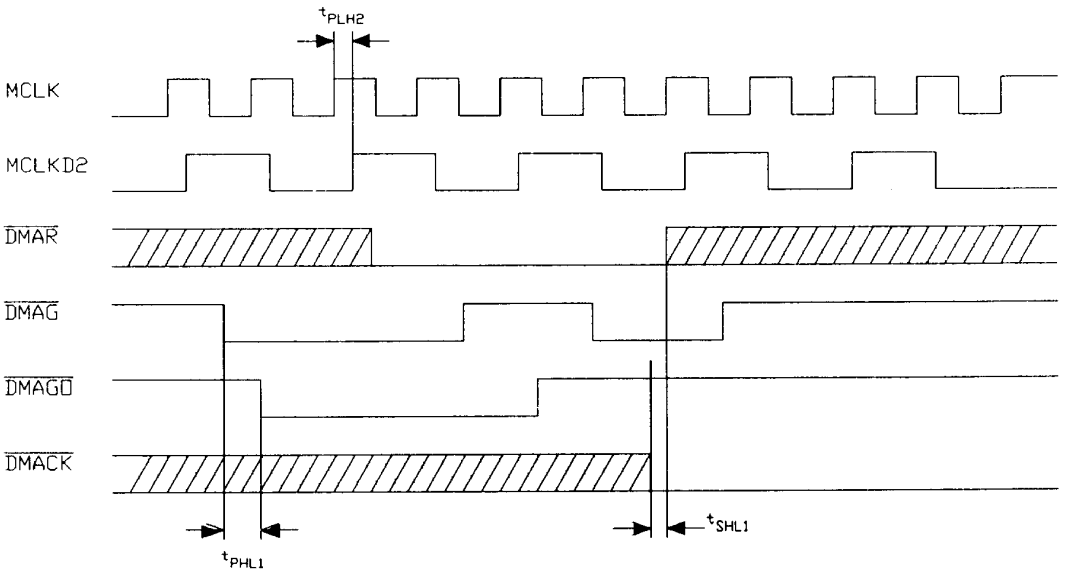


FIGURE 4. Switching test circuit and waveforms - Continued.

Legalization bus timing

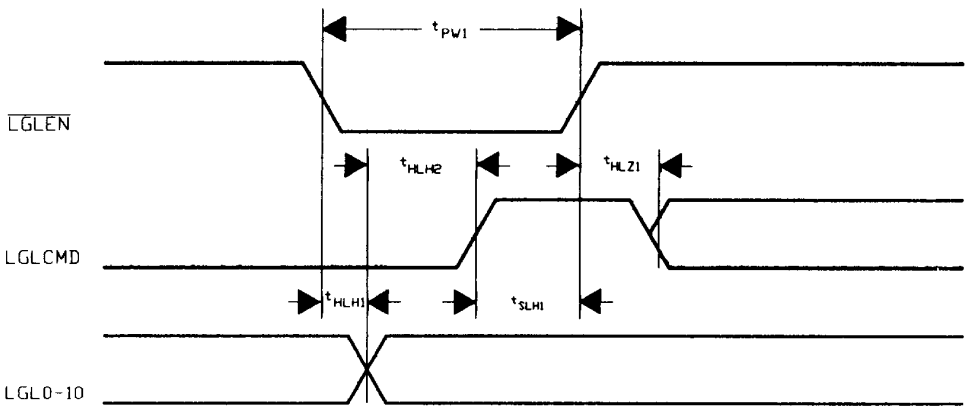


FIGURE 4. Switching test circuit and waveforms - Continued.

Interrupt log list entry operation timing

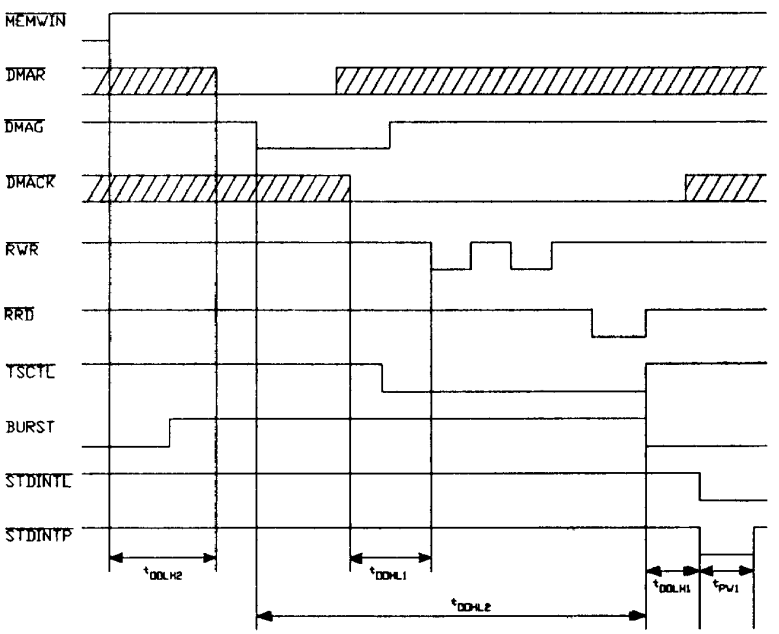


FIGURE 4. Switching test circuit and waveforms - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 or table IV, method 5010 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 or method 5010 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 or table IV method 5010 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, C_{IO} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 10 devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendor`s test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I or 5010, table IV
Interim electrical parameters (method 5004 or 5010)	- - -
Final electrical test parameters (method 5004 or 5010)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005 or 5010)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005 or 5010)	1, 2, 7, 8A

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Symbols and definitions.

Name	Pin number Cases Y	Pin number Cases X	1/ Type	1/ Active	Description
A0	24	N6	TTB		Bit 0 (LSB) of the address bus
A1	25	P6	TTB		Bit 1 of the address bus
A2	26	P7	TTB		Bit 2 of the address bus
A3	27	N7	TTB		Bit 3 of the address bus
A4	28	R6	TTB		Bit 4 of the address bus
A5	29	R7	TTO		Bit 5 of the address bus
A6	30	P8	TTO		Bit 6 of the address bus
A7	31	R8	TTO		Bit 7 of the address bus
A8	36	R9	TTO		Bit 8 of the address bus
A9	37	R10	TTO		Bit 9 of the address bus
A10	38	P9	TTO		Bit 10 of the address bus
A11	39	P10	TTO		Bit 11 of the address bus
A12	40	N10	TTO		Bit 12 of the address bus
A13	41	R11	TTO		Bit 13 of the address bus
A14	42	R12	TTO		Bit 14 of the address bus
A15	43	R13	TTO		Bit 15 of the address bus
D0	91	B10	TTB		Bit 0 (LSB) of the data bus
D1	92	B9	TTB		Bit 1 of the data bus
D2	93	C9	TTB		Bit 2 of the data bus
D3	94	A10	TTB		Bit 3 of the data bus
D4	95	A9	TTB		Bit 4 of the data bus
D5	96	B8	TTB		Bit 5 of the data bus
D6	97	A8	TTB		Bit 6 of the data bus
D7	102	A7	TTB		Bit 7 of the data bus

6.4 Symbols and definitions - Continued.

Name	Pin number Cases Y	Pin number Cases X	1/ Type	1/ Active	Description
D8	103	A6	TTB		Bit 8 of the data bus
D9	104	B7	TTB		Bit 9 of the data bus
D10	105	B6	TTB		Bit 10 of the data bus
D11	106	C6	TTB		Bit 11 of the data bus
D12	107	A5	TTB		Bit 12 of the data bus
D13	108	A4	TTB		Bit 13 of the data bus
D14	109	A3	TTB		Bit 14 of the data bus
D15	110	B4	TTB		Bit 15 of the data bus
RTA0	44	P12	TI		Remote terminal address bit 0 (LSB)
RTA1	45	N11	TI		Remote terminal address bit 1.
RTA2	46	P13	TI		Remote terminal address bit 2.
RTA3	47	R14	TI		Remote terminal address bit 3
RTA4	48	N12	TI		Remote terminal address bit 4
RTPTY	49	N13	TI		Remote terminal (address) parity
$\overline{RD}$	62	J15	TI	AL	Read
$\overline{WR}$	63	H14	TI	AL	Write
$\overline{CS}$	61	K15	TI	AL	Chip select
AEN	60	J13	TI	AH	Address enable
BCRTSEL	87	A13	TUI		BC/$\overline{RT}$ select
LOCK	15	M3	TUI	AH	Lock
$\overline{EXTOVR}$	88	B11	TUI	AL	External override
$\overline{MRST}$	7	K3	TI	AL	Master reset
$\overline{MEMCSO}$	69	G15	TO	AL	Memory chip select out
$\overline{MEMCSI}$	64	H15	TO	AL	Memory chip select in

6.4 Symbols and definitions - Continued.

Name	Pin number Cases Y	Pin number Cases X	1/ Type	1/ Active	Description
$\overline{\text{RRD}}$	70	F15	TO	AL	RAM read
$\overline{\text{RWR}}$	71	G14	TO	AL	RAM write
$\overline{\text{STDINTL}}$	82	C13	TTO	ZL	Standard interrupt level
$\overline{\text{STDPINTP}}$	83	B14	TO	AL	Standard interrupt pulse
$\overline{\text{HPINT}}$	84	B13	TO	ZL	High-priority interrupt
$\overline{\text{TIMRONA}}$	85	B12	TO	AL	Timer on - channel A
$\overline{\text{TIMRONB}}$	86	C11	TO	AL	Timer on - channel B
ACTIVE	81	D13	TO	AH	Active on 1553 bus
$\overline{\text{COMSTR}}$	90	C10	TO	AL	(RT) command strobe
SSYSF	128	G1	TI	AH	Subsystem fail
BCRTF	129	H2	TO	AH	BCRT fail
CHA/$\overline{\text{B}}$	89	A12	TO		Channel A/$\overline{\text{B}}$
$\overline{\text{MEMWIN}}$	59	J14	TO	AL	Memory (access) window
RAO	50	P14	TI		Receive (channel) A O
RAZ	51	N14	TI		Receive (channel) A Z
RBO	54	N15	TI		Receive (channel) B O
RBZ	55	L14	TI		Receive (channel) B Z
TAO	52	M14	TO		Transmit (channel) A O
TAZ	53	L13	TO		Transmit (channel) A Z
TBO	56	M15	TO		Transmit (channel) B O
TBZ	57	K13	TO		Transmit (channel) B Z

6.4 Symbols and definitions - Continued.

Name	Pin number Cases Y	Pin number Cases X	1/ Type	1/ Active	Description
$\overline{\text{DMAR}}$	72	F14	TTO	ZL	DMA request
$\overline{\text{DMAG}}$	73	F13	TI	AL	DMA grant
$\overline{\text{DMAGO}}$	78	E13	TO	AL	DMA grant out
$\overline{\text{DMACK}}$	75	D15	TTO	ZL	DMA acknowledge
BURST	77	D14	TO	AH	Burst (DMA cycle)
$\overline{\text{TSCTL}}$	76	C15	TO	AL	Three-state control
MD7	23	R4	TUI		Mode 7
MD6	22	P5	TUI		Mode 6
MD5	21	R3	TUI		Mode 5
MD4	20	N5	TUI		Mode 4
MD3	19	P4	TUI		Mode 3
MD2	18	P3	TUI		Mode 2
MD1	17	P2	TUI		Mode 1
MD0	16	N3	TUI		Mode 0
MDO6	14	P1	TTO		Mode 6 out
MDO5	13	N2	TTO		Mode 5 out
MDO4	12	L3	TTO		Mode 4 out
MDO3	11	M2	TTO		Mode 3 out
MDO2	10	N1	TTO		Mode 2 out
MDO1	9	M1	TTO		Mode 1 out
MDO0	8	L1	TTO		Mode 0 out

* U. S. GOVERNMENT PRINTING OFFICE: 1988—550-547

6.4 Symbols and definitions - Continued.

Name	Pin number Cases Y	Pin number Cases X	1/ Type	1/ Active	Description
$\overline{\text{FBUSY}}$	79	C14	TUI	AL	Force/busy
$\overline{\text{BUSYACK}}$	80	B15	TO	AL	Busy acknowledge
$\overline{\text{WRAPEN}}$	6	K2	TUI	AL	Wrap around enable
WRAPF	5	J2	TO	AH	Wrap fail
$\overline{\text{ALTWRAP}}$	4	K1	TUI	AL	Alternate wrap around
LGL10	121	E2	TTO		Legalization bus bit 10
LGL9	120	C1	TTO		Legalization bus bit 9
LGL8	119	E3	TTO		Legalization bus bit 8
LGL7	118	D2	TTO		Legalization bus bit 7
LGL6	117	C2	TTO		Legalization bus bit 6
LGL5	116	B2	TTO		Legalization bus bit 5
LGL4	115	C3	TTO		Legalization bus bit 4
LGL3	114	C4	TTO		Legalization bus bit 3
LGL2	113	A2	TTO		Legalization bus bit 2
LGL1	112	B3	TTO		Legalization bus bit 1
LGL0	111	C5	TTO		Legalization bus bit 0

6.4 Symbols and definitions - Continued.

Name	Pin number Cases Y	Pin number Cases X	1/ Type	1/ Active	Description
BRDCAST	122	D1	TTO	AH	Broadcast
MC	123	F3	TTO	AH	Mode code
$\overline{\text{LGLEN}}$	127	F1	TTO	AL	Legalization bus enable
LGLCMD	124	F2	TUI	AH	Legal command
$\overline{\text{ERR}}$	125	G2	TO	AL	Error
DOMC	126	G3	TUI	AH	Do mode code
CLK	3	J1	TI		12 MHz ±.01% with 40-60 duty cycle
MCLK	58	K14	TI		Memory clock
MCLKD2	74	E15	TO		Memory clock divided by two.
VDD	132	H3	PWR		+5 V
VDD	34	N9	PWR		+5 V
VDD	67	G13	PWR		+5 V
VDD	100	C7	PWR		+5 V
VSS	1	J3	GND		Ground
VSS	33	N8	GND		Ground
VSS	66	H13	GND		Ground
VSS	99	C8	GND		Ground

1/ Abbreviations:

TUI = TTL input (pull up) AL = Active low AH = Active high
TI = TTL input TO = TTL output TTB = Bidirectional
TTO = Three state output ZL = Active low, inactive state is high impedance

6.5 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.6 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.7 Approved sources of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreeded to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of the document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8950101XX	65342	UT1553 BCRTMP G
5962-8950101YX	65342	UT1553 BCRTMP A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	United Technologies Microelectronics Center 1575 Garden of the Gods Colorado Springs, CO 80907