VITELIC

# V61C32 FAMILY
# HIGH PERFORMANCE LOW POWER
# 2K x 8 BIT
# CMOS DUAL PORT MEMORY

## Features

- 2K x 8 bit CMOS static RAM with 3-state outputs
- Dual-port with on-chip arbitration logic
- High speed
  - Maximum access time of 55/70/90/120 ns
- Battery backup 2 volt data retention
- Low power operation
  - operating 325 mW (typ)
  - standby 15 $\mu$W (typ)
- VICMOS process virtually eliminates alpha particle induced soft errors
- Full CMOS memory cell
- Both ports fully asynchronous
- Single 5 volt power supply
- TTL compatible

## Description

The Vitelic V61C32 is a CMOS 2K x 8 high-speed dual port static RAM with advanced arbitration logic to provide 55 ns access to both ports simultaneously. Fabrication with VICMOS technology provides a high-performance, low-power alternative to NMOS memory.

The Vitelic V61C32 provides two parallel 8-bit ports with separate controls, addresses, and I/O permitting read or write access to any memory location. Automatic power-down circuitry permits a port to be placed in the standby mode when $\overline{CE}$ is high.

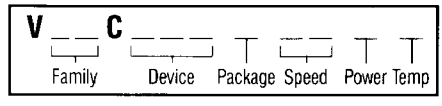
The $\overline{BUSY}$ signal is used to indicate an attempt by both ports to access simultaneously to the same address location. The signal may be ignored or acted upon as required by system design. If both ports are attempting to read or write the same address location simultaneously, data can be compromised and $\overline{BUSY}$ will be asserted on the port denied access.

The Vitelic V61C32 offers a battery backup data retention mode where the device typically consumes only 2.5 $\mu$W from a 2 volt source.

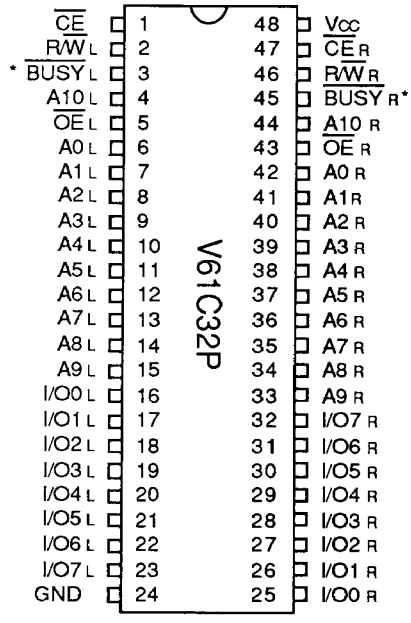
## Device Usage Chart

| Operating Temperature Range | Package Outline | | | | Access Time (ns) | | | | Power | | Temperature Mark |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | P | J | AJ | | 55 | 70 | 90 | 120 | Low | Std. | |
| 0°C to 70°C | • | • | • | | • | • | • | | • | • | Blank |
| −40°C to +85°C | • | • | • | | | • | • | • | • | • | I |

| Package | Std. | Pin Count |
|---|---|---|
| Plastic DIP | P | 48 |
| PLCC (J Lead) | J | 52 |
| PLCC (J Lead) | AJ | 52 |

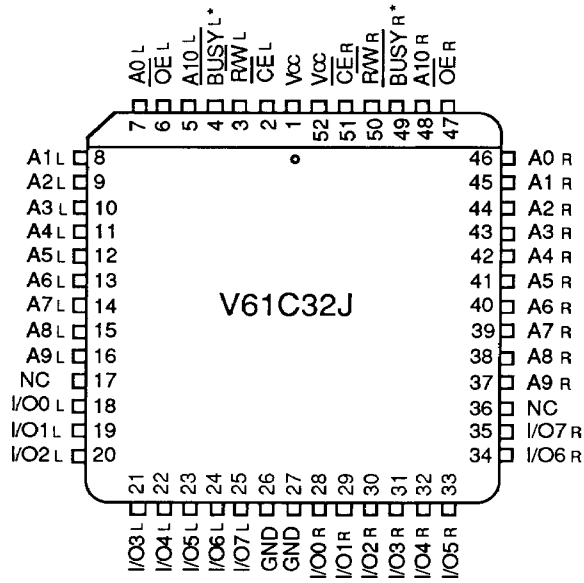


## DIP PIN CONFIGURATION
*Top View*

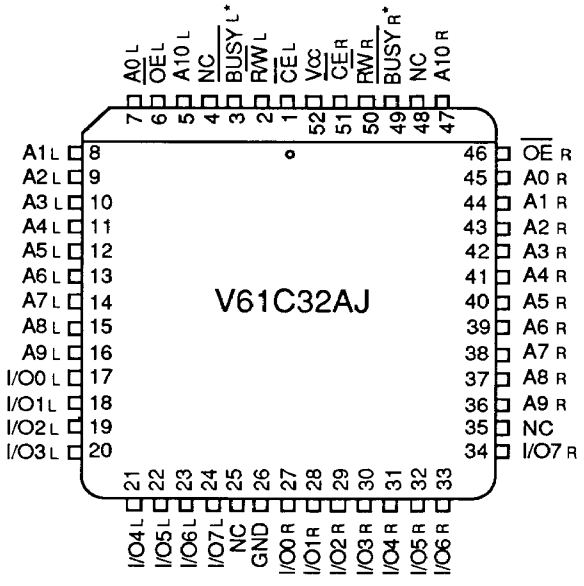



*NOTE: THE BUSY SIGNAL IS AN OPEN DRAIN OUTPUT, AND THUS REQUIRES A PULL-UP RESISTOR

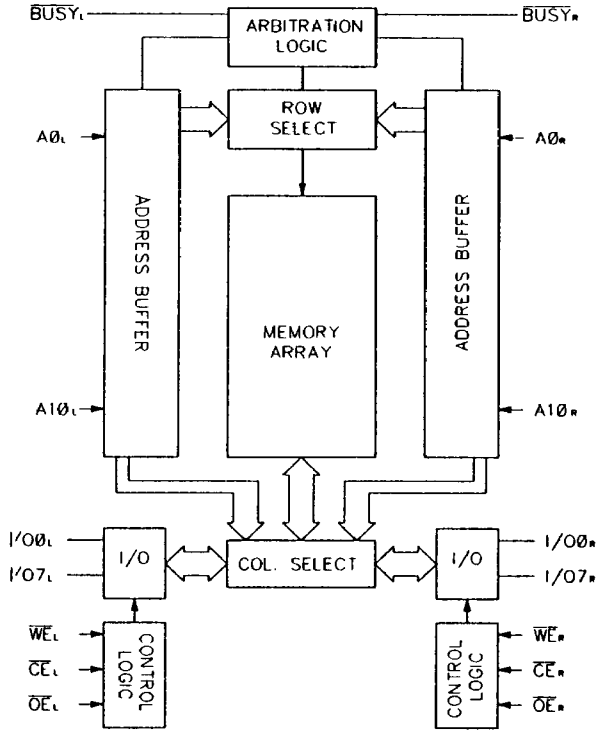
## PLCC PIN CONFIGURATION
*Top View*




## PLCC PIN CONFIGURATION
*Top View*



## BLOCK DIAGRAM




## Absolute Maximum Ratings (1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{TERM}$ | Voltage on any Pin with Respect to $V_{SS}$ | −0.5* to +7.0 | V |
| $T_A$ | Operating Temperature Under Bias | Same as Recommended Operating Conditons | °C |
| $T_{STG}$ | Storage Temperature | −65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

*−3.5V for 20 ns pulse.

**NOTE:**
1. Operation at or near absolute maximum ratings can affect device reliability.

## Recommended Operating Conditions

$T_A$ = Operating Temperature Range

| Range | Temperature |
|---|---|
| Commercial | 0°C to 70°C |
| Industrial | −40°C to +95°C |
| Extended | −55°C to +125°C |

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{SS}$ | Supply Voltage | 0.0 | 0.0 | 0.0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | 3.5 | $V_{DD}$ | V |
| $V_{IL}$ | Input Low Voltage | −0.5* | — | +0.8 | V |

*−3.5V for 20 ns pulse.

## Capacitance

$T_A$ = 25°C, f = 1.0 MHz

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{IN}$ | Input Capacitance | $V_{OUT}$ = 0V | 5 | pF |

## Non-Contention Read-Write Control

| Left Port Inputs | | | Right Port Inputs | | | Flags | | Function |
|---|---|---|---|---|---|---|---|---|
| $R/\overline{W}_L$ | $\overline{CE}_L$ | $\overline{OE}_L$ | $R/\overline{W}_R$ | $\overline{CE}_R$ | $\overline{OE}_R$ | $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | |
| X | H | X | X | X | X | H | H | Left Port in Power Down Mode |
| X | X | X | X | H | X | H | H | Right Port in Power Down |
| L | L | X | X | X | X | H | H | Data on Left Port Written Into Memory |
| H | L | L | X | X | X | H | H | Data in Memory Output on Left Port |
| X | X | X | L | L | X | H | H | Data on Right Port Written Into Memory |
| X | X | X | H | L | L | H | H | Data in Memory Output on Right Port |

H = High, L = Low, X = Don't Care

## $\overline{CE}$ Arbitration with Address Match Before $\overline{CE}$

| Left Port | | | | Right Port | | | | Flags | | Function |
|---|---|---|---|---|---|---|---|---|---|---|
| $R/\overline{W}_L$ | $\overline{CE}_L$ | $\overline{OE}_L$ | $A_{0L}$-$A_{10L}$ | $R/\overline{W}_R$ | $\overline{CE}_R$ | $\overline{OE}_R$ | $A_{0R}$-$A_{10R}$ | $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | |
| X | LBR | X | Match | X | L | X | Match | H | L | Left Operation Permitted<br>Right Operation Not Permitted |
| X | L | X | Match | X | LBL | X | Match | L | H | Left Operation Not Permitted<br>Right Operation Permitted |
| X | LST | X | Match | X | LST | X | Match | H | L | Left Operation Permitted<br>Right Operation Not Permitted |

**NOTE:**
X = Don't Care, L = Low, H = High, LST = Low Same Time, LBR = Low Before Right, LBL = Low Before Left

## Address Arbitration with $\overline{CE}$ Low Before Address Match

| Left Port | | | | Right Port | | | | Flags | | Function |
|---|---|---|---|---|---|---|---|---|---|---|
| $R/\overline{W}_L$ | $\overline{CE}_L$ | $\overline{OE}_L$ | $A_{0L}$-$A_{10L}$ | $R/\overline{W}_R$ | $\overline{CE}_R$ | $\overline{OE}_R$ | $A_{0R}$-$A_{10R}$ | $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | |
| X | L | X | VBR | X | L | X | Valid | H | L | Left Operation Permitted<br>Right Operation Not Permitted |
| X | L | X | Valid | X | L | X | VBL | L | H | Left Operation Not Permitted<br>Right Operation Permitted |
| X | L | X | VST | X | L | X | VST | H | L | Left Operation Permitted<br>Right Operation Not Permitted |

**NOTE:**
X = Don't Care, L = Low, H = High, VST = Valid Same Time, VBR = Valid Before Right, VBL = Valid Before Left

## DC Characteristics

For operating conditions, refer to Temperature Range Marking

| Symbol | Parameter | Test Conditions | Range | V61C32 | | | V61C32L | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. (1) | Max. | Min. | Typ. (1) | Max. | |
| $I_{LI}$ | Input Leakage Current | $V_{DD}$ = 5.5V, $V_{IN}$ = 0.0V to $V_{DD}$ | * — | — | — | 10 | — | — | 5 | µA |
| | | | ** I | — | — | 10 | — | — | 5 | |
| | | | *** X | — | — | 20 | — | — | 10 | |
| $I_{LO}$ | Output Leakage Current | $\overline{CE} \geq V_{IL}$, $V_{OUT}$ = 0.0V to $V_{DD}$ | — | — | — | 10 | — | — | 5 | µA |
| | | | I | — | — | 10 | — | — | 5 | |
| | | | X | — | — | 20 | — | — | 10 | |
| $V_{IH}$ | Input High Voltage | | | 2.2 | — | 6.0 | 2.2 | — | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.5 (2) | — | +0.8 | -0.5 (2) | — | +0.8 | V |
| $I_{DD}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R \leq V_{IH}$, Outputs Open | — | — | 65 | 120 | — | 65 | 100 | mA |
| | | | I | — | 65 | 175 | — | 65 | 135 | |
| | | | X | — | 65 | 180 | — | 65 | 150 | |
| $I_{SB1}$ | Standby Current (Both Ports Standby) | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ | — | — | 15 | 25 | — | 15 | 20 | mA |
| | | | I | — | 15 | 50 | — | 15 | 30 | |
| | | | X | — | 15 | 50 | — | 15 | 30 | |
| $I_{SB2}$ | Standby Current (One Port Standby) | $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$, other $\overline{CE} \leq V_{IL}$ Active Port Data Pins Open | — | — | 40 | 100 | — | 40 | 60 | mA |
| | | | I | — | 40 | 110 | — | 40 | 75 | |
| | | | X | — | 40 | 110 | — | 40 | 75 | |
| $I_{SB3}$ | CMOS Standby Current (Both Ports Standby) | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD}$ -0.2V $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V | — | — | 5 | 10000 | — | 3 | 100 | µA |
| | | | I | — | 5 | 15000 | — | 3 | 250 | |
| | | | X | — | 5 | 15000 | — | 3 | 4000 | |
| $I_{SB4}$ | CMOS Standby Current (One Port Standby) | $\overline{CE}_L$ or $\overline{CE}_R \geq V_{DD}$-0.2V, Other $\overline{CE} \leq V_{IL}$, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, Active Data Pins Open | — | — | 40 | 90 | — | 35 | 55 | mA |
| | | | I | — | 40 | 90 | — | 35 | 65 | |
| | | | X | — | 40 | 90 | — | 35 | 65 | |
| $V_{OL}$ | Output Low Voltage ($I/O_0$-$I/O_7$) | $I_{OL}$ = 3.5 mA | | — | — | 0.4 | — | — | 0.4 | V |
| | | $I_{OL}$ = 8.0 mA | | — | — | 0.5 | — | — | 0.5 | |
| $V_{OL}$ | Open Drain Output Low Voltage ($\overline{BUSY}$) | $I_{OL}$ = 8.0 mA | | — | — | 0.5 | — | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4.0 mA | | 2.4 | — | — | 2.4 | — | — | V |

**NOTES:**

1. $V_{DD}$ = 5.0V, $T_A$ = +25°C.
2. $V_{IL}$ (min) = -3.5 for pulse width less than 20 ns.

* (—) $T_A$ = 0°C to 70°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

** (I) $T_A$ = -40°C to +85°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

*** (X) $T_A$ = -55°C to +125°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V unless otherwise noted

For availabillity in a particular temperature range, refer to Device Usage Chart, Page 1.

## AC Characteristics

For operating conditions, refer to Temperature Range Marking

### Read Cycle

| Symbol | Parameter | Range | 55 | | 70 | | 90 | | 120 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | | 55 | — | 70 | — | 90 | — | 120 | — | ns |
| $t_{AA}$ | Address Access Time | | — | 55 | — | 70 | — | 90 | — | 120 | ns |
| $t_{ACE}$ | Chip Enable Access Time | | — | 55 | — | 70 | — | 90 | — | 120 | ns |
| $t_{AOE}$ | Output Enable Access Time | *— | — | 20 | — | 35 | — | 40 | N/A | N/A | ns |
| | | **I | N/A | N/A | — | 35 | — | 40 | — | 40 | |
| | | ***X | N/A | N/A | — | 35 | — | 40 | — | 40 | |
| $t_{OH}$ | Output Hold From Address Change | — | 10 | — | 10 | — | 10 | — | N/A | N/A | ns |
| | | I | N/A | N/A | 10 | — | 10 | — | 20 | — | |
| | | X | N/A | N/A | 10 | — | 15 | — | 20 | — | |
| $t_{LZ}$ | Output Low-Z Time (1) | — | 5 | — | 5 | — | 5 | — | N/A | N/A | ns |
| | | I | N/A | N/A | 5 | — | 5 | — | 10 | — | |
| | | X | N/A | N/A | 5 | — | 5 | — | 10 | — | |
| $t_{HZ}$ | Output High-Z Time (1) | | — | 20 | — | 35 | — | 40 | — | 40 | ns |
| $t_{PU}$ | $\overline{CE}$ to Power Up Time | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$ | Chip Disable to Power Down Time | | — | 35 | — | 40 | — | 50 | — | 50 | ns |

### Write Cycle

| Symbol | Parameter | Range | 55 | | 70 | | 90 | | 120 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{WC}$ | Write Cycle Time | | 55 | — | 70 | — | 90 | — | 120 | — | ns |
| $t_{EW}$ | Chip Enable to End of Write | | 50 | — | 65 | — | 85 | — | 110 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | | 50 | — | 65 | — | 85 | — | 110 | — | ns |
| $t_{AS}$ | Address Setup Time | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | — | 30 | — | 40 | — | 50 | — | N/A | N/A | ns |
| | | I | N/A | N/A | 40 | — | 50 | — | 60 | — | |
| | | X | N/A | N/A | 40 | — | 50 | — | 60 | — | |
| $t_{WR}$ | Write Recovery Time | | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{DW}$ | Data Valid to End of Write | — | 20 | — | 25 | — | 30 | — | N/A | N/A | ns |
| | | I | N/A | N/A | 25 | — | 30 | — | 35 | — | |
| | | X | N/A | N/A | 25 | — | 30 | — | 35 | — | |
| $t_{DH}$ | Data Hold Time | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZ}$ | Output High-Z Time (1) | | — | 20 | — | 35 | — | 40 | — | 50 | ns |
| $t_{WZ}$ | $\overline{WE}$ to Output High-Z (1) | | 0 | 25 | 0 | 35 | 0 | 40 | 0 | 50 | ns |
| $t_{OW}$ | Output Active From End of Write (1) | | 0 | — | 0 | — | 0 | — | 0 | — | ns |

**NOTE:**

1. Transition is measured ± 500 mV from low or high voltage with load (Figure 2). This parameter is sampled and not 100% tested.

* (—) $T_A$ = 0°C to 70°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

** (I) $T_A$ = −40°C to +85°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

*** (X) $T_A$ = −55°C to +125°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V unless otherwise noted

For part availabillity in a particular temperature range, refer to Device Usage Chart, Page 1.

## AC Characteristics

### $\overline{BUSY}$ Timing (1)

| Symbol | Parameter | 55 | | 70 | | 90 | | 120 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 55 | — | 70 | — | 90 | — | 120 | — | ns |
| $t_{WC}$ | Write Cycle Time | 55 | — | 70 | — | 90 | — | 120 | — | ns |
| $t_{BAA}$ | $\overline{BUSY}$ Access Time to Address | — | 40 | — | 45 | — | 45 | — | 60 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable Time to Address | — | 45 | — | 45 | — | 45 | — | 60 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access Time to $\overline{CE}$ | — | 40 | — | 45 | — | 45 | — | 60 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable Time to $\overline{CE}$ | — | 45 | — | 45 | — | 45 | — | 60 | ns |
| $t_{APS}$ | Arbitration Priority Setup Time | 10 | — | 10 | — | 10 | — | 10 | — | ns |

**NOTE:**

1. Commercial Temperature Range—$T_A$ = 0°C to 70°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V
   Industrial Temperature Range—$T_A$ = 40°C to +85°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V
   Extended Temperature Range—$T_A$ = −55°C to +125°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V unless otherwise noted.
   For availability in a particular temperature range, refer to Device Usage Chart, Page 1.

## AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | $V_{SS}$ to 3.0V |
| Input Rise and Fall Times | 5 ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1, 2 and 3 |

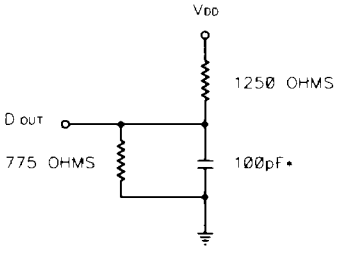



Figure 1.
*Including scope and jig.

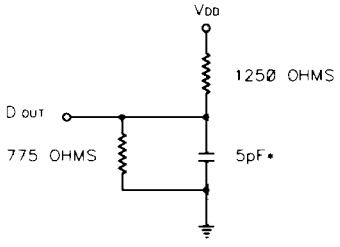



Figure 2.
(for $t_{HZ}$, $t_{LZ}$, $t_{WZ}$, and $t_{OW}$)

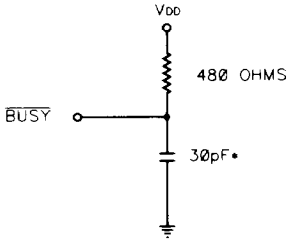
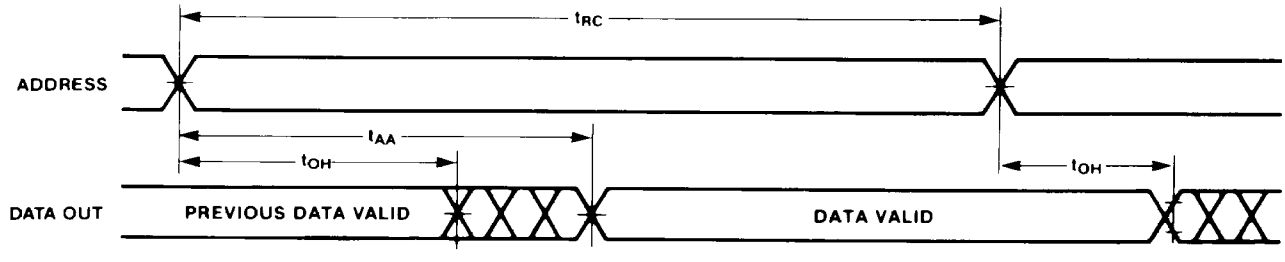
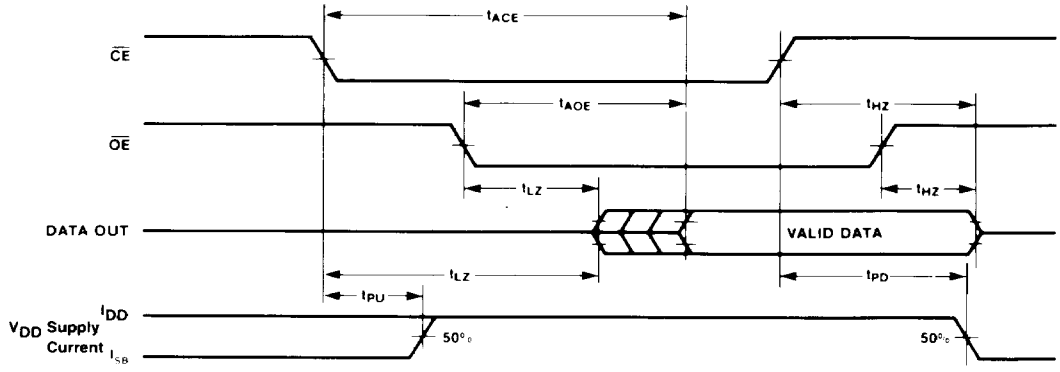



Figure 3.

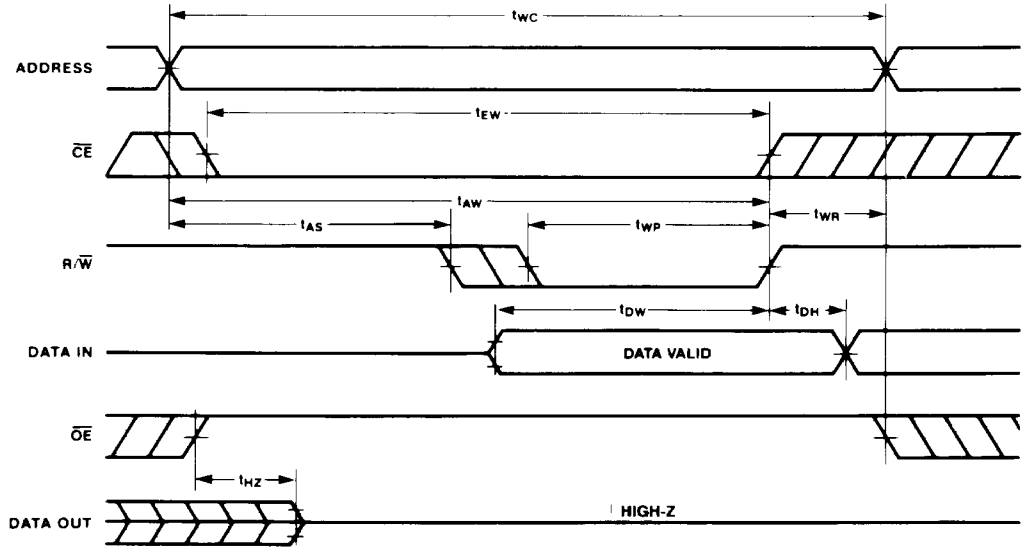
### Timing Waveform of Read Cycle No. 1 Either Side (1, 2, 6)



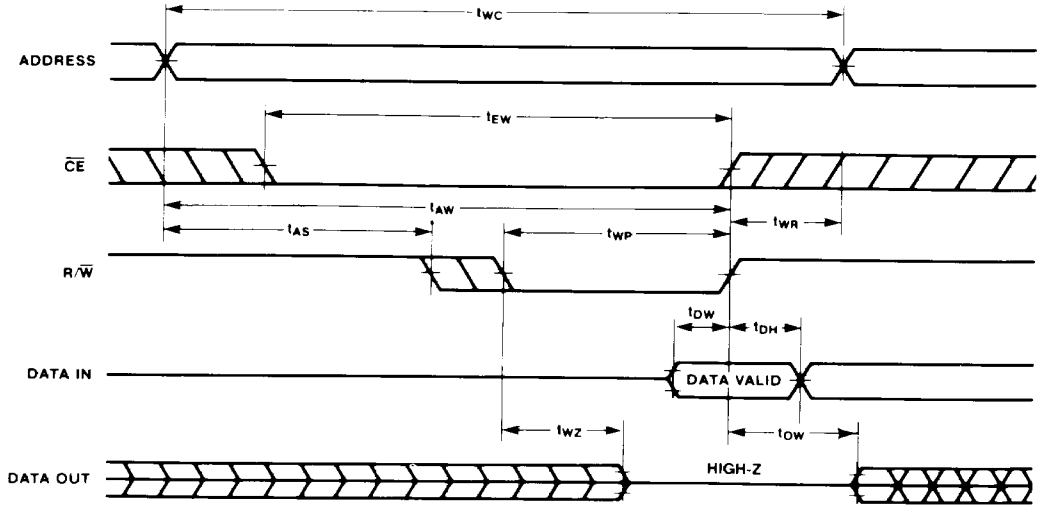
### *Timing Waveform of Read Cycle No. 2 Either Side (1, 3)*




### *Timing Waveform of Write Cycle No. 2 Either Side (4, 7)*

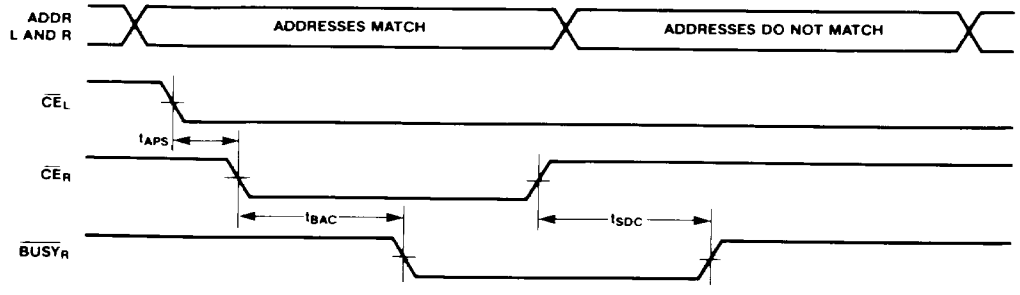


### Timing Waveform of Write Cycle No. 1 Either Side (4, 7)

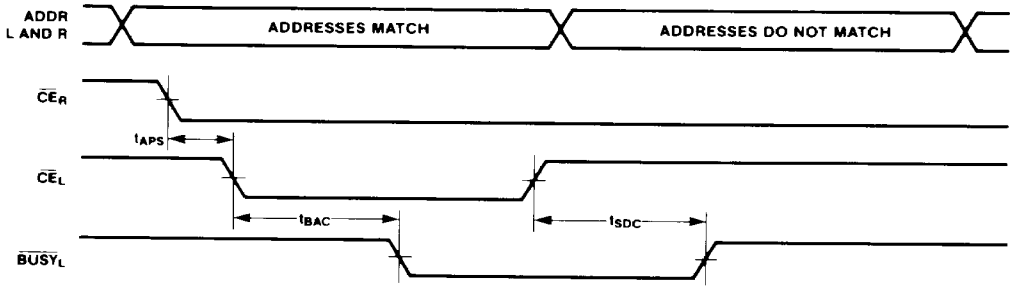



### Timing Waveform of Contention Cycle No. 1 $\overline{CE}$ Arbitration

**$\overline{CE}_L$ VALID FIRST:**

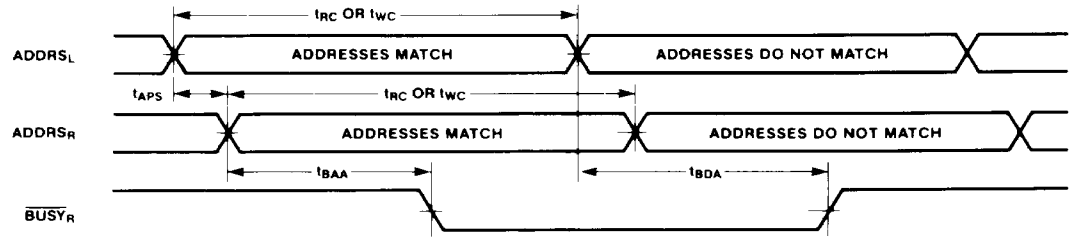



**$\overline{CE}_R$ VALID FIRST:**

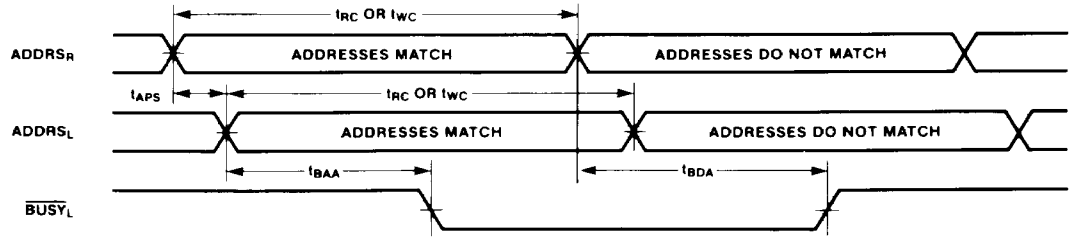


### *Timing Waveform of Contention Cycle No. 2 Address Valid Arbitration (5)*

**LEFT ADDRESS VALID FIRST**




**RIGHT ADDRESS VALID FIRST**




**NOTES:**

1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled. $\overline{CE}$ = $V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = $V_{IL}$.
6. $\overline{OE}$ = $V_{IL}$.
7. R/$\overline{W}$ = $V_{IH}$ during address transition.

## *Data Retention Characteristics*

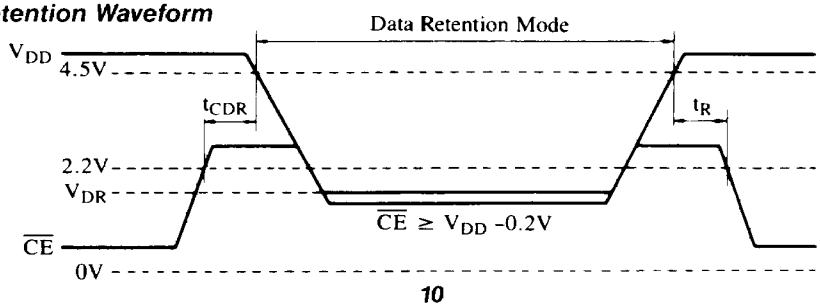
V61C32L

| Symbol | Parameter | Test Conditions | Min. | Typ. (1) | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Retention Data | | 2.0 | — | — | V |
| $I_{DDDR}$ | Data Retention Current | $V_{DD}$ = 3.0V, $\overline{CE}$ ≥ $V_{DD}$ − 0.2V<br>$V_{IN}$ ≥ $V_{DD}$ −0.2V or $V_{IN}$ ≤ +0.2V | — | 3 | 100 (3) | μA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | — | — | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$ (2) | — | — | ns |

**NOTES:**

1. $V_{DD}$ = 2V, $T_A$ = +25°C.
2. $t_{RC}$ = Read Cycle Time.
3. 100 μA max. for 0°C to 70°C, 250 μA max. for −40°C to +85°C, 4000 μA max. for −55°C to +125°C.

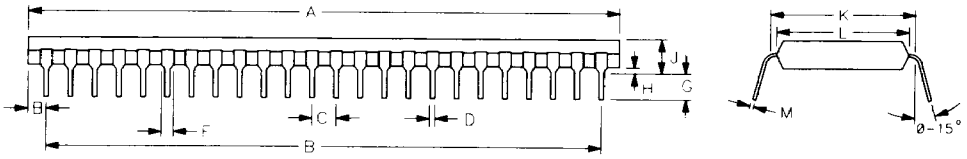
### *Low $V_{DD}$ Data Retention Waveform*



## Package Outline

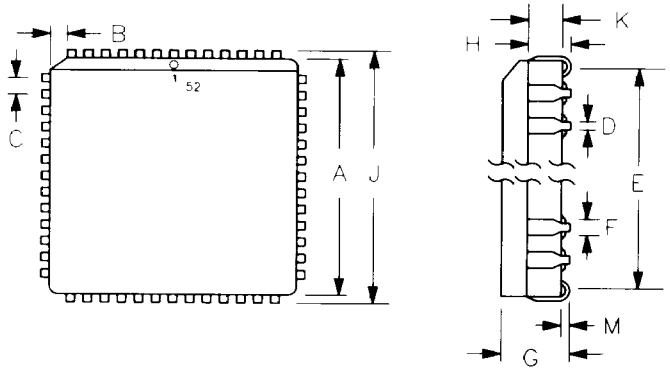
### 48 Pin Plastic

| Dimension | Inches | Millimeters |
|---|---|---|
| A | 2 460 max | 62 484 max |
| B | 080 | 2 032 |
| C | 1 | 2 54 |
| D | 015/ 020 | 381/ 508 |
| F | 2 3 | 58 42 |
| F | 040/ 065 | 1.016/1 651 |
| G | 125/ 160 | 3 175/4 064 |
| H | 015/.065 | 381/1 651 |
| J | 160/ 225 | 4 064/5 715 |
| K | 540/ 610 | 14 986/15 494 |
| L | 530/ 550 | 13 462/13 970 |
| M | 009/ 012 | 229/ 305 |




### 52 Pin PLCC-J

| Dimension | Inches | Millimeters |
|---|---|---|
| A | 760 max | 19.30 max |
| B | 045 | 1 14 |
| C | 050 typ | 1 27 typ |
| D | 017 typ | 43 typ |
| E | 730 max | 18 54 max |
| F | 026/ 032 | 66/ 81 |
| G | 180 max | 4 57 |
| H | 098 nom | 2 49 |
| J | 795 | 20 19 |
| K | 055 nom | 1 40 |
| M | 030/0 45 | 76/1 14 |



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