FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12514-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89670/A Series

MB89673/677A/P677A/PV670A

■ DESCRIPTION

The MB89670/A series has been developed as a line of proprietary 8-bit, single-chip microcontrollers.

In addition to the F²MC*-8L CPU core which can operate at low voltage but at high speed, the microcontrollers contain pheripheral functions such as timers, a serial interface, an A/D converter, a UART, an up/down counter, and an external interrupt.

The MB89670/A series is applicable to a wide range of applications from welfare products to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

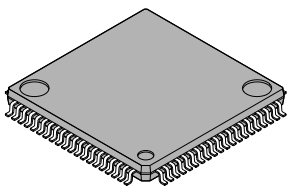
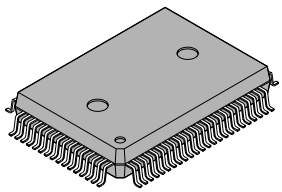
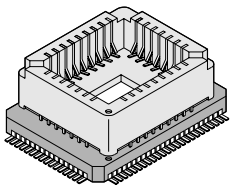
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- High-speed processing at low voltage
- Minimum execution time: 0.4 µs/3.5 V, 0.8 µs/2.7 V, 2.0 µs/2.2 V
- I/O ports: max. 69 channels

(Continued)

■ PACKAGE

80-pin Plastic QFP	80-pin Plastic QFP	80-pin Ceramic MQFP
		
(FPT-80P-M11)	(FPT-80P-M06)	(MQP-80C-P01)

(Continued)

- Timers: 9 channels (MB89670A: 12 channels)
  8-bit PWM timer: 3 channels (MB89670A: 6 channels) (also usable as a reload timer)
  16-bit timer/counter
  21-bit time-base timer
  8/16-bit timer (8 bits × 2 channels or 16 bits)
  8/16-bit up/down counter timer (8 bits × 2 channels or 16 bits)
- Two serial interfaces
  8-bit synchronized serial: 1 channel (Switchable transfer direction allows communication with various equipment.)
  UART: 1 channel (with full-duplex double buffer)
- External interrupts: 8 channels
  Eight channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Buzzer output
- 10-bit A/D converter
  8-channel input
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
- Bus interface function
  Including hold and ready functions

■ PRODUCT LINEUP

Part number / Parameter	MB89673*1	MB89677A	MB89P677A	MB89PV670A
Classification	Mass production products (mask ROM products)		One-time PROM product (for development)	Piggyback/ evaluation product (for development)
ROM size	8 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM)	48 K × 8 bits (external ROM)
RAM size	384 × 8 bits	1 K × 8 bits		
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs/10 MHz to 6.4 µs/10 MHz Interrupt processing time: 3.6 µs/10 MHz to 57.6 µs/10 MHz			
Ports	Output ports (N-channel open-drain): 14 (12 also serve as peripherals.) Output ports (CMOS): 8 (All also serve as peripherals.) I/O ports (N-channels open-drain): 7 (All also serve as peripherals.) I/O ports (CMOS): 32 (All also serve as peripherals.) Input ports: 8 (All also serve as peripherals.) Total: 69			
Option	Specify when ordering masking		Set with EPROM programmer	Setting not possible
21-bit time-base timer	21 bits (0.81 ms, 3.27 ms, 26.21 ms, 419 ms/10 MHz)			
8/16-bit up/ down counter	8 bits × 2 channels or 16 bits × 1 channel Timer operation Up/down counter operation Phase difference counting (successive double mode, quadruple mode)			
16-bit timer/ counter	16-bit timer operation 16-bit event counter operation (edge selectability)			
8/16-bit timer counter	8 bits × 2 channels or 16 bits × 1 channel Reload timer operation (toggled output capable) Event counter operation			
8-bit PWM timer 1, 8-bit PWM timer 2	8 bits × 2 channels reload timer operation (toggled output capable) 8 bits × 2 channels PWM operation (four fixed frequency) 8 bits × 1 channel PPG operation (variable frequency) Capable of output switching between 2 channels			
8-bit PWM timer 3, 8-bit PWM timer 4, 5, 6	8-bit reload timer operation (toggled output capable) 8-bit PWM operation (four fixed frequency) Capable of output switching between 2 channels			
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks)			

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Part number / Parameter	MB89673*1	MB89677A	MB89P677A	MB89PV670A
UART	Variable data length (7 or 8 bits) Internal baud rate generator Error detection function Intenal full-duplex double buffer NRZ transfer format CLK synchrnous/asynchronous data transfer capable			
10-bit A/D converter	10 bit × 8 channels			
External interrupt	8 channels (Rising edge/falling edge)			
Operating voltage*2	2.2 V to 6.0 V		2.7 V to 6.0 V	
EPROM for use				MBM27C512-20TV (LCC package)

*1: 8-bit PWM timer 4, 5, and 6 is not provided for the MB89673.
*2: The minimum operating voltage varies with the operating frequency, the function, and the connected ICE.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89673 MB89677A MB89P677A	MB89PV670A
FPT-80P-M06	○	×
FPT-80P-M11	○	×*
MQP-80C-P01	×	○

○ : Available × : Not available

* : Lead pitch converter sockets (manufacturer: Sun Hayato Co., Ltd.) are available
80QF-80QF2-8L-UP
+ (MQP-80C-P01 or FPT-80P-M06) → for conversion to FPT-80P-M11
80QF-80QF2-8L-DWN

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P677A, the program area starts from address 8007_H but on the MB89677A and MB89PV670A starts from 8000_H.

  (On the MB89P677A, addresses 8000_H to 8006_H comprise the option setting area, option settings can be read by reading these addresses. On the MB89677A and MB89PV670A, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P677A.)
- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV670A, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following point:

- Options are fixed on the MB89PV670A.

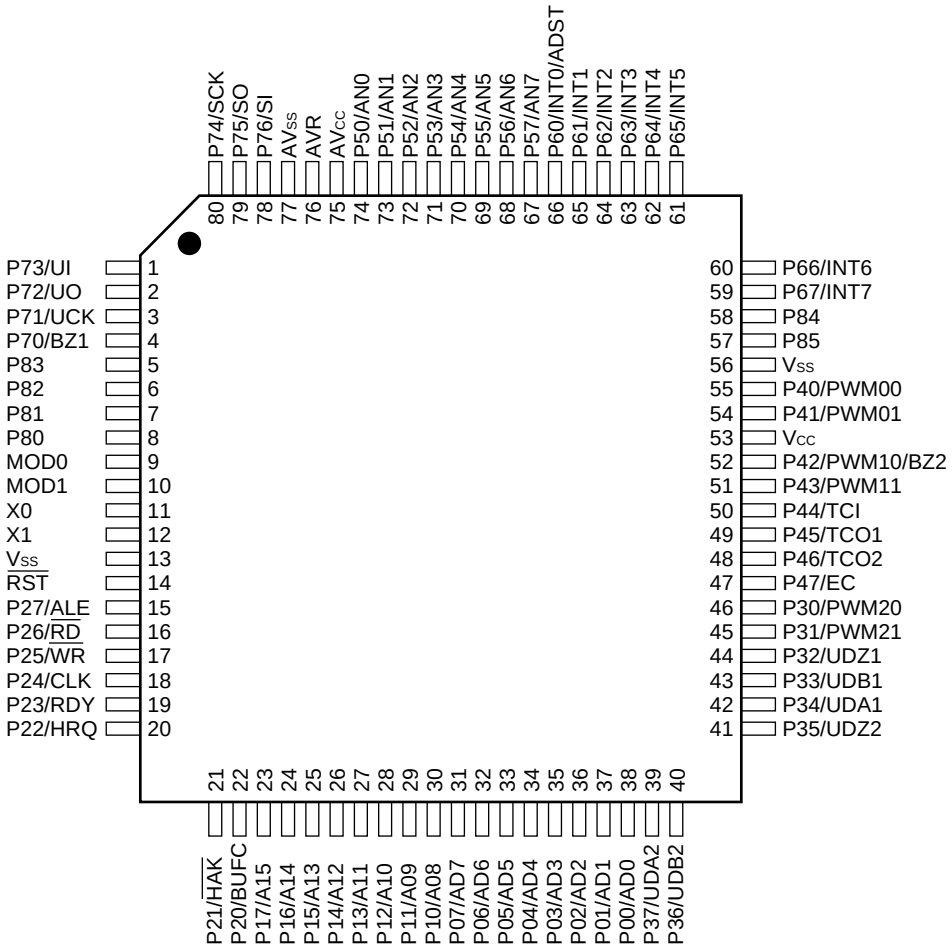
■ CORRESPONDENCE BETWEEN THE MB89670/A AND MB89670R/AR SERIES

- The MB89670R/AR series is the reduction version of the MB89670/A series.
  For their differences, refer to the MB89670R/AR series data sheet.

MB89670/A series	MB89673	—	MB89677A	MB89P677A	MB89PV670A
MB89670R/AR series	MB89673R	MB89675R	MB89677AR		

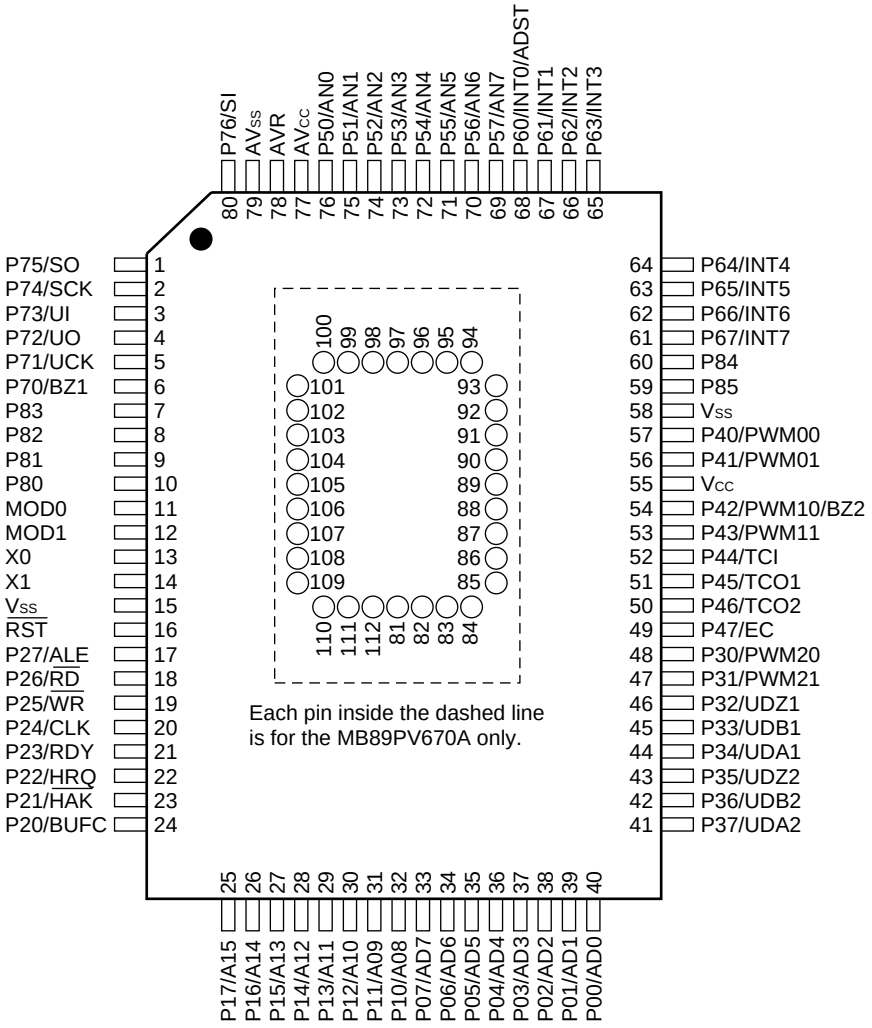
■ PIN ASSIGNMENT

(Top view)



(FPT-80P-M11)

(Top view)



(FPT-80P-M06)

(MQP-80C-P01)

- **Pin assignment on package top (MB89PV670A only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{OE}/V_{PP}$
82	A15	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	$\overline{O6}$	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	CE	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	QFP*2 MQFP*3			
11	13	X0	A	Clock oscillator pins
12	14	X1		
9	11	MOD0	B	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
10	12	MOD1		
14	16	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with pull-up resistor and a hysteresis input. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
38 to 31	40 to 33	P00/AD0 to P07/AD7	D	General-purpose I/O ports When an external bus is used, these ports function as multiplex pins of lower address output and data I/O.
30 to 23	32 to 25	P10/A08 to P17/A15		General-purpose I/O ports When an external bus is used, these ports function as upper address output pins.
22	24	P20/BUFC	F	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
21	23	P21/$\overline{HAK}$	F	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge output by setting the BCTR.
20	22	P22/HRQ	D	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
19	21	P23/RDY	D	General-purpose output port When an external bus is used, this port functions as a ready input.
18	20	P24/CLK	F	General-purpose output port When an external bus is used, this port functions as a clock output.
17	19	P25/$\overline{WR}$	F	General-purpose output port When an external bus is used, this port functions as a write signal output.
16	18	P26/$\overline{RD}$	F	General-purpose output port When an external bus is used, this port functions as a read signal output.
15	17	P27/ALE	F	General-purpose output port When an external bus is used, this port functions as an address latch signal output.

(Continued)

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

Pin no.		Pin name	Circuit type	Function
QFP*1	QFP*2 MQFP*3			
46	48	P30/PWM20	D	General-purpose I/O port Also serves as the PWM20 output for the 8-bit PWM timer.
45	47	P31/PWM21	D	General-purpose I/O port Also serves as the PWM21 output for the 8-bit PWM timer.
44	46	P32/UDZ1	E	General-purpose I/O port Also serves as the Z-phase input for the 16-bit up/down counter/timer.
43	45	P33/UDB1	E	General-purpose I/O port Also serves as the B-phase input for the 16-bit timer/ counter.
42	44	P34/UDA1	E	General-purpose I/O ports Also serves as the A-phase input for the 16-bit up/down counter/timer.
41	43	P35/UDZ2	E	General-purpose I/O port Also serves as the Z-phase input for the 16-bit up/down counter/timer.
40	42	P36/UDB2	E	General-purpose I/O port Also serves as the B-phase input for the 16-bit up/down counter/timer.
39	41	P37/UDA2	E	General-purpose I/O port Also serves as the A-phase input for the 16-bit up/down counter/timer.
55	57	P40/PWM00	D	General-purpose I/O port Also serves as the PWM00 output for the 8-bit PWM timer.
54	56	P41/PWM01	D	General-purpose I/O port Also serves as the PWM01 output for the 8-bit PWM timer.
52	54	P42/PWM10/ BZ2	D	General-purpose I/O port Also serves as the PWM10 and the BZ2 output for the 8-bit PWM timer.
51	53	P43/PWM11	D	General-purpose I/O port Also serves as the PWM11 output for the 8-bit PWM timer.
50	52	P44/TCI	E	General-purpose I/O port Also serves as the TCI input for the 8/16-bit timer/ counter.
49	51	P45/TCO1	D	General-purpose I/O port Also serves as the TCO1 output for the 8/16-bit timer/ counter.

(Continued)

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

(Continued)

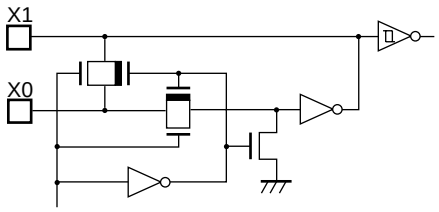
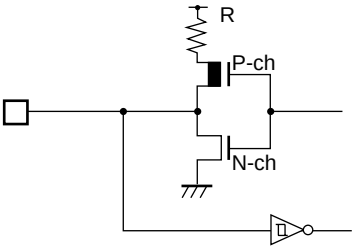
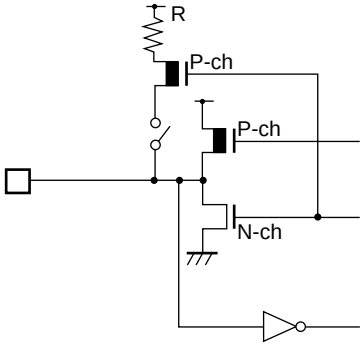
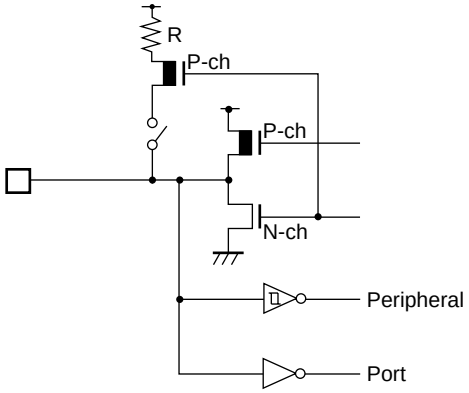
Pin no.		Pin name	Circuit type	Function
QFP*1	QFP*2 MQFP*3			
48	50	P46/TCO2	D	General-purpose I/O port Also serves as the TCO2 output for the 8/16-bit timer/counter.
47	49	P47/EC	E	General-purpose I/O port Also serves as input for the16-bit timer/counter. The EC input is a hysteresis input type.
74 to 67	76 to 69	P50/AN0 to P57/AN7	I	N-ch open-drain output ports Also serve as the analog input for the A/D converter.
66	68	P60/INT0/ ADST	J	General-purpose input port The software pull-up resistor is provided. Also serves as an external interrupt input (INT0) and an A/D converter external activation. This port is a hysteresis input type.
65 to 59	67 to 61	P61/INT1 to P67/INT7	J	General-purpose input ports A software pull-up resistor is provided. Also serve as an external interrupt input (INT1 to INT7). These ports are a hysteresis input type.
4	6	P70/BZ1	G	N-ch open-drain I/O port Also serves as a buzzer output.
3	5	P71/UCK	K	N-ch open-drain I/O port Also serves as a UART clock I/O (UCK) switchable to CMOS.
2	4	P72/UO	K	N-ch open-drain I/O port Also serves as a UART data output (UO) switchable to CMOS.
1	3	P73/UI	G	N-ch open-drain I/O port Also serves as a UART data input (UI).
80	2	P74/SCK	K	N-ch open-drain I/O port Also serves as the clock I/O for the serial I/O (SCK) switchable to CMOS.
79	1	P75/SO	K	N-ch open-drain I/O port Also serves as the data output (SO) for the serial I/O switchable to CMOS.
78	80	P76/SI	G	N-ch open-drain I/O port Also serves as the data input (SI) for the serial I/O.
8 to 5 57, 58	10 to 7 59, 60	P80 to P83 P85, P84	H	N-ch open-drain output ports
53	55	V_{CC}	—	Power supply pin
13, 56	15, 58	V_{SS}	—	Power supply (GND) pin
75	77	AV_{CC}	—	A/D converter power supply pin
76	78	AVR	—	A/D converter reference voltage input pin
77	79	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

- **External EPROM pins (MB89PV670A only)**

Pin no.	Pin name	I/O	Function
82 83 84 85 86 87 88 89 90 91	A15 A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}/V_{PP}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V_{CC}	O	
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Crystal or ceramic oscillation type • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS output • CMOS inout • Pull-up resistor optional (except P22 and P23)
E		• CMOS output • CMOS input • The peripheral is a hysteresis input type. • Pull-up resistor optional

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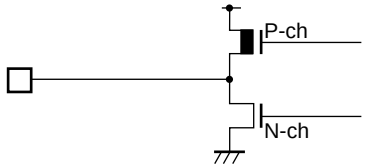
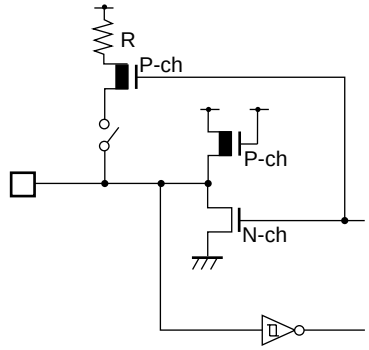
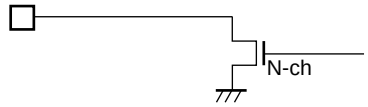
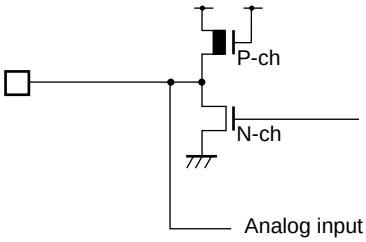
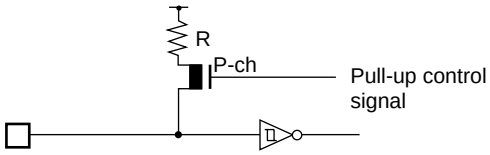
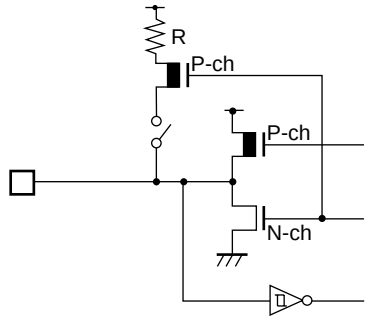
Type	Circuit	Remarks
F		• CMOS output
G		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional
H		• N-ch open-drain output
I		• N-ch open-drain output • Analog input
J		• Hysteresis input • With software pull-up resistor
K		• CMOS output • Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P677A

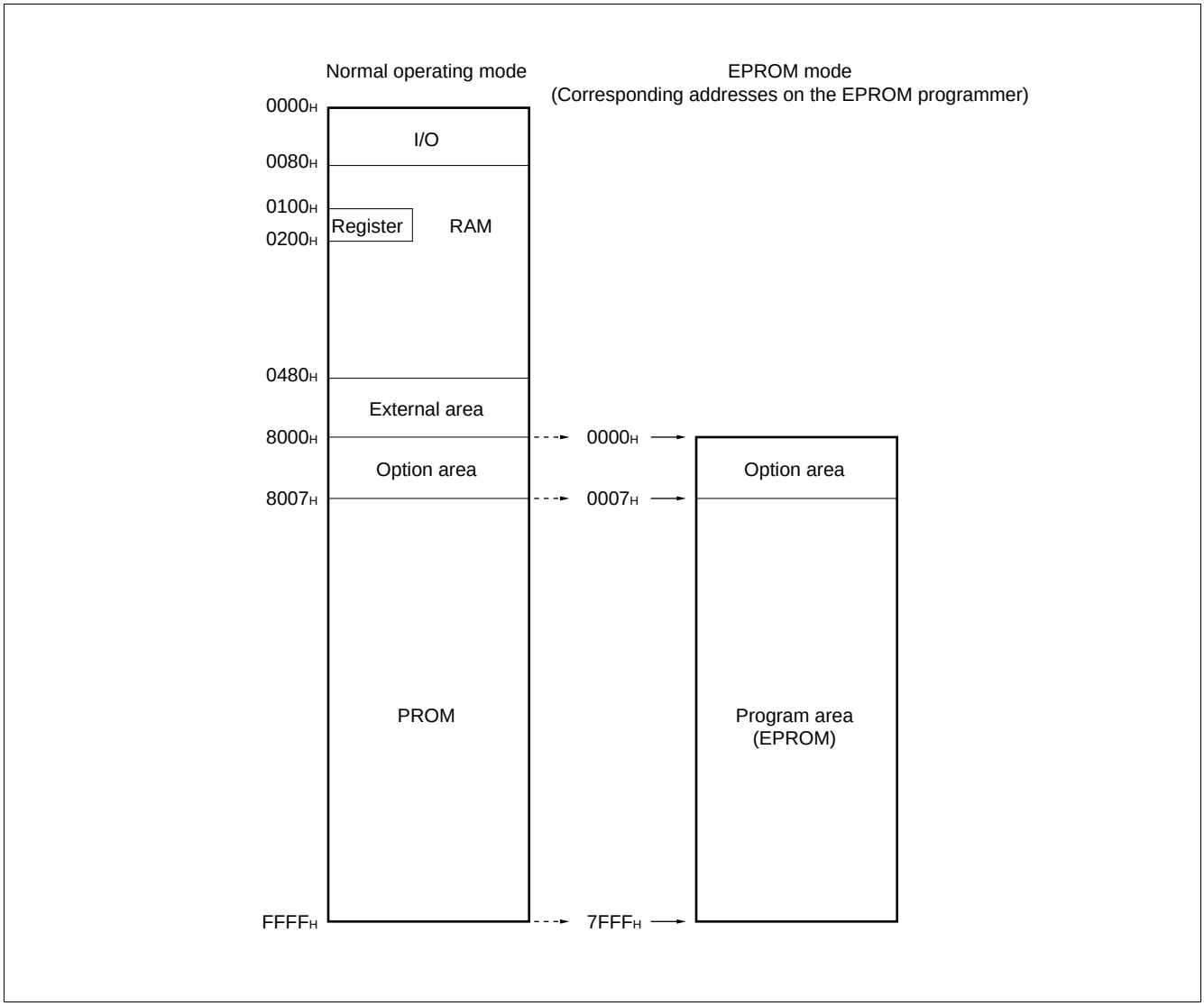
The MB89P677A is an OTPROM version of the MB89670/A series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in the EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P677A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

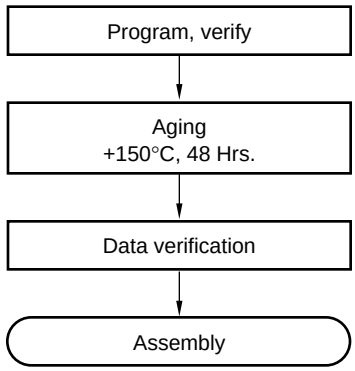
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$ (note that addresses 8007_H to $FFFF_H$ while operating as a normal operating mode assign to 0007_H to $7FFF_H$ in EPROM mode).
Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see “7. Bit Map for PROM Options.”)

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M11	ROM-80QF2-28DP-8L
FPT-80P-M06	ROM-80QF-28DP-8L2

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: Depending on the EPROM programmer, inserting a capacitor of about 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

7. PROM Option Bit Map

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization time 00: $2^4/F_C$ 10: $2^{17}/F_C$	 01: $2^{14}/F_C$ 11: $2^{18}/F_C$
0001_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0002_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0003_H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0004_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
0005_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
0006_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	P04 to P07 Pull-up 1: No 0: Yes	P00 to P03 Pull-up 1: No 0: Yes	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes

Notes:
- Set each bit to 1 to erase.
- Do not write 0 to the vacant bit.
  The read value of the vacant bit is 1, unless 0 is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

2. Programming Socket Adapter

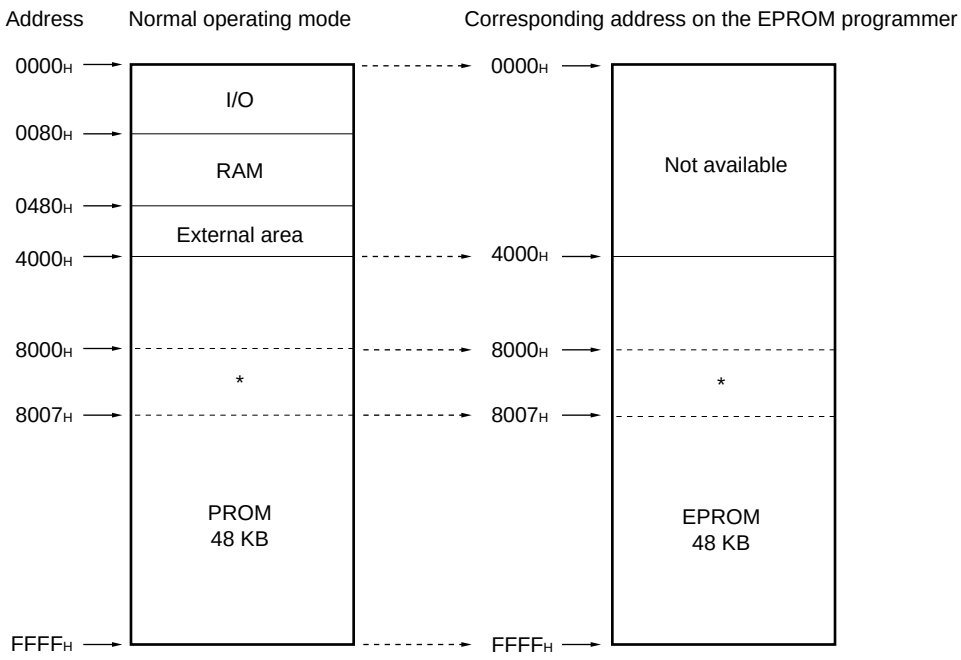
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode is diagrammed below.



*: Note that for the MB89P677A this area comprise an option setting area.

4. Programming to the EPROM

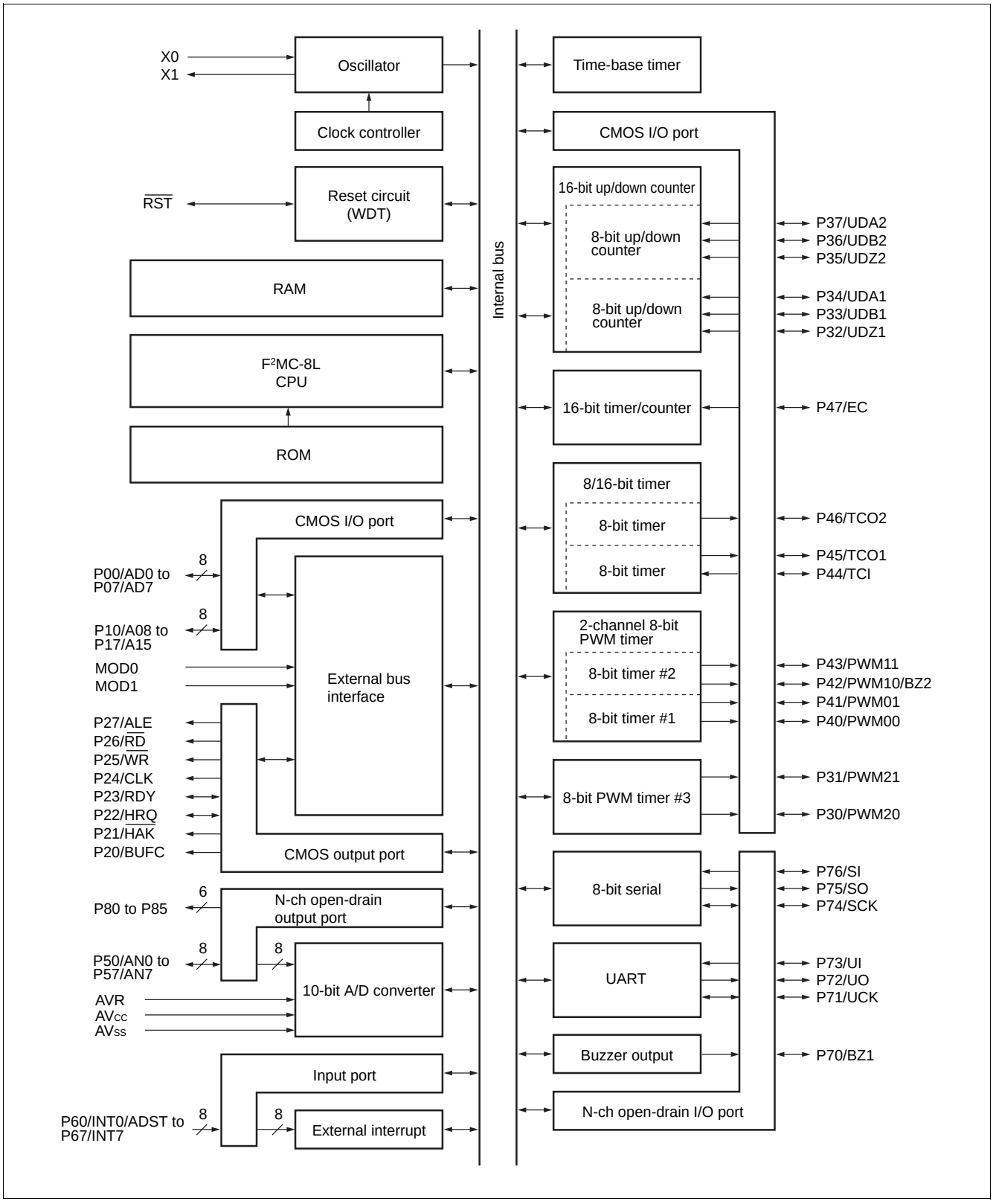
(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 4000_H to $FFFF_H$.

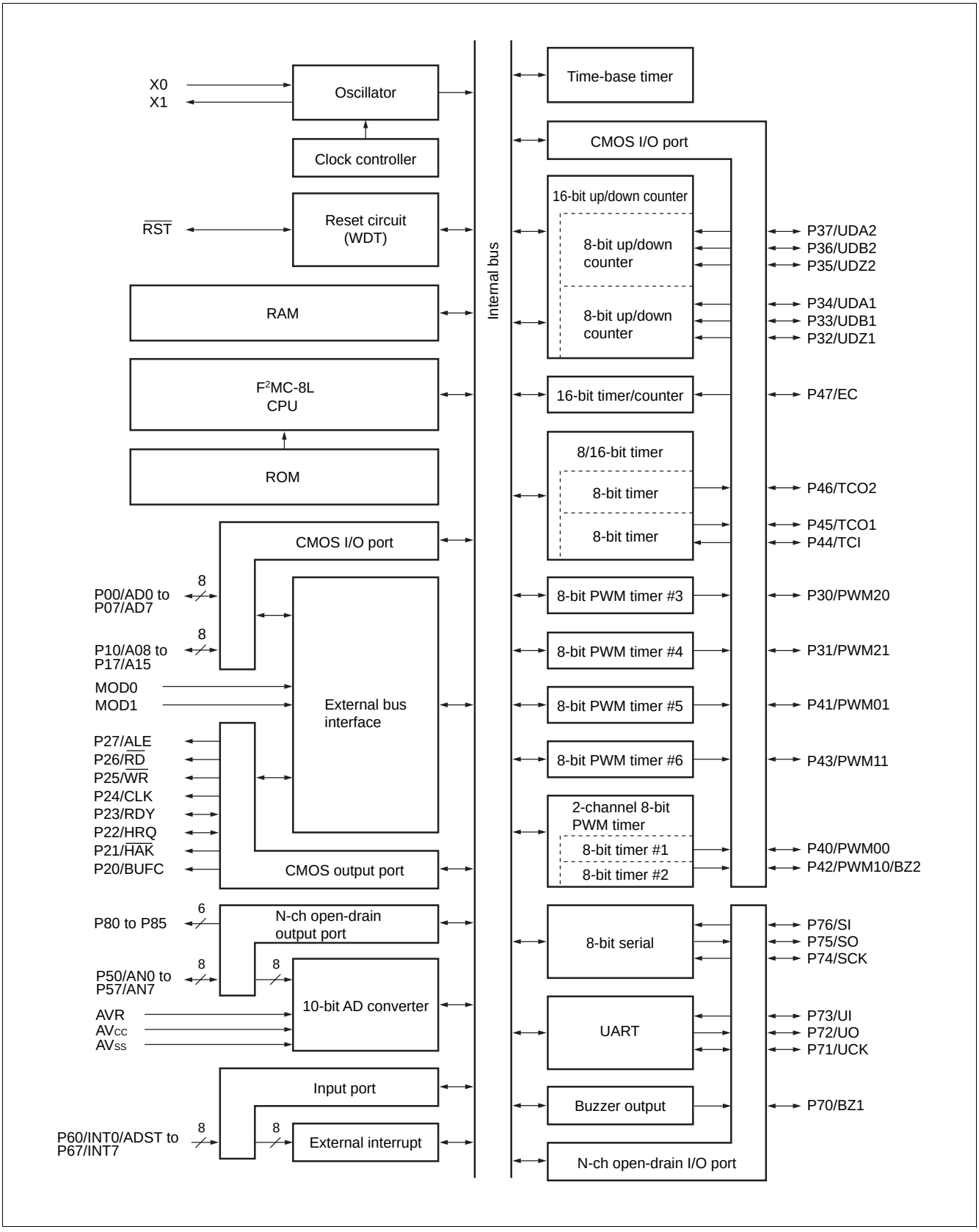
(3) Program to 4000_H to $FFFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

1. MB89673



2. MB89677A/89P677A/89PV670A

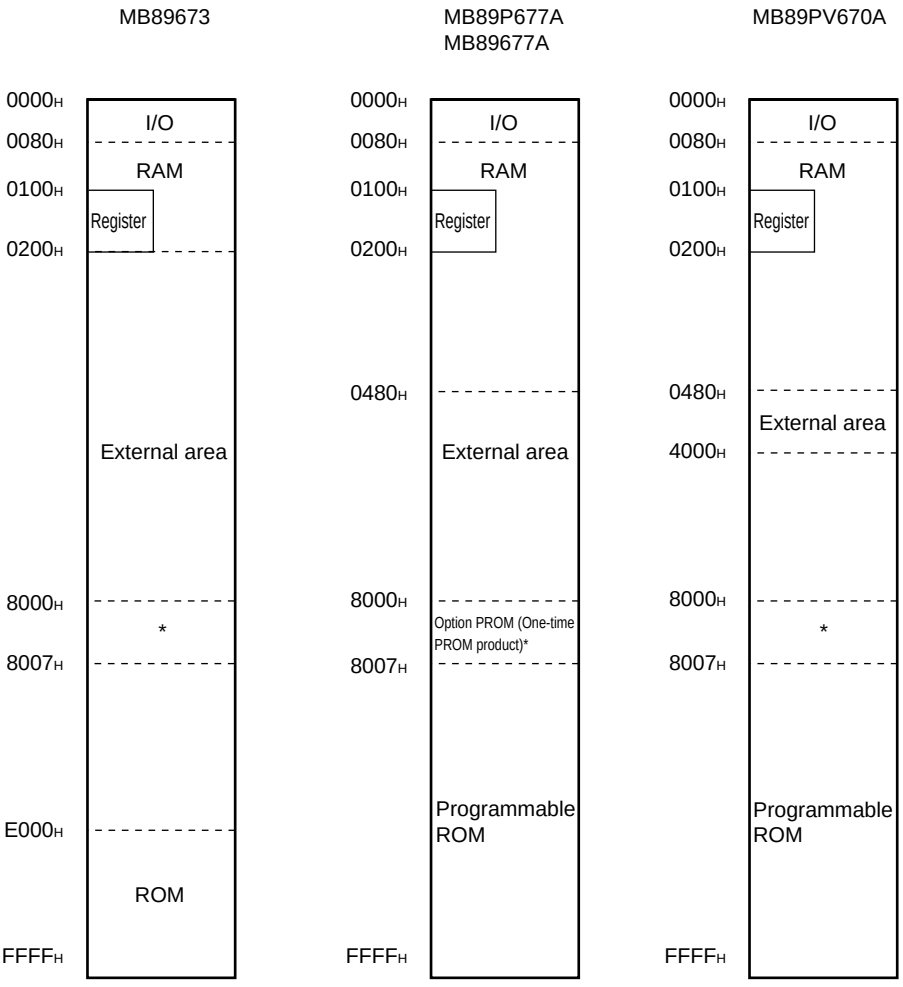


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89670/A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89670/A series is structured as illustrated below.

Memory Space

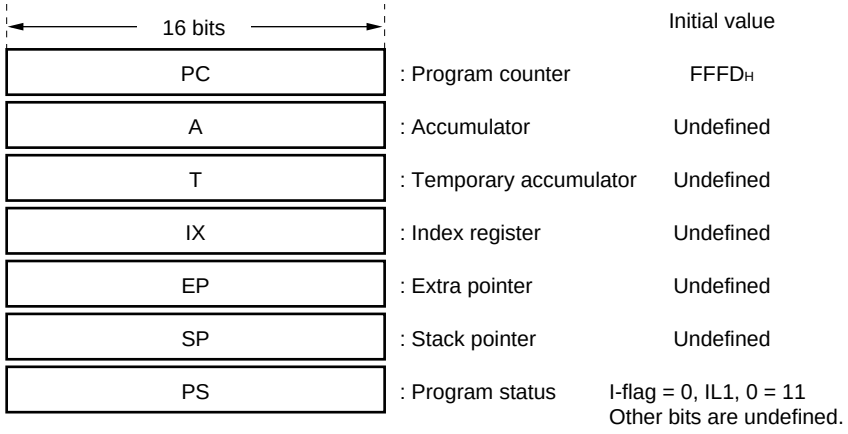


*: Since addresses 8000H to 8006H for the MB89P677A comprise an option area, do not use this area for the other products in this series.

2. Registers

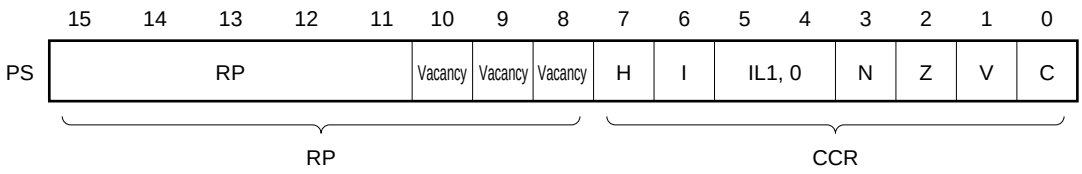
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



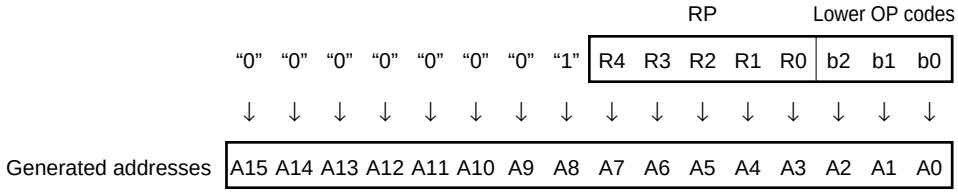
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

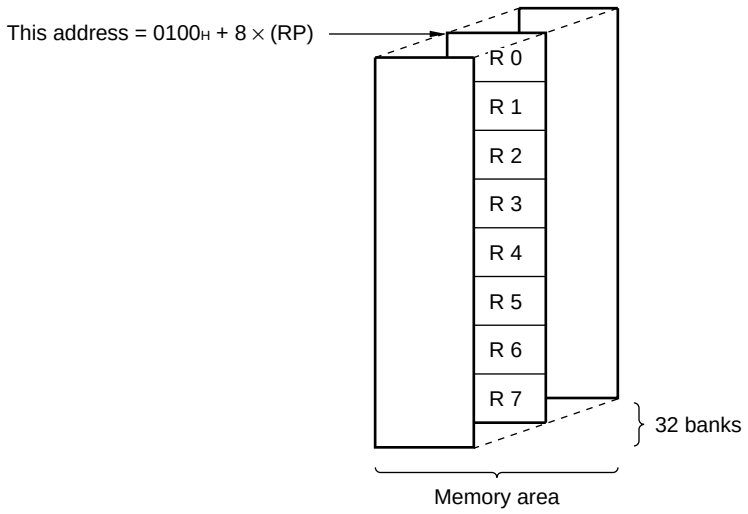
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89677A. On the MB89673, there are 16 banks in internal RAM. The remaining 16 banks can be extended externally by allocating an external RAM to addresses 0180_H to $01FF_H$ using an external circuit. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description	Initial value
00H	(R/W)	PDR0	Port 0 data register	XXXX XXXXB
01H	(W)	DDR0	Port 0 data direction register	0000 0000B
02H	(R/W)	PDR1	Port 1 data register	XXXX XXXXB
03H	(W)	DDR1	Port 1 data direction register	0000 0000B
04H	(R/W)	PDR2	Port 2 data register	0000 0000B
05H	(W)	BCTR	External bus pin control register	XXXX XX01B
06H			Vacancy	
07H	(R/W)	SYCC	System clock control register	X– –M MX00B
08H	(R/W)	STBC	Standby control register	0001 XXXXB
09H	(R/W)	WDTE	Watchdog timer control register	XXXX XXXXB
0AH	(R/W)	TBCR	Time-base timer control register	00XX X000B
0BH			Vacancy	
0CH	(R/W)	PDR3	Port 3 data register	XXXX XXXXB
0DH	(W)	DDR3	Port 3 data direction register	0000 0000B
0EH	(R/W)	PDR4	Port 4 data register	XXXX XXXXB
0FH	(W)	DDR4	Port 4 data direction register	0000 0000B
10H	(R/W)	PDR5	Port 5 data register	1111 1111B
11H	(R)	PDR6	Port 6 data register	XXXX XXXXB
12H	(R/W)	PPCR	Port 6 pull-up control register	0000 0000B
13H	(R/W)	PDR7	Port 7 data register	X111 1111B
14H	(R/W)	PDR8	Port 8 data/port 7 swiching register	0011 1111B
15H	(R/W)	BUZR	Buzzer control register	XXXX X000B
16H	(R/W)	CNTR	PWM control register #3	0000 0000B
17H	(R/W)	COMP	PWM compare register #3	XXXX XXXXB
18H	(R/W)	TMCR	16-bit timer control register	0000 0000B
19H	(R/W)	TCHR	16-bit timer count register H	0000 0000B
1AH	(R/W)	TCLR	16-bit timer count register L	0000 0000B
1BH			Vacancy	
1CH	(R/W)	SMR	Serial mode register	0000 0000B
1DH	(R/W)	SDR	Serial data register	XXXX XXXXB
1EH			Vacancy	
1FH			Vacancy	

–: Unused, X: Undefined, M: Set using the mask option

(Continued)

Address	Read/write	Register name	Register description	Initial value
20H	(R/W)	ADC1	A/D converter control register 1	0 0 0 0 0 0 0 0 B
21H	(R/W)	ADC2	A/D converter control register 2	X 0 0 0 0 0 0 1 B
22H	(R/W)	ADCH	A/D converter data register H	– – – – – – X X B
23H	(R/W)	ADCL	A/D converter data register L	X X X X X X X X B
24H	(R/W)	T2CR	Timer 2 control register	X 0 0 0 X X X 0 B
25H	(R/W)	T1CR	Timer 1 control register	X 0 0 0 X X X 0 B
26H	(R/W)	T2DR	Timer 2 data register	X X X X X X X X B
27H	(R/W)	T1DR	Timer 1 data register	X X X X X X X X B
28H	(R/W)	CNTR1	PWM timer control register 1	0 0 0 0 0 0 0 0 B
29H	(R/W)	CNTR2	PWM timer control register 2	0 0 0 0 0 0 0 0 B
2AH	(R/W)	CNTR3	PWM timer control register 3	X X X 0 0 0 0 0 B
2BH	(W)	COMR2	PWM timer compare register 2	X X X X X X X X B
2CH	(W)	COMR1	PWM timer compare register 1	X X X X X X X X B
2DH			Vacancy	
2EH			Vacancy	
2FH			Vacancy	
30H	(R) (W)	UDCR1 RCR1	Up/down counter register 1 Reload compare register1	X X X X X X X X B X X X X X X X X B
31H	(R) (W)	UDCR2 RCR2	Up/down counter register 2 Reload compare register2	X X X X X X X X B X X X X X X X X B
32H	(R/W)	CCRA1	Counter control register A1	0 0 0 0 0 0 0 0 B
33H	(R/W)	CCRA2	Counter control register A2	0 0 0 0 0 0 0 0 B
34H	(R/W)	CCRB1	Counter control register B1	0 0 0 0 0 0 0 0 B
35H	(R/W)	CCRB2	Counter control register B2	0 0 0 0 0 0 0 0 B
36H	(R/W)	CSR1	Counter status register 1	0 0 0 0 0 0 0 0 B
37H	(R/W)	CSR2	Counter status register 2	0 0 0 0 0 0 0 0 B
38H	(R/W)	EIC1	External interrupt 1 control register 1	0 0 0 0 0 0 0 0 B
39H	(R/W)	EIC2	External interrupt 1 control register 2	0 0 0 0 0 0 0 0 B
3AH	(R/W)	EIE2	External interrupt 2 enable register	0 0 0 0 0 0 0 0 B
3BH	(R/W)	EIF2	External interrupt 2 flag register	X X X X 0 0 0 0 B
3CH			Vacancy	
3DH			Vacancy	
3EH			Vacancy	
3FH			Vacancy	

–: Unused, X: Undefined, M: Set using the mask option

(Continued)

(Continued)

Address	Read/write	Register name	Register description	Initial value
40H	(R/W)	USMR	UART mode register	0 0 0 0 0 0 0 0 B
41H	(R/W)	USCR	UART control register	0 0 0 0 0 0 0 0 B
42H	(R/W)	USTR	UART status register	0 0 0 0 1 X X X B
43H	(R) (W)	RXDR TXDR	UART receiver data register UART transmitter data register	X X X X X X X X B X X X X X X X X B
44H			Vacancy	
45H	(R/W)	RRDR	Baud rate generator reload data register	X X X X X X X X B
46H			Vacancy	
47H			Vacancy	
48H*	(R/W)	CNTR #4	PWM timer control register #4	0 X 0 0 0 0 0 0 B
49H*	(R/W)	COMP #4	PWM timer compare register #4	X X X X X X X X B
4AH*	(R/W)	CNTR #5	PWM timer control register #5	0 X 0 0 0 0 0 0 B
4BH*	(R/W)	COMP #5	PWM timer compare register #5	X X X X X X X X B
4CH*	(R/W)	CNTR #6	PWM timer control register #6	0 X 0 0 0 0 0 0 B
4DH*	(R/W)	COMP #6	PWM timer compare register #6	X X X X X X X X B
4E to 7AH			Vacancy	
7BH			Vacancy	
7CH	(W)	ILR1	Interrupt level setting register 1	1 1 1 1 1 1 1 1 B
7DH	(W)	ILR2	Interrupt level setting register 2	1 1 1 1 1 1 1 1 B
7EH	(W)	ILR3	Interrupt level setting register 3	1 1 1 1 1 1 1 1 B
7FH			Vacancy	

–: Unused, X: Undefined, M: Set using the mask option

* : For the MB89673, these are vacancies.

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*
	AV_{CC}	V_{SS} – 0.3	V_{CC} + 0.3	V	
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{CC} + 0.3	V	AVR must not exceed AV_{CC} + 0.3 V.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P80 to P85
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P80 to P85
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating rate)
	I_{OLAV2}	—	8	mA	Average value (operating current × operating rate) P80 to P85
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AVR does not exceed AV_{CC} + 0.3 V and AV_{CC} does not exceed V_{CC}, such as when power is turned on.

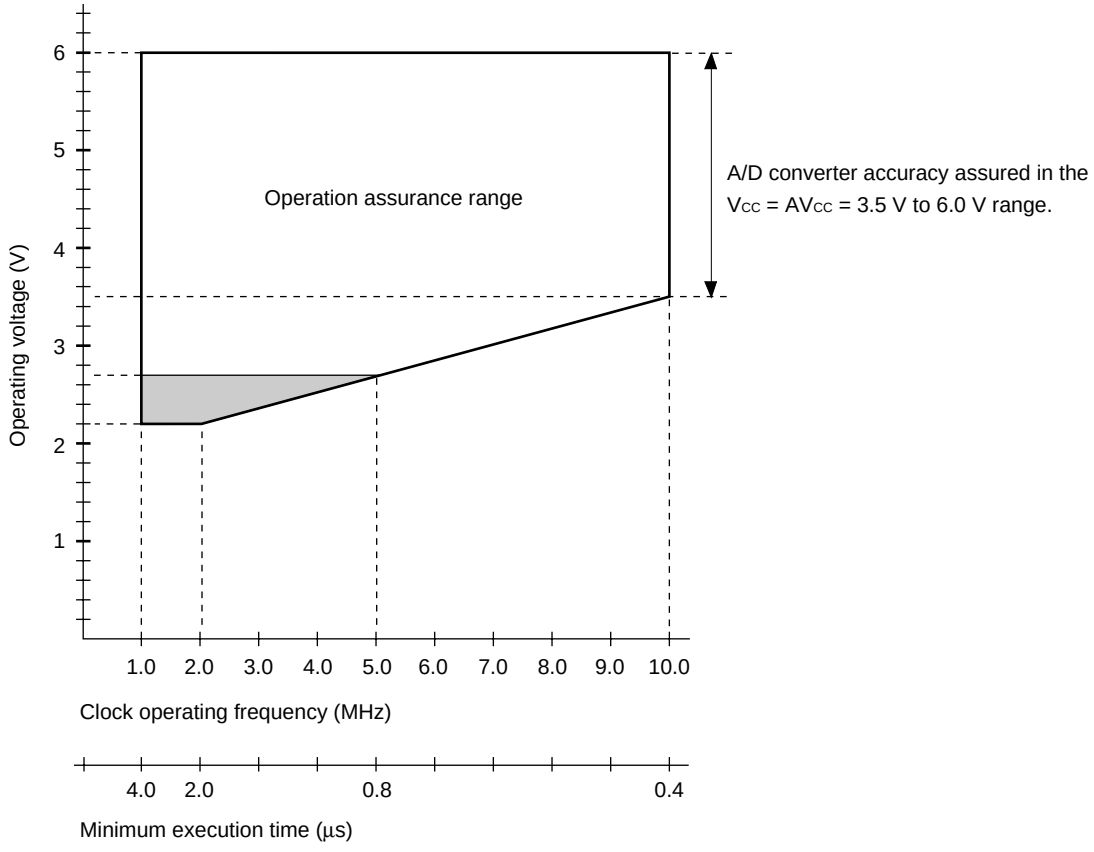
Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0	V	Normal operation assurance range MB89673/677A
		2.7*	6.0	V	Normal operation assurance range MB89PV670A/P677A
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."



Note: The shaded area is assured only for the MB89673/677A.

Figure 1 Operating Voltage vs. Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an minimum execution time of 4/F_C.

Since the operating voltage range is dependent on the minimum execution time, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P30 to P37, P40 to P47	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P32 to P37, P44, and P47 are port input.
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P32 to P37, P44, P47, P60 to P67, P70 to P76		0.8 V_{CC}	—	V_{CC} + 0.3	V	P32 to P37, P44, and P47 are peripheral input.
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47		V_{SS} – 0.3	—	0.3 V_{CC}	V	P32 to P37, P44, and P47 are port input.
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, P32 to P37, P44, P47, P60 to P67, P70 to P76		V_{SS} – 0.3	—	0.2 V_{CC}	V	P32 to P37, P44, and P47 are peripheral input.
Open-drain output pin application voltage	V_D	P80 to P85		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P71, P72, P74, P75	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P76	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P80 to P85	I_{OL} = 10 mA	—	—	0.5	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P76, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
	I_{LI2}	P80 to P85	0.0 V < V_I < V_{CC}	—	—	±1	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P60 to P67, P70 to P76, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC1}	V_{CC}	F_C = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_C = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1	2	mA	MB89673, MB89677A, MB89PV670A
				—	1.5	2.5	mA	MB89P677A
	I_{CCS1}		Sleep mode: F_C = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_C = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1	1.5	mA	
	I_{CCH}		V_{CC} = 3.0 V, T_A = +25°C, Stop mode	—	—	1	mA	
	I_A	AV_{CC}	F_C = 10 MHz, When A/D converter starts	—	6	8	mA	
	I_{AH}		F_C = 10 MHz, T_A = +25°C, When A/D converter stops	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The measurement conditions of the power supply current are as follows: the external clock and open output pins.

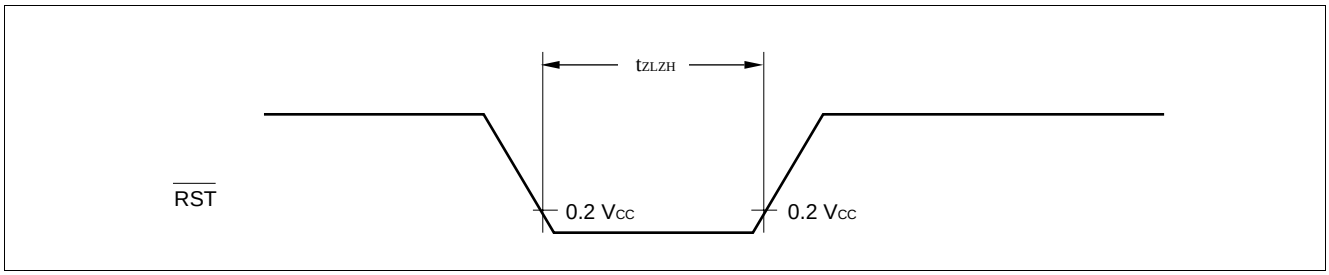
*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

4. AC Characteristics

(1) Reset Timing

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

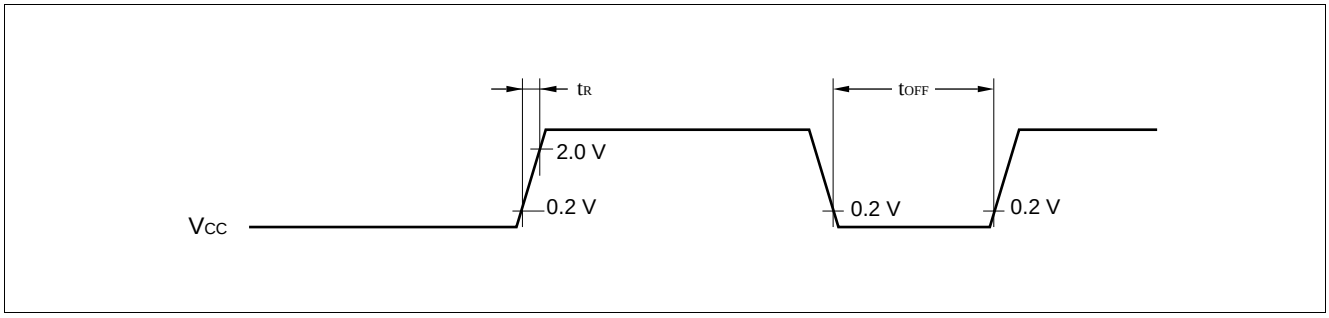


(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

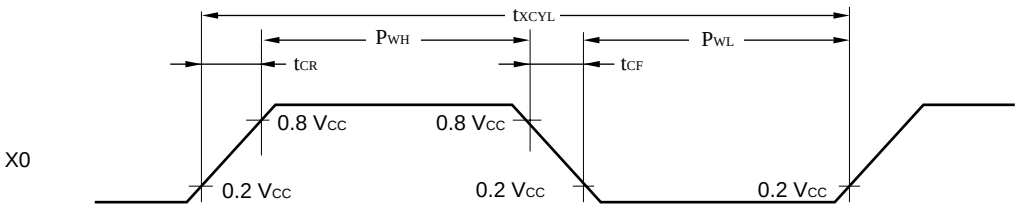


(3) Clock Timing

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

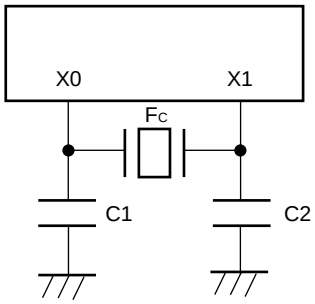
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	10	MHz	
Clock cycle time	t_{XCYL}	X0, X1		100	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	10	ns	External clock

X0 and X1 Timing and Conditions

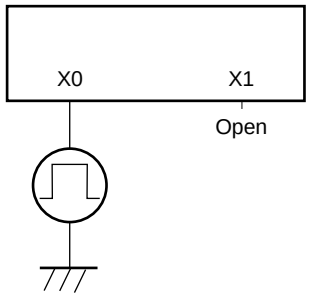


Clock Conditions

When a crystal or ceramic resonator is used



When an external clock is used

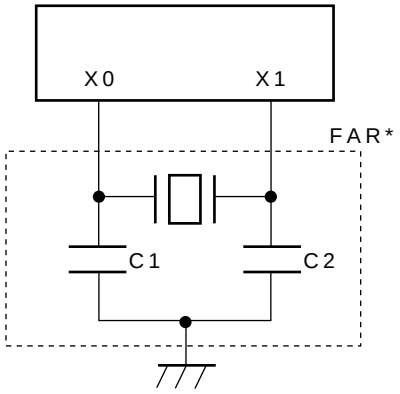


(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$, $8/F_C$, $16/F_C$, $64/F_C$	µs	$(4/F_C)$ t_{inst} = 0.4 µs when operating at F_C = 10 MHz

(5) Recommended Resonator Manufacturers

Sample Application of Piezoelectric Resonator (FAR series)

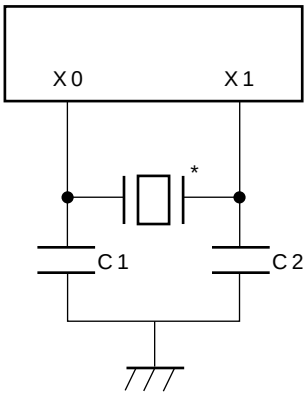


*: Fujitsu Acoustic Resonator
C1 = C2 = 20 pF±8 pF (built-in FAR)

FAR part number (built-in capacitor type)	Frequency	Initial deviation of FAR frequency (T_A = +25°C)	Temperature characteristics of FAR frequency (T_A = –20°C to +60°C)
FAR-C4CB-08000-M02	8.00 MHz	±0.5%	±0.5%
FAR-C4CB-10000-M02	10.00 MHz	±0.5%	±0.5%

Inquiry: FUJITSU LIMITED

Sample Application of Ceramic Resonator



Resonator manufacturer*	Resonator	Frequency	C1 (pF)	C2 (pF)	R (kΩ)
Kyocera Corporation	KBR-7.68MWS	7.68 MHz	33	33	—
	KBR-8.0MWS	8.0 MHz	33	33	—
Murata Mfg. Co., Ltd.	CSA8.00MTZ	8.0 MHz	30	30	—

Inquiry: Kyocera Corporation

- AVX Corporation
  North American Sales Headquarters: TEL 1-803-448-9411
- AVX Limited
  European Sales Headquarters: TEL 44-1252-770000
- AVX/Kyocera H.K. Ltd.
  Asian Sales Headquarters: TEL 852-363-3303

Murata Mfg. Co., Ltd.

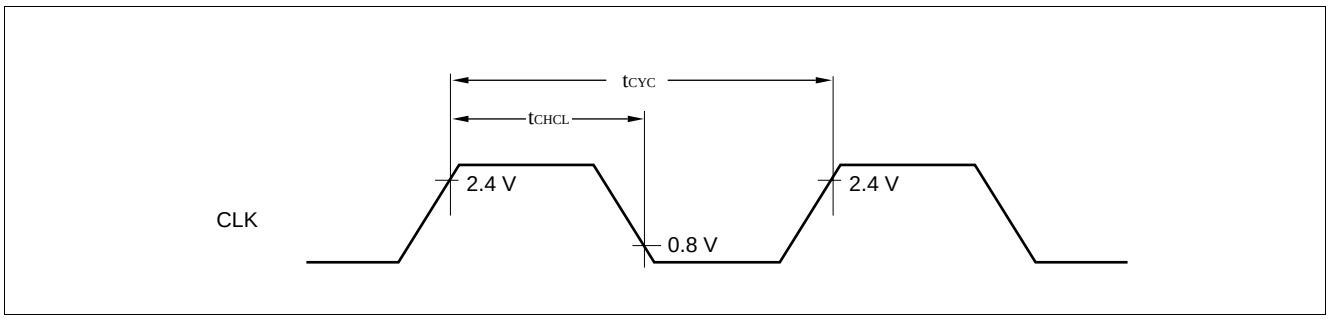
- Murata Electronics North America, Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

(6) Clock Output Timing

(AV_{CC} = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	1/2 t_{inst}*	—	µs	
CLK ↑ → CLK ↓	t_{CHCL}	CLK		1/4 t_{inst} – 0.07	1/4 t_{inst}	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

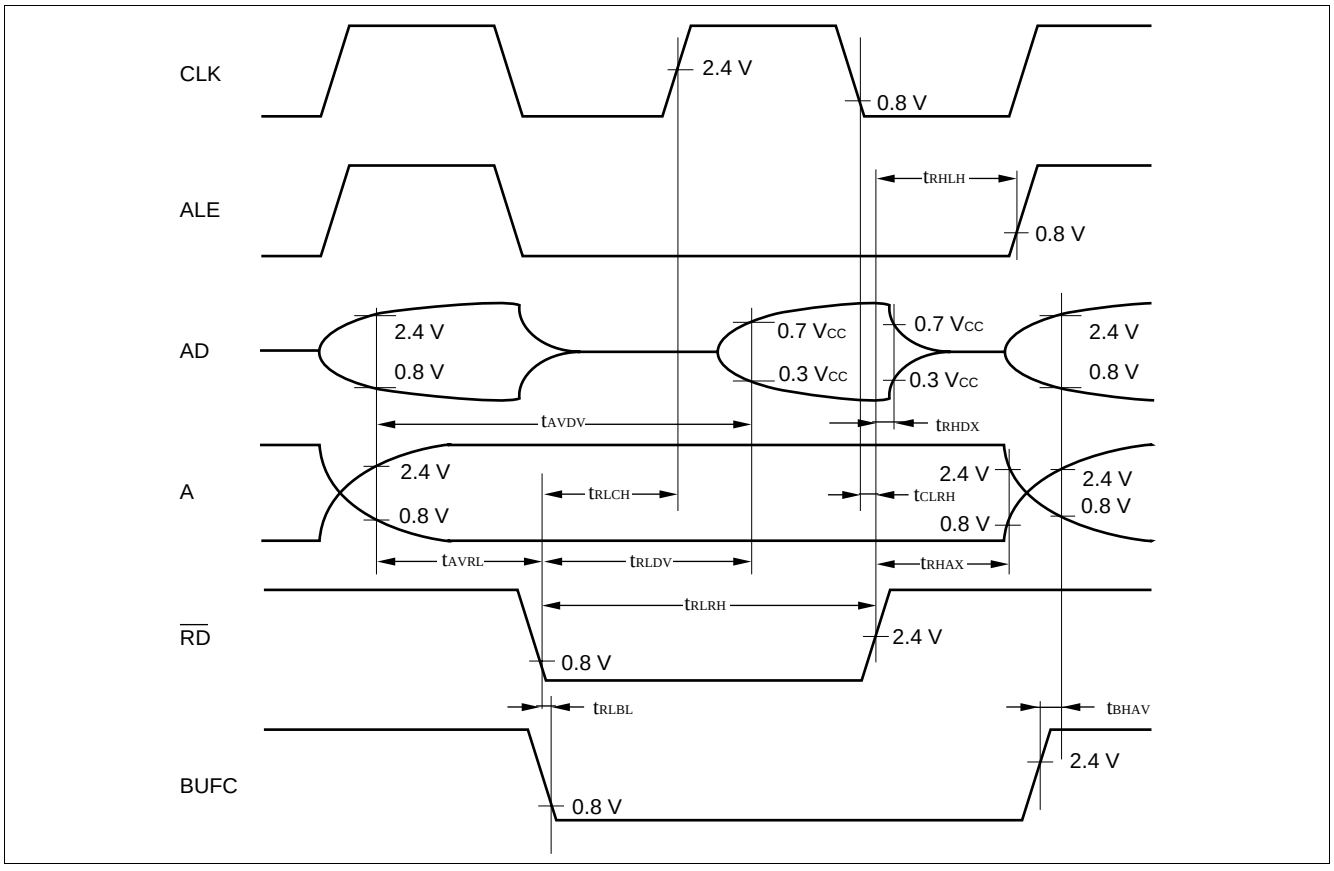


(7) Bus Read Timing

(AV_{CC} = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to 08, AD7 to 0	—	1/4 t_{inst}* – 0.06	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst} *– 0.02	—	µs	
Valid address → Data read time	t_{AVDV}	AD7 to 0, A15 to 08		—	1/2 t_{inst} *	µs	Wait
$\overline{RD}$ ↓ → Data read time	t_{RLDV}	$\overline{RD}$, AD7 to 0		—	1/2 t_{inst} *– 0.08	µs	No wait
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	AD7 to 0, $\overline{RD}$		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}* – 0.04	—	µs	
$\overline{RD}$ ↑ → Address loss time	t_{RHAX}	$\overline{RD}$, A15 to 08		1/4 t_{inst}* – 0.04	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}* – 0.04	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}	$\overline{RD}$, CLK		0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	ns	
BUFC ↑ → Valid address time	t_{BHAV}	A15 to 08, AD7 to 0, BUFC		5	—	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



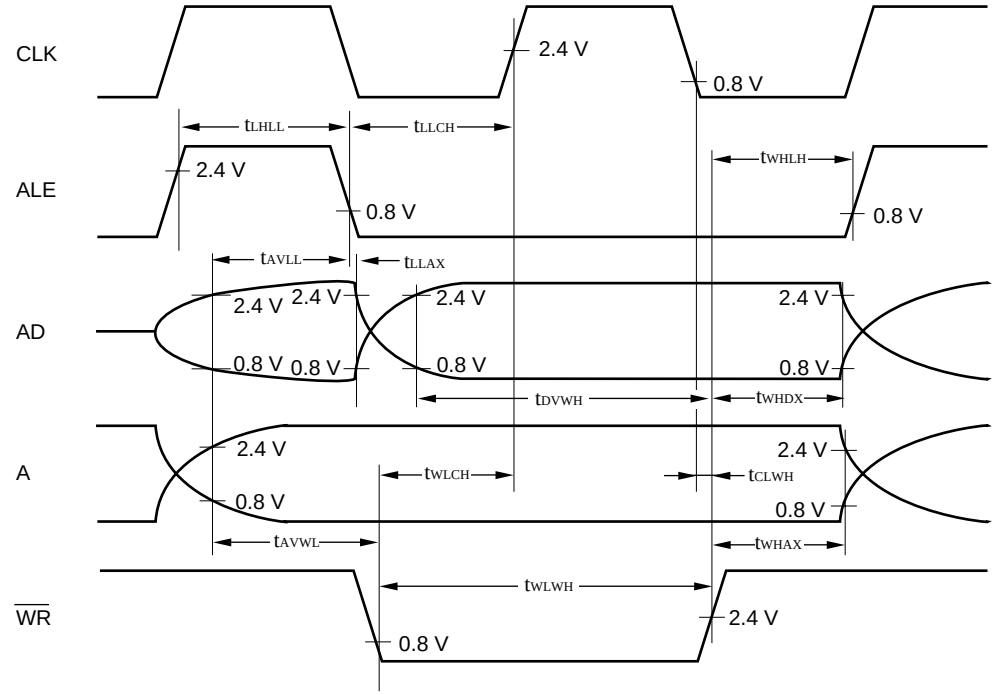
(8) Bus Write Timing

(AV_{CC} = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to 0, ALE, A15 to 08	—	1/4 t_{inst}*2 – 0.064	—	µs	
ALE ↓ time → Address loss time	t_{LLAX}	AD7 to 0, ALE, A15 to 08		5*1	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*2 – 0.06	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*2 – 0.02	—	µs	
Writing data → $\overline{WR}$ ↑ time	t_{DVWL}	AD7 to 0, $\overline{WR}$		1/2 t_{inst}*2 – 0.06	—	ns	
$\overline{WR}$ ↑ → Address loss time	t_{WHAX}	$\overline{WR}$, A15 to 08		1/4 t_{inst}*2 – 0.04	—	µs	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD7 to 0, $\overline{WR}$		1/4 t_{inst}*2 – 0.04	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}* – 0.04	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*2 – 0.04	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}	$\overline{WR}$, CLK		0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*2 – 0.035	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE, CLK		1/4 t_{inst}*2 – 0.03	—	µs	

*1: These characteristics are also applicable to the bus read timing.

*2: For information on t_{inst}, see “(4) Instruction Cycle.”

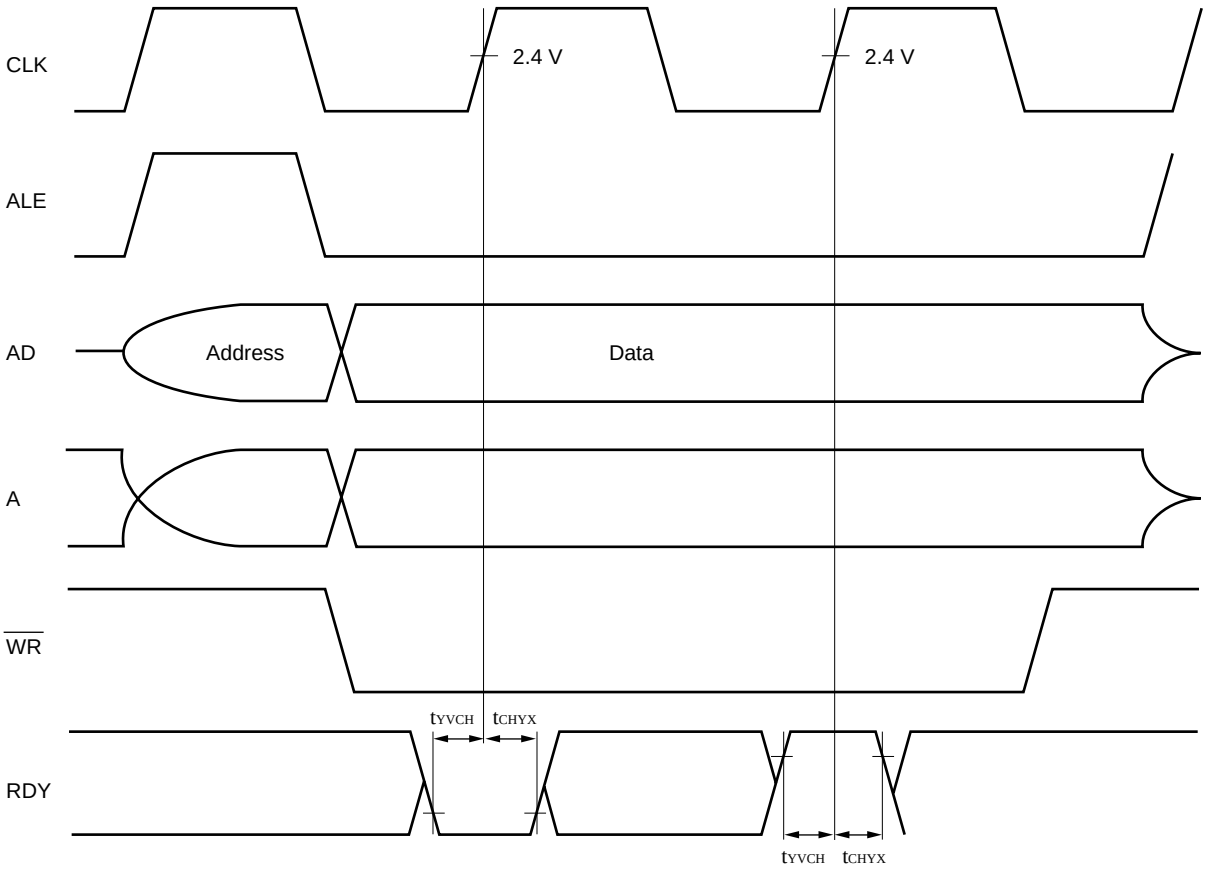


(9) Ready Input Timing

(AV_{CC} = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY invalid time	t_{CHYX}	RDY, CLK		0	—	ns	*

* : These characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

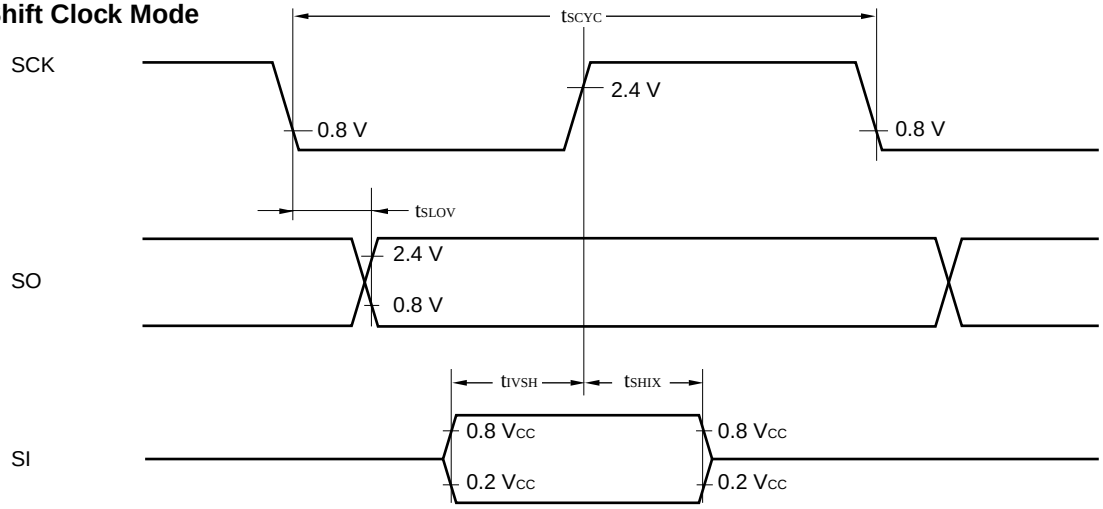
(10) Serial I/O Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

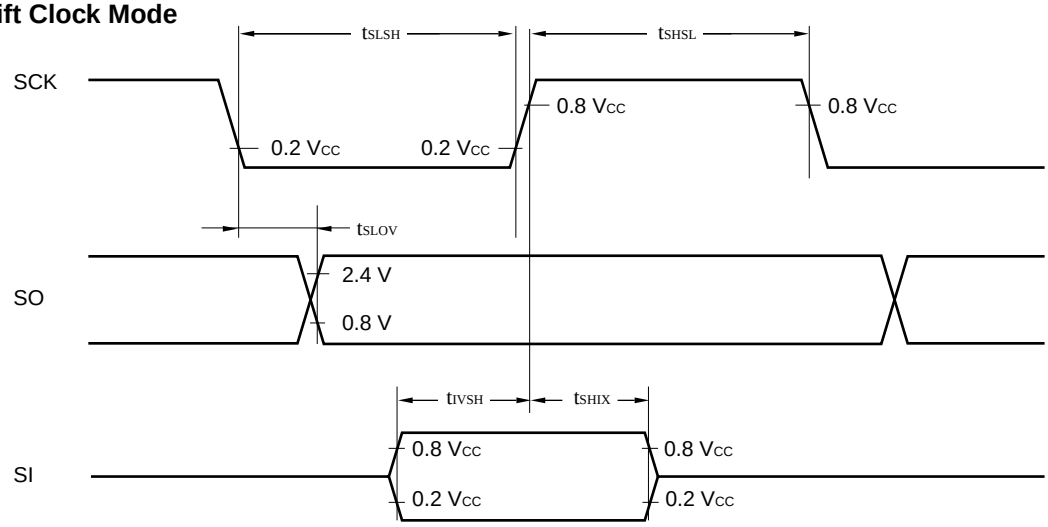
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

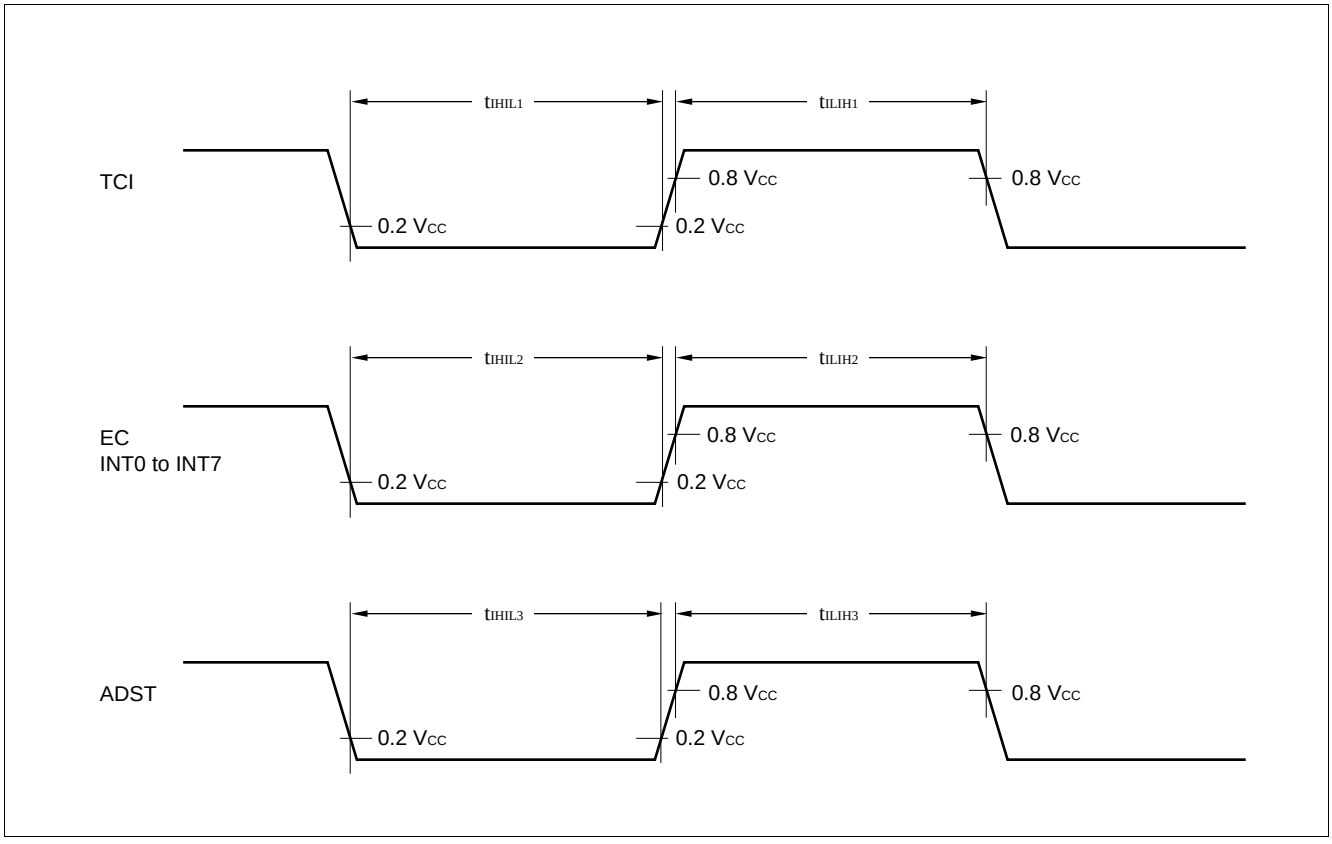


(11) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	TCI	—	1 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}	TCI		1 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	EC, INT0 to INT7		2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}	EC, INT0 to INT7		2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	A/D mode	64 t_{inst}*	—	µs	
Peripheral input “L” pulse width 3	t_{IHIL3}	ADST		64 t_{inst}*	—	µs	
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	Sense mode	64 t_{inst}*	—	µs	
Peripheral input “L” pulse width 3	t_{IHIL3}	ADST		64 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

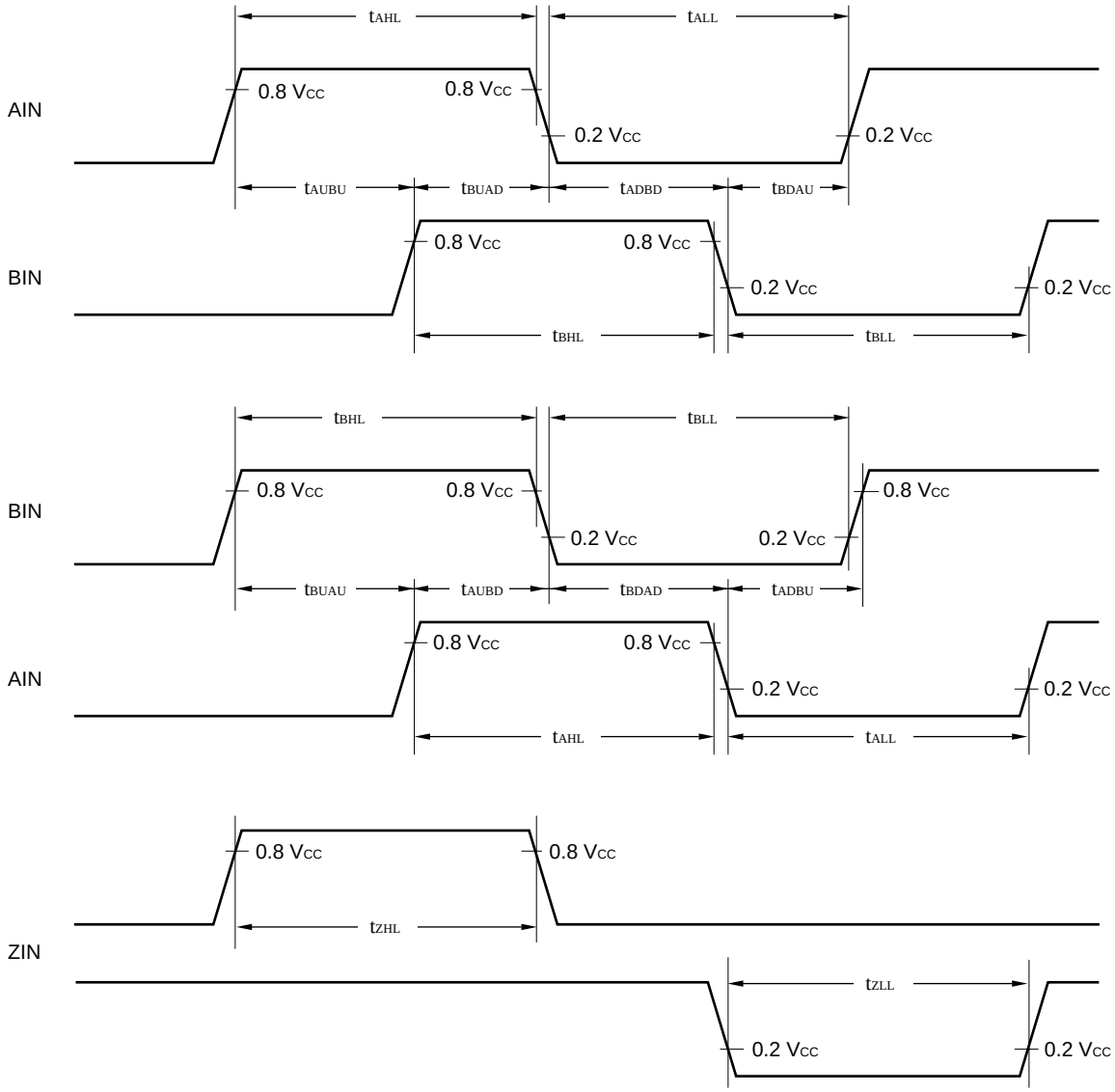


(12) Up/down Counter Input Timing

(AV_{CC} = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
AIN input “1” pulse width	t_{AHL}	P36, P37, P33, P34	—	2 t_{inst}*	—	µs	
AIN input “0” pulse width	t_{ALL}			2 t_{inst}*	—	µs	
BIN input “1” pulse width	t_{BHL}			2 t_{inst}*	—	µs	
BIN input “0” pulse width	t_{BLL}			2 t_{inst}*	—	µs	
AIN ↑ → BIN ↑ time	t_{AUBU}			1 t_{inst}*	—	µs	
BIN ↑ → AIN ↓ time	t_{BUAD}			1 t_{inst}*	—	µs	
AIN ↓ → BIN ↓ time	t_{ADBD}			1 t_{inst}*	—	µs	
BIN ↓ → AIN ↑ time	t_{BDAU}			1 t_{inst}*	—	µs	
BIN ↑ → AIN ↑ time	t_{BUAU}			1 t_{inst}*	—	µs	
AIN ↑ → BIN ↓ time	t_{AUBD}			1 t_{inst}*	—	µs	
BIN ↓ → AIN ↓ time	t_{BDAD}			1 t_{inst}*	—	µs	
AIN ↓ → BIN ↑ time	t_{ADBU}			1 t_{inst}*	—	µs	
ZIN input “1” pulse width	t_{ZHL}	P32, P35		1 t_{inst}*	—	µs	
ZIN input “0” pulse width	t_{ZLL}			1 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”


AIN
BIN
BIN
AIN
ZIN
tAHL
tALL
0.8 VCC
0.2 VCC
tAUBU
tBUAD
tADBD
tBDAU
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tZHL
tZLL

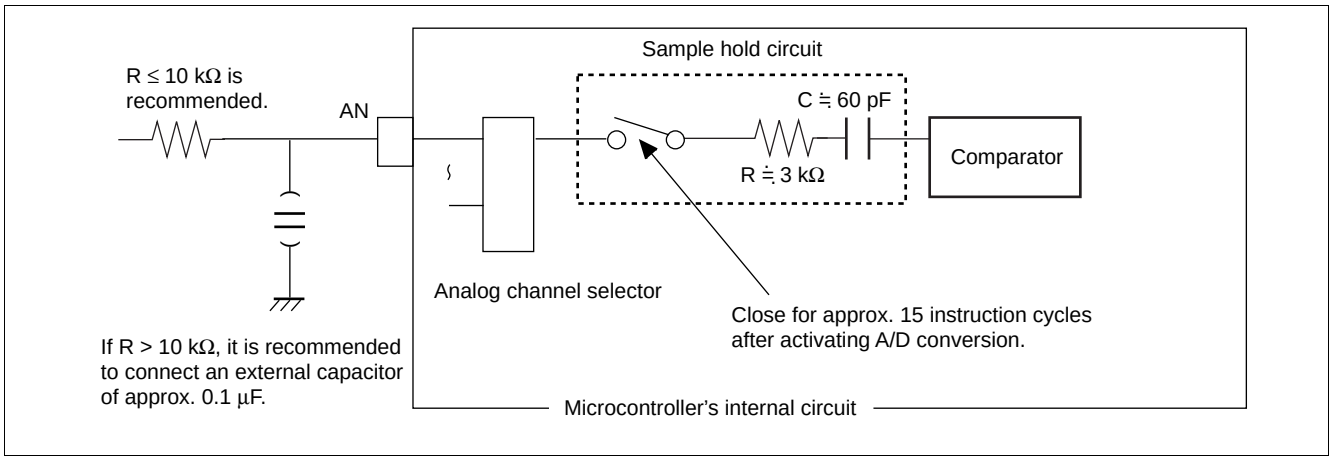
5. A/D Converter Electrical Characteristics

(AV_{CC} = V_{CC} = +3.5 V to +6.0 V, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	
Linearity error			—	—	±2.0	LSB	AV_{CC} = AVR = V_{CC}
Differential linearity error			—	—	±1.5	LSB	
Total error			—	—	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	
Interchannel disparity	—	—	—	—	4	LSB	
A/D mode conversion time			—	—	13.2	µs	At 10-MHz oscillation
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	—	AN0 to AN7	0	—	AVR	V	
Reference voltage		AVR	0	—	AV_{CC}	V	
Reference voltage supply current	I_R	AVR	—	200	—	µA	AVR = 5.0 V

Precautions:
- The smaller | AVR – AV_{SS} |, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions:
  Output impedance of the external circuit < Approx. 10 kΩ
  If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10 MHz oscillation).

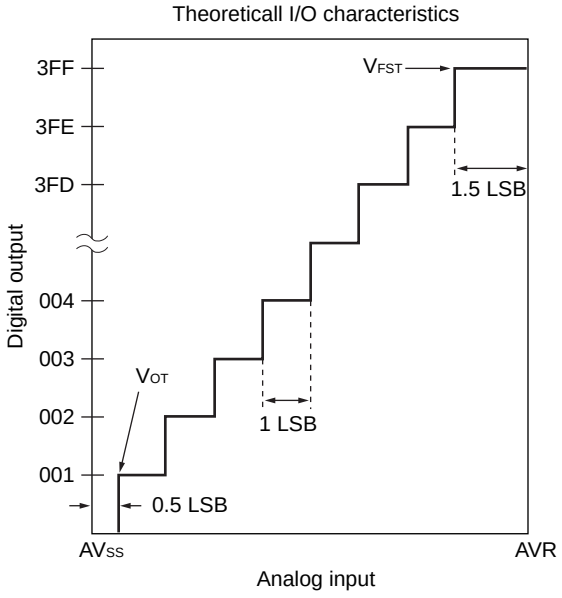
An analog input equivalent circuit is shown below.

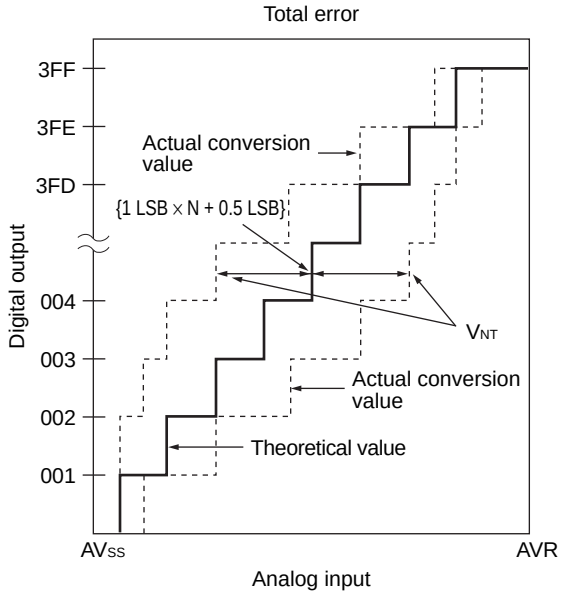


Since the A/D converter contains sample hold circuit, the level of the analog input pin might not stabilize within the sampling period after A/D activation, resulting in inaccurate A/D conversion values, if the input impedance to the analog pin is too high. Be sure to maintain an appropriate input impedance to the analog pin.
It is recommended to keep the input impedance to the analog pin not exceed 10 kΩ. If it exceeds 10 kΩ, it is recommended to connect a capacitor of approx. 0.1 µF for the analog input pin.
Except for the sampling period after A/D activation, the input leakage current of the analog input pin is less than 10 µA.

(1) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error
  The difference between theoretical and actual conversion values, caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise.





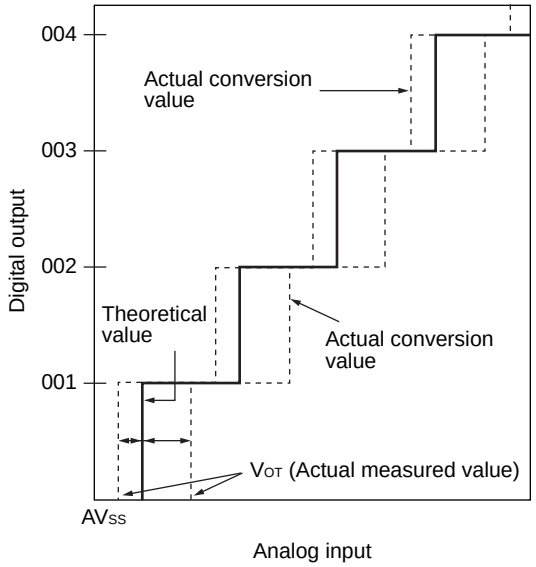
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)}$$

$$\text{Total error of digital output N} \quad \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

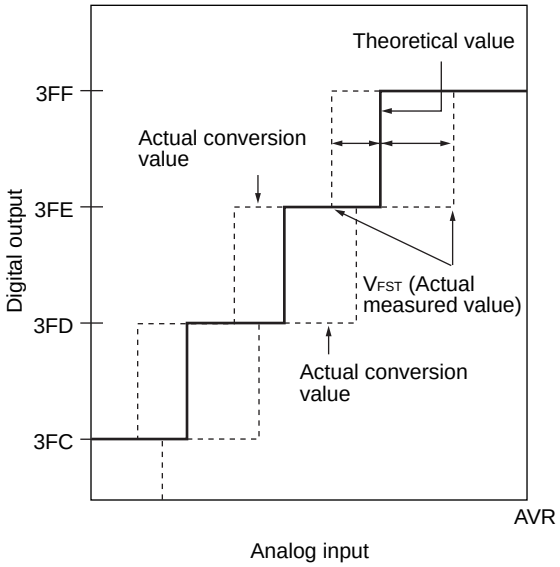
(Continued)

(Continued)

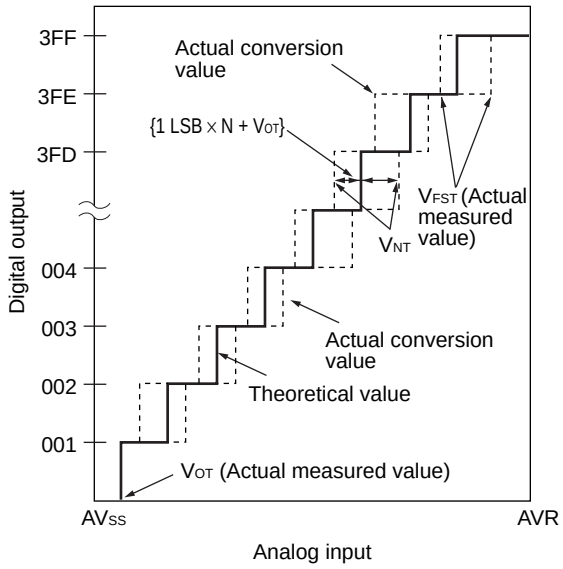
Zero transition error



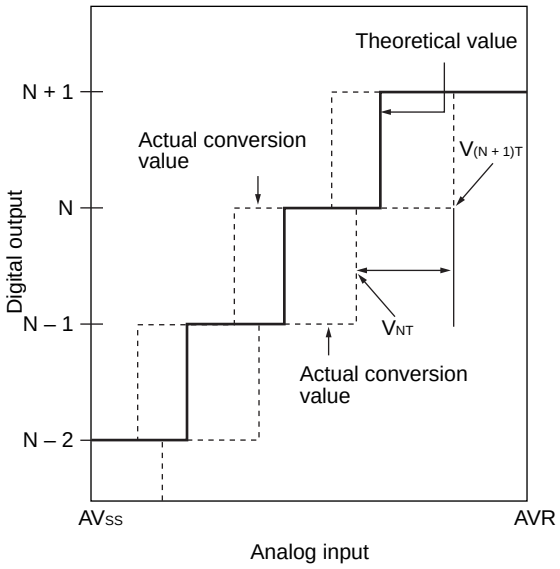
Full-scale transition error



Linearity error



Differential linearity error

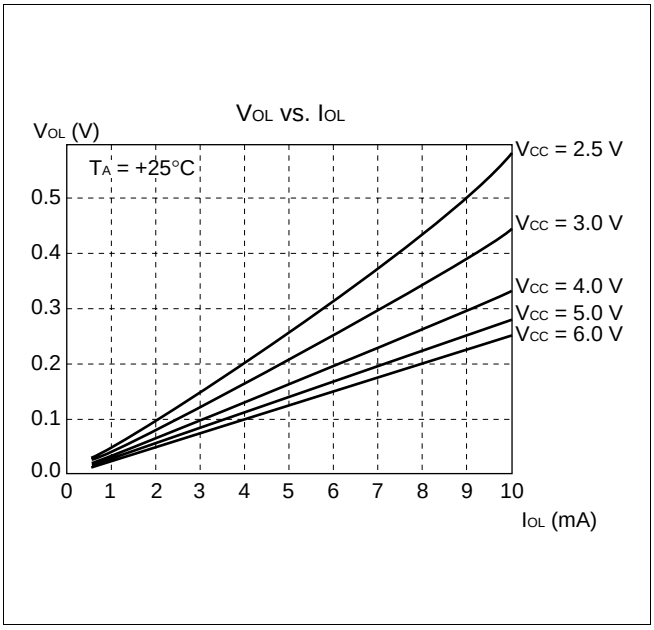


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

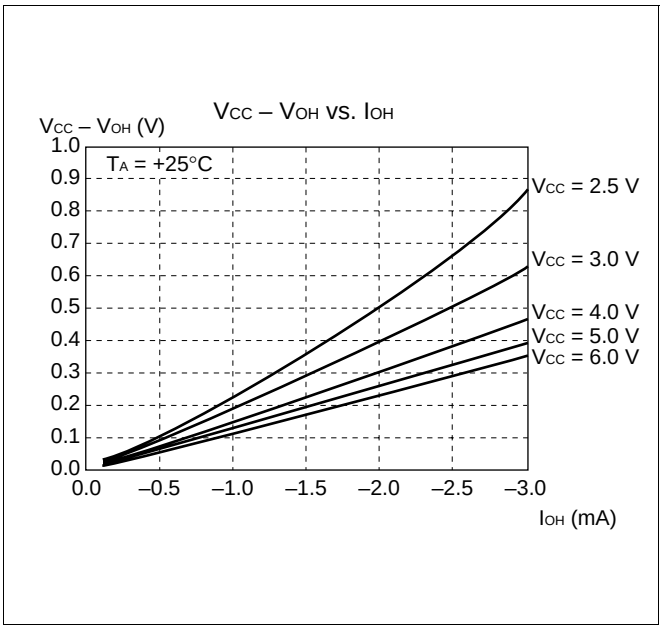
$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

■ EXAMPLE CHARACTERISTICS

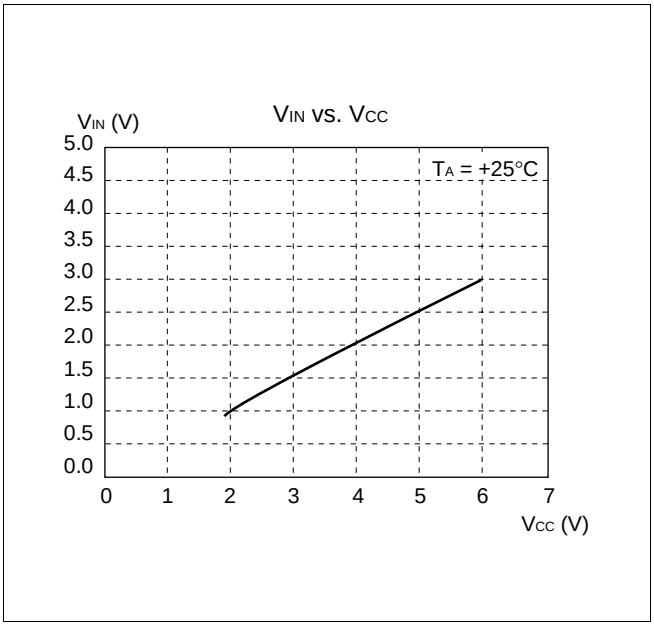
(1) “L” Level Output Voltage



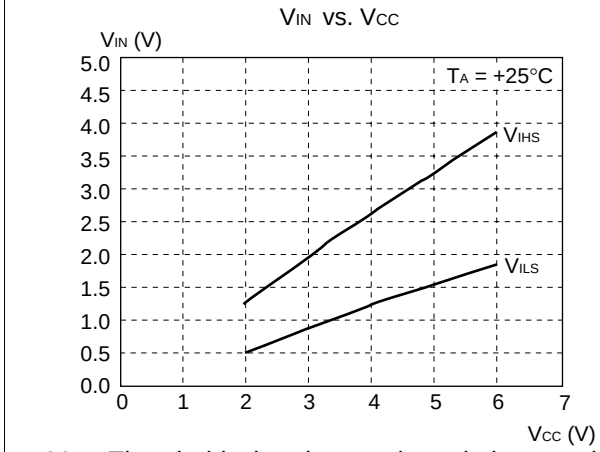
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



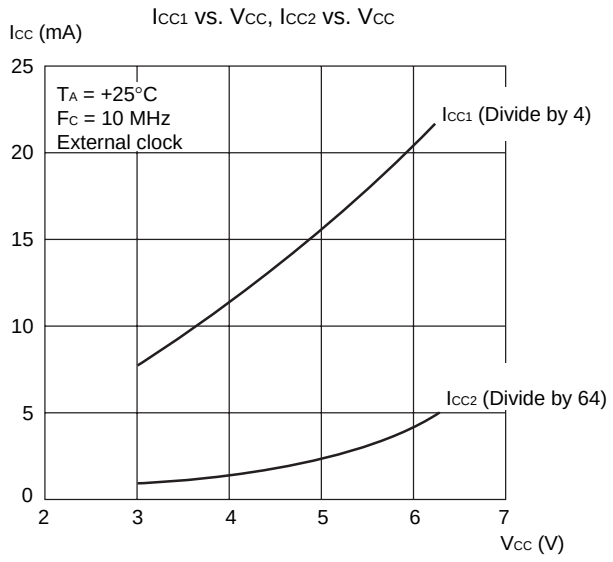
(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

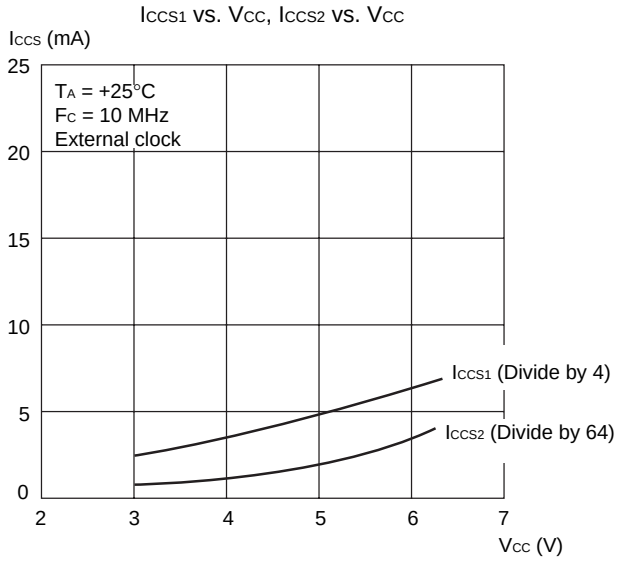


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

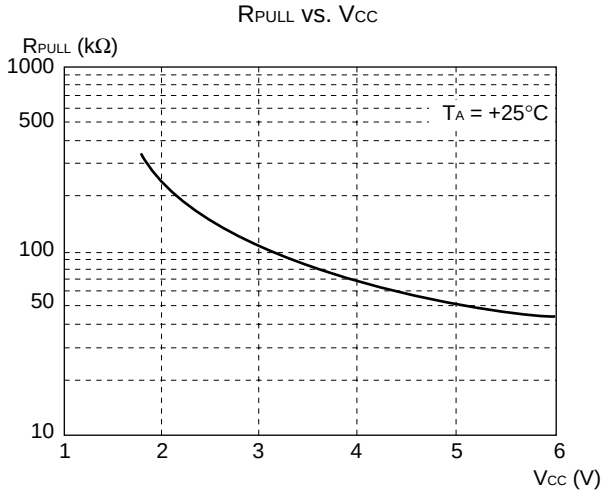
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)





(6) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

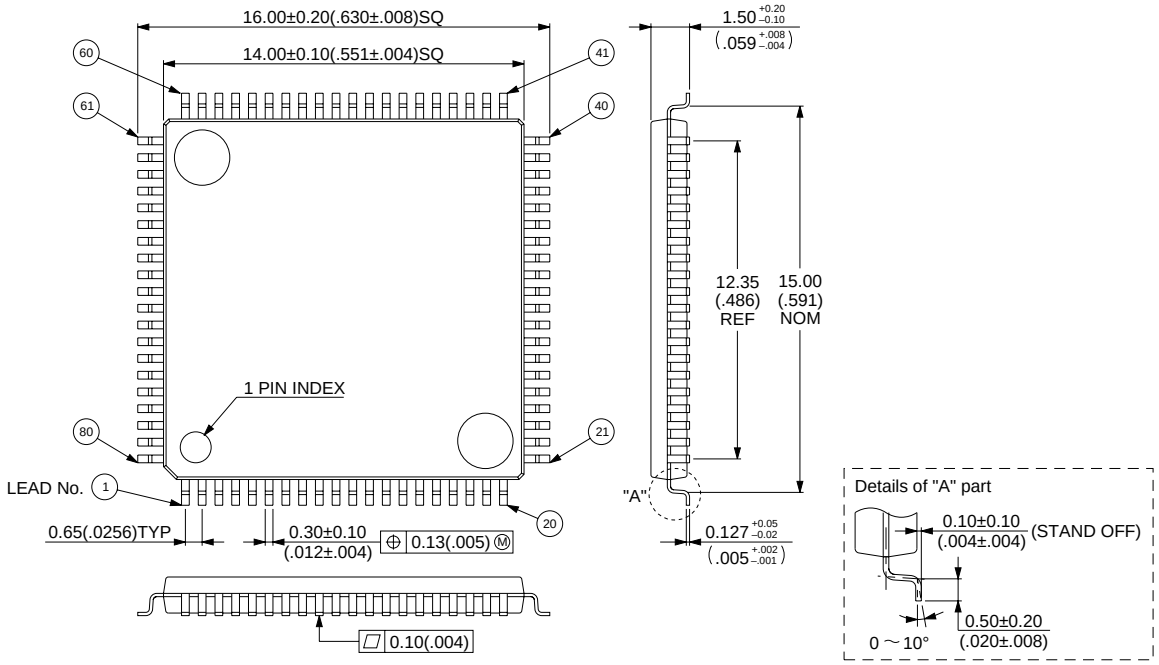
No.	Part number	MB89673 MB89677A	MB89P677A	MB89PV670A
	Specifying procedure	**Specify when ordering masking**	**Set with EPROM programmer**	**Setting not possible**
1	Pull-up resistors P10 to P17, P30 to P37, P40 to P47, P70 to P76	Selectable by pin	Selectable by pin	Fixed to without pull-up resistor
2	Pull-up resistors P00 to P03	Selectable by pin	Selectable in 4-pin unit	
3	Pull-up resistors P04 to P07	Selectable by pin	Selectable in 4-pin unit	
4	Power-on reset With power-on reset Without power-on reset	Selectable	Selectable	Fixed to with power-on reset
5	Oscillation stabilization time selection (at 10 MHz) Approx. $2^{18}/F_C$ (about 26.2 ms) Approx. $2^{17}/F_C$ (about 13.1 ms) Approx. $2^{14}/F_C$ (about 1.6 ms) Approx. $2^4/F_C$ (about 0 ms) F_C: Clock frequency	Selectable	Selectable	Fixed to Approx. $2^{18}/F_C$ (Approx. 26.2 ms)
6	Reset pin output With reset output Without reset output	Selectable	Selectable	Fixed to with reset output

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89673PF MB89677APF MB89P677APF	80-pin Plastic QFP (FPT-80P-M06)	
MB89673PFM MB89677APFM MB89P677APFM	80-pin Plastic QFP (FPT-80P-M11)	
MB89P670ACF	80-pin Ceramic MQFP (MQP-80C-P01)	

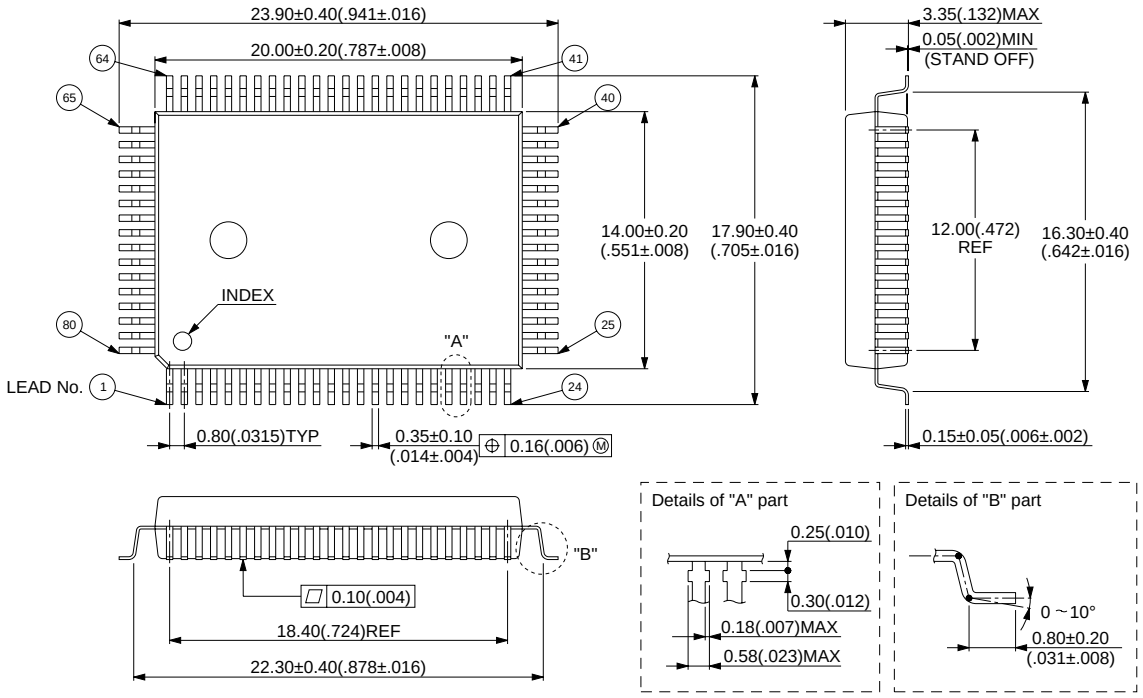
■ PACKAGE DIMENSIONS

80-pin Plastic QFP
(FPT-80P-M11)



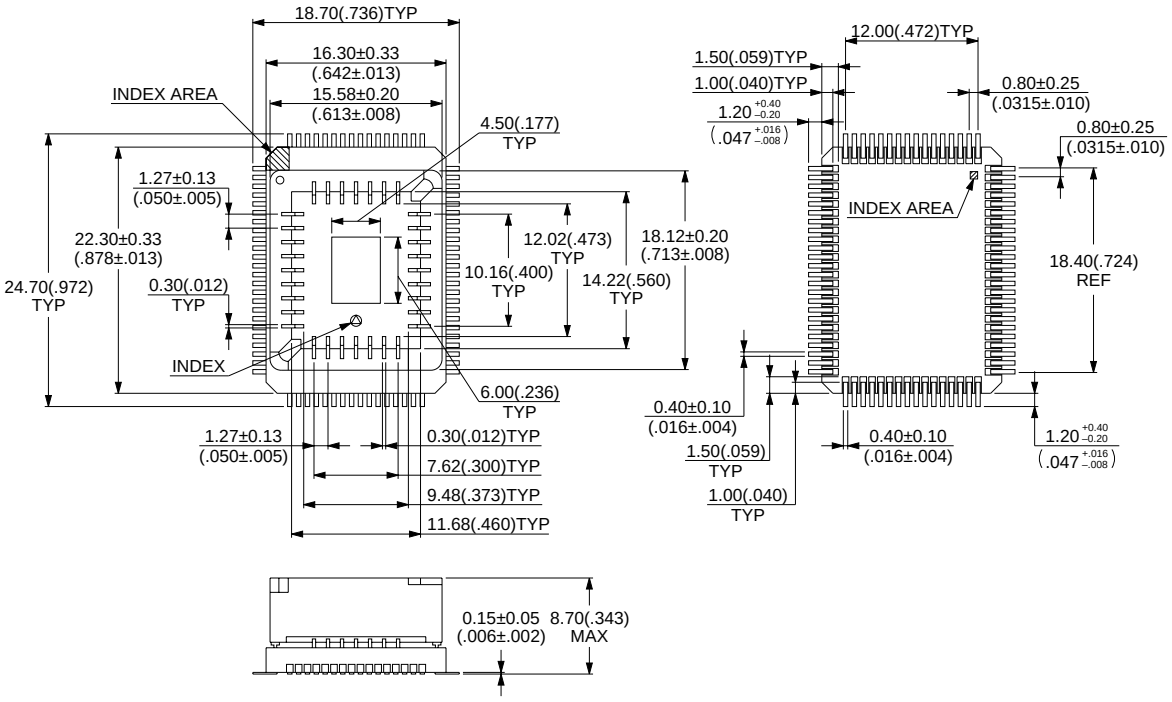
Dimensions in mm (inches)

80-pin Plastic QFP
(FPT-80P-M06)



Dimensions in mm (inches)

80-pin Ceramic MQFP
(MQP-80C-P01)



Dimensions in mm (inches)

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