

December 1997

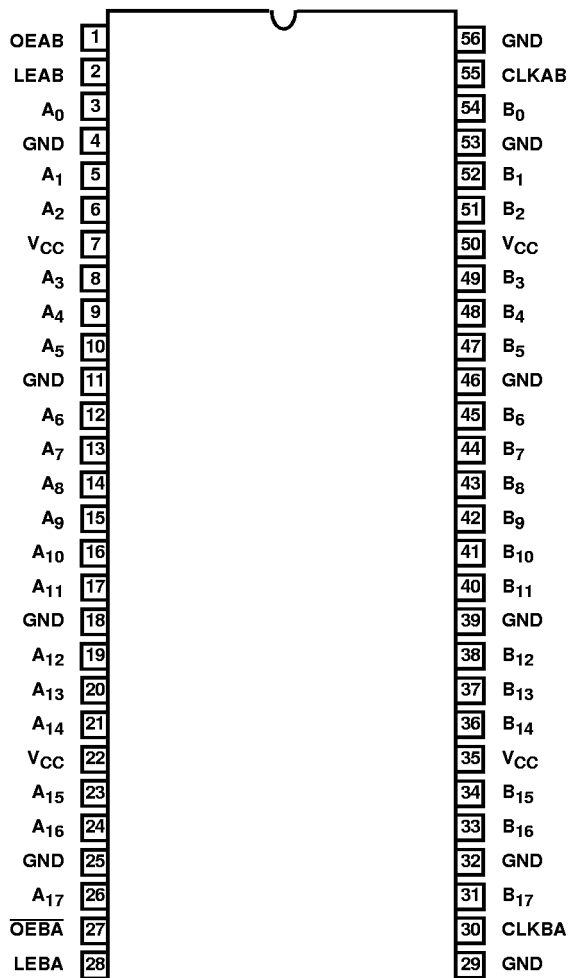
## Fast CMOS 18-Bit Registered Transceiver

### Features

- Advanced 0.6 micron CMOS Technology
- 5V Tolerant Inputs and Outputs
- Supports Live Insertion of PCBs
- 2.0V to 3.6V V<sub>CC</sub> Supply Range
- Balanced 24mA Output Drive
- Low Ground Bounce Outputs
- ESD Protection Exceeds 2000V, HBM; 200V, MM
- Functionally Compatible with FCT3, LVC, LVT, and 74 Series Logic Families

### Pinout

CD74LCX16501  
(SSOP, TSSOP)  
TOP VIEW



### Description

The CD74LCX16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and  $\overline{OEBA}$ ), Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using  $\overline{OEBA}$ , LEBA and CLKBA. This high-speed, low power device offers a flow-through organization for ease of board layout.

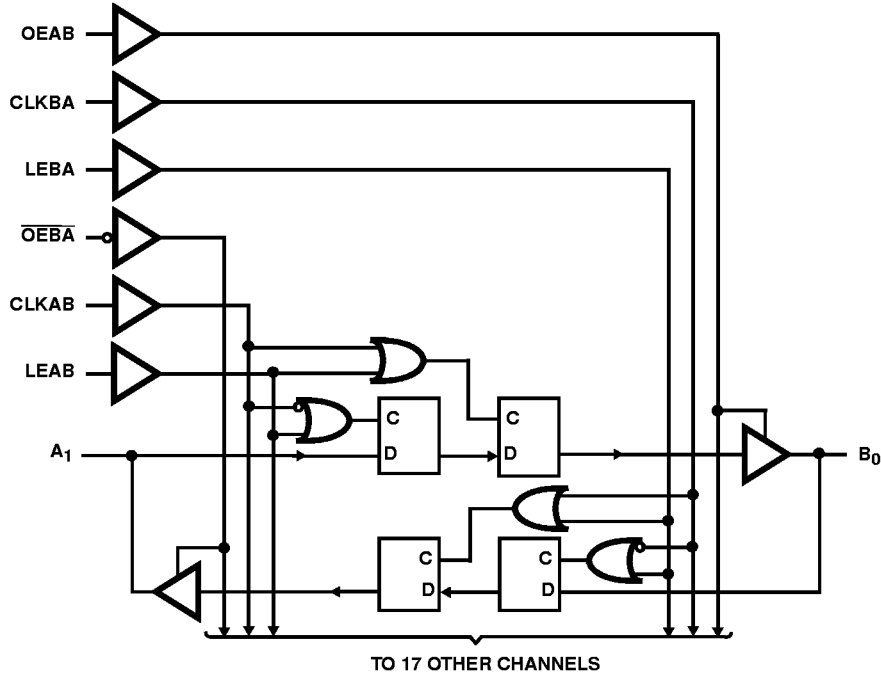
The CD74LCX16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LCX16501MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LCX16501SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

**Functional Block Diagram**



TRUTH TABLE (NOTES 1, 4)

INPUTS				OUTPUTS
OEAB	LEAB	CLKAB	A <sub>X</sub>	B <sub>X</sub>
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B (Note 2)
H	L	H	X	B (Note 3)

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = High Voltage Level; L = Low Voltage Level; Z = High Impedance; ↑ = LOW-to-HIGH Transition

**Pin Descriptions**

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A <sub>X</sub>	A-to-B Data Inputs or B-to-A Three-State Outputs
B <sub>X</sub>	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V <sub>CC</sub>	Power



# CD74LCX16501

## Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS	MIN	(NOTE 7) TYP	MAX	UNITS
<b>CAPACITANCE</b>						
Input Capacitance (Note 9)	C <sub>IN</sub>	V <sub>CC</sub> = Open, V <sub>IN</sub> = 0V or V <sub>CC</sub>	-	7	-	pF
Output Capacitance (Note 9)	C <sub>OUT</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = 0V or V <sub>CC</sub>	-	8	-	pF
Power Dissipation Capacitance (Note 10)	C <sub>PD</sub>	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = 0V or V <sub>CC</sub> , f = 10MHz	-	20	-	pF

## Switching Specifications Over Operating Range

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> = 3.3V ±0.3V		V <sub>CC</sub> = 2.7V		UNITS
			MIN	MAX	MIN	MAX	
Maximum Clock Frequency	f <sub>MAX</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	170	-	-	-	MHz
Propagation Delay, Bus to Bus	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	6.0	1.5	7.0	ns
Propagation Delay, Clock to Bus	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	6.5	1.5	7.5	ns
Propagation Delay, LE to Bus	t <sub>PHL</sub> , t <sub>PLH</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	6.5	1.5	7.5	ns
Output Enable Time	t <sub>PZL</sub> , t <sub>PZH</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	7.5	1.5	8.5	ns
Output Disable Time (Note 13)	t <sub>PLZ</sub> , t <sub>PHZ</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	6.0	1.5	7.0	ns
Setup Time	t <sub>S</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	2.5	-	2.5	-	ns
Hold Time	t <sub>H</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	1.5	-	1.5	-	ns
Pulse Width (Note 13)	t <sub>W</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	3.0	-	3.0	-	ns
Output to Output Skew (Note 14)	t <sub>SK(O)</sub>	C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω	-	1.0	-	-	ns

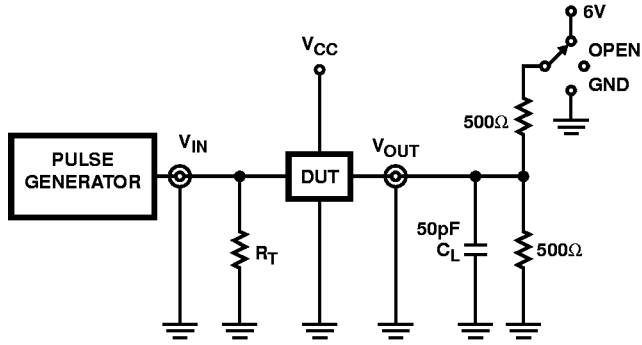
## Dynamic Switching Characteristics T<sub>A</sub> = 25°C

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	TYP	UNITS
Dynamic LOW Peak Voltage	V <sub>OLP</sub>	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V
Dynamic LOW Valley Voltage	V <sub>OLV</sub>	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	0.8	V

### NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V<sub>CC</sub> = 3.3V, 25°C ambient and maximum loading.
8. Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
9. This parameter is determined by device characterization but is not production tested.
10. C<sub>PD</sub> determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:  
P<sub>D</sub> (total power per latch) = V<sub>CC</sub><sup>2</sup> f<sub>i</sub> (C<sub>PD</sub> + C<sub>L</sub>) where f<sub>i</sub> = input frequency, C<sub>L</sub> = output load capacitance, V<sub>CC</sub> = supply range.
11. See test circuit and waveforms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.
14. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
15. Measured with n-1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.

**Test Circuits and Waveforms**



NOTE:

16. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_f, t_r \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}, t_{PZL}, \text{Open Drain}$	6V
$t_{PHZ}, t_{PZH}$	GND
$t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

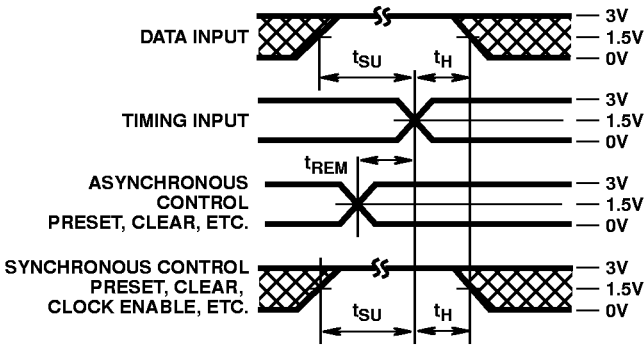


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

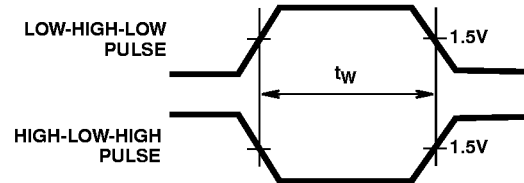


FIGURE 3. PULSE WIDTH

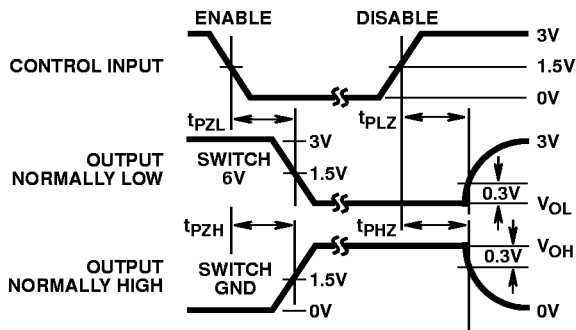


FIGURE 4. ENABLE AND DISABLE TIMING

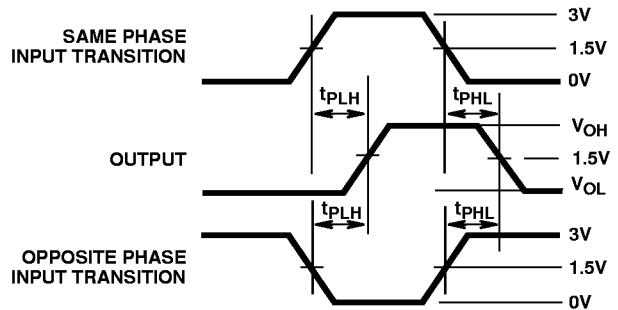
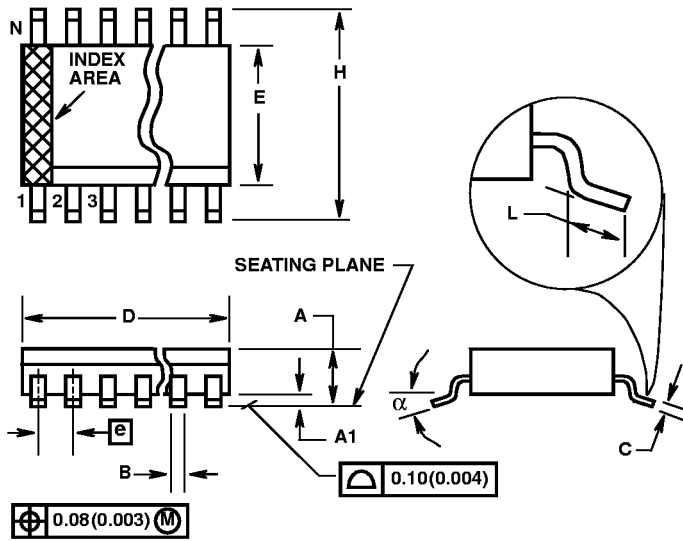


FIGURE 5. PROPAGATION DELAY

**Thin Shrink Small Outline Plastic Packages (TSSOP)**



**M56.240-P**  
56 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

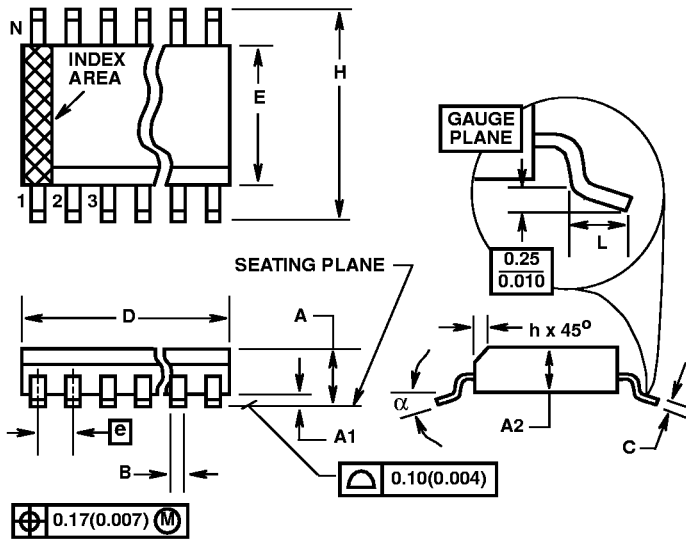
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.547	0.555	13.90	14.09	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	56		56		4
$\alpha$	0°	8°	0°	8°	-

Rev. 0 6/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

**Shrink Small Outline Plastic Packages (SSOP)**



**M56.300-P**  
56 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.720	0.730	18.29	18.54	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	56		56		5
$\alpha$	0°	8°	0°	8°	-

Rev. 0 5/96

**NOTES:**

1. These package dimensions are within allowable dimensions of JECEC MO-118-AB, Issue B.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
3. Dimension "E" does not include interlead flash or protrusions.
4. "L" is the length of terminal for soldering to a substrate.
5. "N" is the number of terminal positions.
6. Terminal numbers are shown for reference only.
7. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.