REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added devices 03 and 04, editorial changes to table I and the appropriate paragraphs throughout the document. Added figures for bond pad locations for device 03.	99-11-10	Ramond Monnin

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Jeff Bowling

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
99-07-01

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 16,000 GATES, MONOLITHIC SILICON

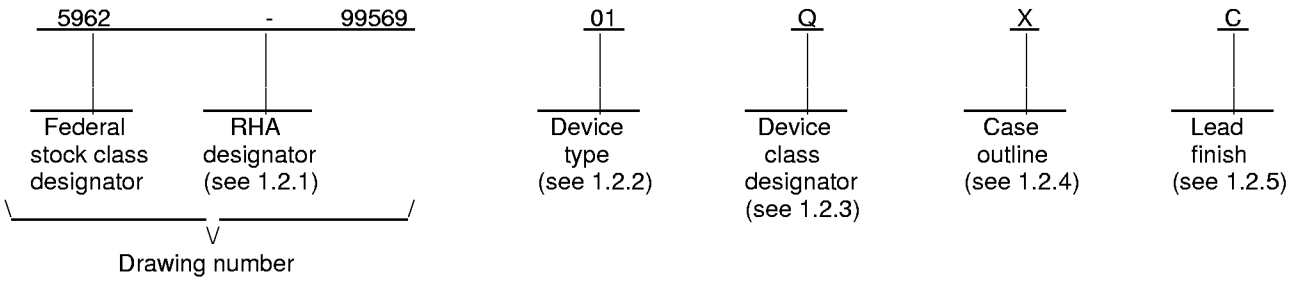
SIZE	CAGE CODE	
A	**67268**	**5962-99569**

SHEET 1 OF 29

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	RT54SX16	16,000 gate field programmable gate array	86 ns
02	RT54SX16-1	16,000 gate field programmable gate array	73 ns
03	A54SX16	16,000 gate field programmable gate array	40 ns
04	A54SX16-1	16,000 gate field programmable gate array	34 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	256	Ceramic Quad Flat Pack
Y	See figure 1	208	Ceramic Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

3.3V DC supply voltage range (V_{CCA}, and V_{CCI})	-0.3 V dc to +4.0 V dc
5.0V DC supply voltage range (V_{CCR})	-0.3 V dc to +6.0 V dc
Input voltage range (V_I)	-0.5 V dc to +5.5 V dc
Output voltage range (V_O)	-0.5 V dc to +3.6 V dc
I/O source sink current (I_{IO})	-30 to +5.0 mA
Storage temperature range (T_{STG})	-40°C to +125°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (Θ_{JC}) :	
Case X	8°C/W 2/
Case Y	9°C/W 2/
Maximum junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

3.3V Power supply	+3.0 V dc to +3.6 V dc (±10% Vcc)
5.0V Power supply	+4.5 V dc to +5.5 V dc (±10% Vcc)
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
3/ 100 percent test coverage of blank programmable logic devices.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Switching test circuit and waveforms . The switching test circuit and waveforms diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device classes M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency less than 1 MHz. Sample size is five devices with no failures on a minimum of ten worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012.

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(2) These eight devices shall also be submitted to the requirements of the specified tests of group A, subgroups 1 and 7. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3a) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3b) If the binning circuit is tested on 100 percent of the products, then the above requirement (3a) is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE I. Electrical performance characteristics.

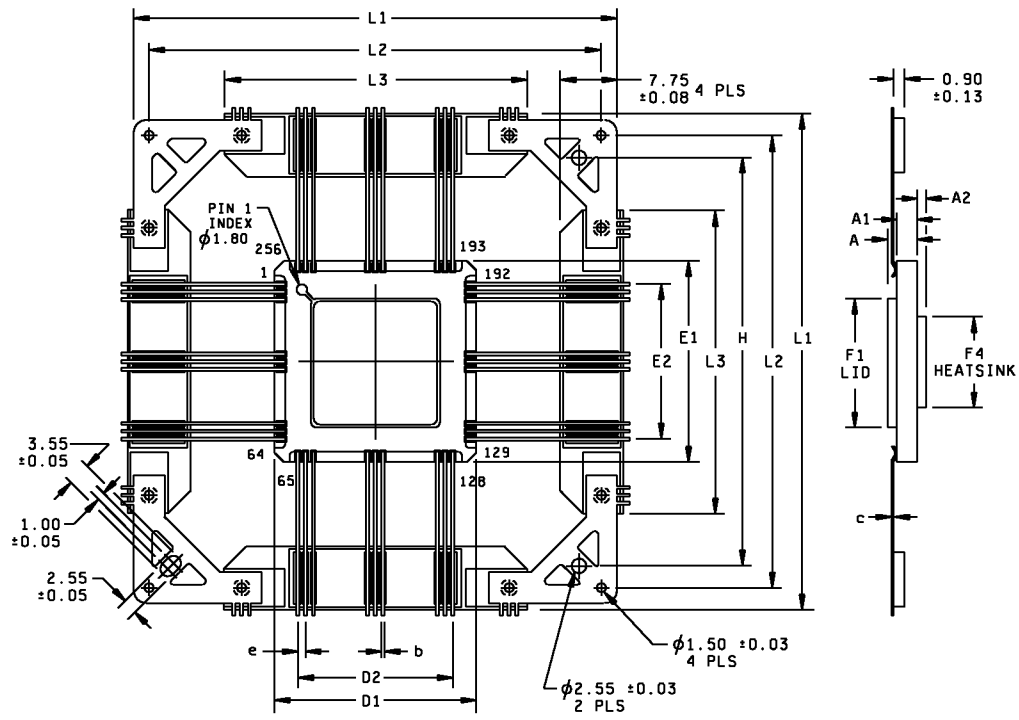
Test	Symbol	Conditions 1/ 4.5 V ≤ V_{CC} ≤ 5.5 V (V_{CCR}) 3.0 V ≤ V_{CC} ≤ 3.6 V (V_{CCI} and V_{CCA}) -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 3.0 V and 4.5 V, I_{OH} = -20 mA (CMOS)	1, 2, 3	All	V_{CC}-0.1	V_{CC}	V
		V_{CC} = 3.0 V and 4.5 V, I_{OH} = -6 mA (TTL)	1, 2, 3	All	2.4	V_{CC}	V
Low level output voltage	V_{OL}	V_{CC} = 3.0 V and 4.5 V, I_{OL} = 8 mA (TTL)	1, 2, 3	All		0.5	V
Low level input voltage	V_{IL}		1, 2, 3	All		0.8	V
High level input voltage	V_{IH}		1, 2, 3	All	2.0		V
Standby supply current	I_{CC}	V_{CC} = 5.5 V and 3.6 V, V_{IN} = V_{CC} or GND	1, 2, 3	All		25	mA
Input leakage current	I_{IL}	V_{CC} = 5.5 V and 3.6 V, V_{IN} = V_{CC} or GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V and 3.6 V, V_O = V_{CC} or GND	1, 2, 3	All	-10	10	µA
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c, f < 1.0 Mhz, V_{OUT} = 0 V	4	All		20	pF
Functional tests	FT 2/	See 4.4.1e	7, 8A, 8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, V_{IL} = 0 V, V_{IH} = 3.0 V, V_{CC} = 4.5 V, V_{OUT} = 1.5 V 3/	9, 10, 11	01		86	ns
				02		73	
				03		40	
				04		34	

1/ All tests shall be performed under the worst case condition unless otherwise specified.

2/ Devices are functionally tested using a serial scan test method. Data is shifted into the TDI pin and the TCK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB, or TDO pins. These tests form a part of the manufacturers's test tape and shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request.

3/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus 16 combinatorial logic modules plus one output buffer. The logic modules are distributed along the left side of the device. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

Case Outline X



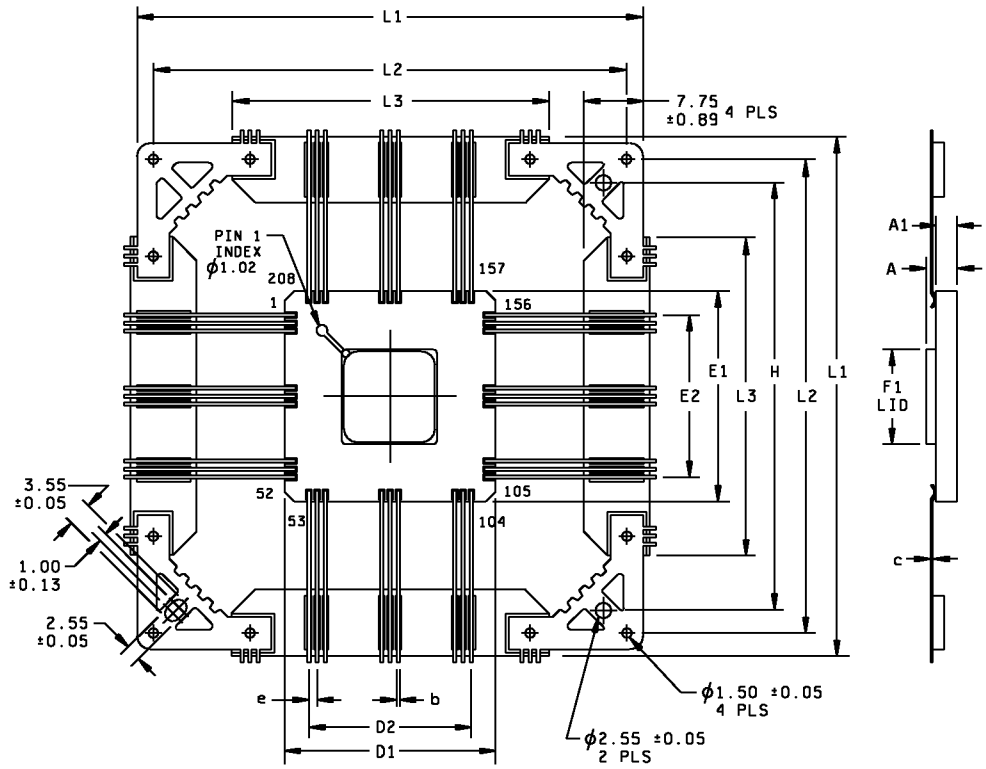
	Dimension (unit : mm)		
Symbol	Min.	Nom.	Max.
A	2.79	3.30	3.81
A1	2.04	2.29	2.54
A2	0.38	0.51	0.64
b	0.18	0.20	0.23
c	0.10	0.15	0.18
D1/E1	35.64	36.00	36.36
D2/E2	31.50 BSC		
e	0.50 BSC		
F1	21.72	21.85	21.98
F4	12.57	12.70	12.83
L1	74.62	75.00	75.38
L2	69.87	70.00	70.13
L3	55.80	56.30	56.80
H	65.77	65.90	66.03
Weight	15 gm (typical)		

NOTES:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 μm) minimum thickness over 80 to 350 microinches (2.0 to 8.9 μm) thickness nickel.
2. Heatsink is connected to GND.
3. Seal ring area is connected to GND.
4. Die attach pad is connected to GND.
5. 15 gm weight is measured after tie-bar removed.
6. Tie-bar dimensions are for reference only.

FIGURE 1. Case outlines.

Case Outline Y



	Dimension (unit : mm)		
Symbol	Min.	Nom.	Max.
A	2.44	2.80	3.16
A1	2.00	2.23	2.46
b	0.18	0.20	0.23
c	0.10	0.15	0.20
D1/E1	28.96	29.21	29.46
D2/E2	25.50 BSC		
e	0.50 BSC		
F1	14.87	15.00	15.13
L1	74.60	75.00	75.40
L2	69.87	70.00	70.13
L3	55.80	56.30	56.80
H	65.77	65.90	66.03
Weight	8.6 gm (typical)		

NOTES:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 μm) minimum thickness over 80 to 350 microinches (2.0 to 8.9 μm) thickness nickel.
2. Seal ring area is connected to GND.
3. Die attach pad is connected to GND.
4. 8.6 gm weight is measured after tie-bar removed.
5. Tie-bar dimensions are for reference only.

FIGURE 1. Case outlines.- Continued.

Case Outline X

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	44	I/O	87	I/O
2	TDI, I/O	45	I/O	88	I/O
3	I/O	46	VCCA	89	I/O
4	I/O	47	I/O	90	PRB, I/O
5	I/O	48	NC	91	GND
6	I/O	49	I/O	92	VCCI
7	I/O	50	I/O	93	GND
8	I/O	51	NC	94	VCCA
9	I/O	52	I/O	95	I/O
10	I/O	53	I/O	96	HCLK
11	TMS	54	NC	97	I/O
12	NC	55	I/O	98	NC
13	NC	56	I/O	99	I/O
14	I/O	57	NC	100	I/O
15	I/O	58	I/O	101	I/O
16	NC	59	GND	102	NC
17	I/O	60	I/O	103	I/O
18	I/O	61	NC	104	I/O
19	I/O	62	I/O	105	I/O
20	NC	63	NC	106	NC
21	I/O	64	I/O	107	I/O
22	I/O	65	I/O	108	I/O
23	I/O	66	I/O	109	I/O
24	I/O	67	I/O	110	GND
25	I/O	68	NC	111	I/O
26	I/O	69	I/O	112	I/O
27	I/O	70	I/O	113	I/O
28	VCCI	71	I/O	114	NC
29	GND	72	I/O	115	I/O
30	VCCA	73	NC	116	I/O
31	GND	74	I/O	117	I/O
32	NC	75	I/O	118	NC
33	I/O	76	I/O	119	I/O
34	1/	77	NC	120	I/O
35	I/O	78	I/O	121	I/O
36	NC	79	I/O	122	NC
37	I/O	80	I/O	123	I/O
38	I/O	81	I/O	124	I/O
39	I/O	82	I/O	125	NC
40	I/O	83	I/O	126	TDO, I/O
41	NC	84	I/O	127	NC
42	I/O	85	I/O	128	GND
43	I/O	86	I/O	129	I/O

FIGURE 2. Terminal connections.

Case Outline X - Continued.

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
130	I/O	173	I/O	216	I/O
131	I/O	174	VCCA	217	I/O
132	I/O	175	GND	218	I/O
133	I/O	176	GND	219	CLKA
134	I/O	177	I/O	220	CLKB
135	I/O	178	NC	221	VCCI
136	I/O	179	I/O	222	GND
137	I/O	180	I/O	223	VCCR
138	NC	181	NC	224	GND
139	NC	182	I/O	225	PRA, I/O
140	NC	183	I/O	226	I/O
141	VCCA	184	NC	227	NC
142	I/O	185	I/O	228	I/O
143	I/O	186	I/O	229	I/O
144	I/O	187	NC	230	I/O
145	I/O	188	I/O	231	I/O
146	I/O	189	GND	232	NC
147	I/O	190	I/O	233	I/O
148	I/O	191	NC	234	I/O
149	I/O	192	NC	235	I/O
150	I/O	193	I/O	236	NC
151	I/O	194	I/O	237	I/O
152	I/O	195	NC	238	I/O
153	I/O	196	I/O	239	NC
154	I/O	197	I/O	240	GND
155	NC	198	I/O	241	I/O
156	NC	199	I/O	242	I/O
157	NC	200	NC	243	NC
158	GND	201	I/O	244	I/O
159	VCCR	202	I/O	245	I/O
160	GND	203	I/O	246	I/O
161	VCCI	204	NC	247	NC
162	I/O	205	I/O	248	I/O
163	I/O	206	I/O	249	I/O
164	I/O	207	I/O	250	NC
165	I/O	208	NC	251	I/O
166	I/O	209	I/O	252	I/O
167	I/O	210	I/O	253	NC
168	I/O	211	I/O	254	I/O
169	I/O	212	I/O	255	I/O
170	I/O	213	I/O	256	TCK, I/O
171	I/O	214	I/O		
172	I/O	215	I/O		

1/ Pin#34 is TRST for device 01 and 02; and is I/O for device 03 and 04.

FIGURE 2. Terminal connections. - Continued.

Case Outline Y

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	36	I/O	71	I/O
2	TDI, I/O	37	I/O	72	I/O
3	I/O	38	I/O	73	I/O
4	I/O	39	I/O	74	I/O
5	I/O	40	VCCI	75	I/O
6	I/O	41	VCCA	76	PRB, I/O
7	I/O	42	I/O	77	GND
8	I/O	43	I/O	78	VCCA
9	I/O	44	I/O	79	GND
10	I/O	45	I/O	80	VCCR
11	TMS	46	I/O	81	I/O
12	VCCI	47	I/O	82	HCLK
13	I/O	48	I/O	83	I/O
14	I/O	49	I/O	84	I/O
15	I/O	50	I/O	85	I/O
16	I/O	51	I/O	86	I/O
17	I/O	52	GND	87	I/O
18	I/O	53	I/O	88	I/O
19	I/O	54	I/O	89	I/O
20	I/O	55	I/O	90	I/O
21	I/O	56	I/O	91	I/O
22	I/O	57	I/O	92	I/O
23	I/O	58	I/O	93	I/O
24	I/O	59	I/O	94	I/O
25	VCCR	60	VCCI	95	I/O
26	GND	61	I/O	96	I/O
27	VCCA	62	I/O	97	I/O
28	GND	63	I/O	98	VCCI
29	I/O	64	I/O	99	I/O
30	1/	65	I/O	100	I/O
31	I/O	66	I/O	101	I/O
32	I/O	67	I/O	102	I/O
33	I/O	68	I/O	103	TDO, I/O
34	I/O	69	I/O	104	I/O
35	I/O	70	I/O	105	GND

1/ Pin #30 is TRST for device 01 and 02; and is I/O for device 03 and 04.

FIGURE 2. Terminal Connections. - Continued.

Case Outline Y - Continued.

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
106	I/O	141	I/O	176	I/O
107	I/O	142	I/O	177	I/O
108	I/O	143	I/O	178	I/O
109	I/O	144	I/O	179	I/O
110	I/O	145	VCCA	180	CLKA
111	I/O	146	GND	181	CLKB
112	I/O	147	I/O	182	VCCR
113	I/O	148	VCCI	183	GND
114	VCCA	149	I/O	184	VCCA
115	VCCI	150	I/O	185	GND
116	I/O	151	I/O	186	PRA, I/O
117	I/O	152	I/O	187	I/O
118	I/O	153	I/O	188	I/O
119	I/O	154	I/O	189	I/O
120	I/O	155	I/O	190	I/O
121	I/O	156	I/O	191	I/O
122	I/O	157	GND	192	I/O
123	I/O	158	I/O	193	I/O
124	I/O	159	I/O	194	I/O
125	I/O	160	I/O	195	I/O
126	I/O	161	I/O	196	I/O
127	I/O	162	I/O	197	I/O
128	I/O	163	I/O	198	I/O
129	GND	164	VCCI	199	I/O
130	VCCA	165	I/O	200	I/O
131	GND	166	I/O	201	VCCI
132	VCCR	167	I/O	202	I/O
133	I/O	168	I/O	203	I/O
134	I/O	169	I/O	204	I/O
135	I/O	170	I/O	205	I/O
136	I/O	171	I/O	206	I/O
137	I/O	172	I/O	207	I/O
138	I/O	173	I/O	208	TCK, I/O
139	I/O	174	I/O		
140	I/O	175	I/O		

FIGURE 2. Terminal Connections. - Continued.

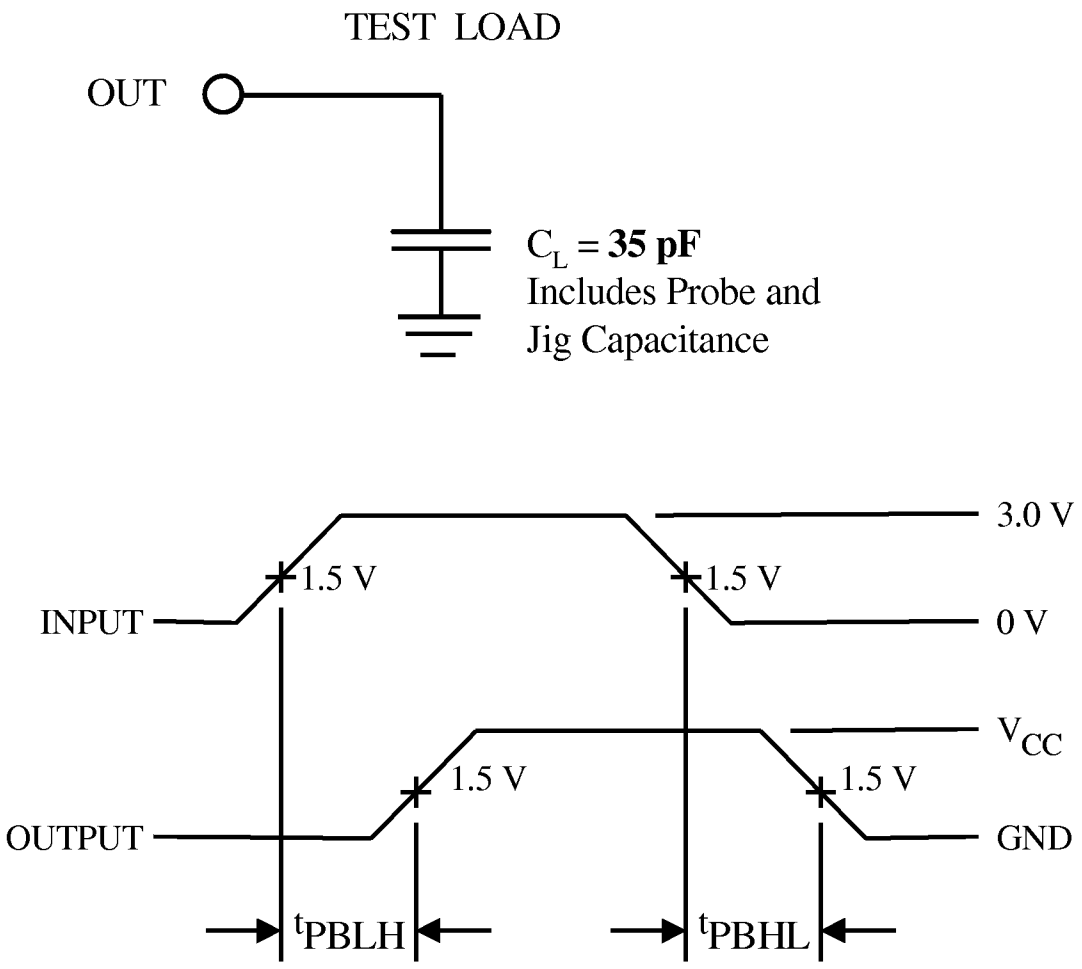


FIGURE 3. Switching test circuit and waveforms.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A,8B,910,11	1*, 2, 3, 7*, 8A,8B, 9, 10, 11	1*, 2, 3, 7*, 8A,8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC}	±1 mA of specified value of table I
I_{OZ}	±2 μA of specified value of table I
t_{PBLH}, t_{PBHL}	±10 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

Appendix A

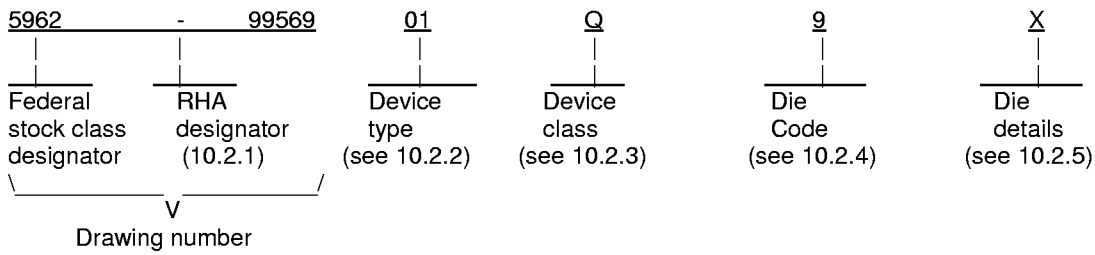
Appendix A forms a part of SMD 5962-99569

10. Scope

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2

PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	RT54SX16	16,000 gate, field programmable gate array	86 ns
03	A54SX16	16,000 gate, field programmable gate array	40 ns

10.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
01	307 mils X 298 mils 1/	16±2 mils	A	A-1
03	201 mils X 195 mils 2/	19±2 mils	B	A-2

1/ Add an additional 8.0 mil (200 micron) for scribeline area on each dimension for device 01.
2/ Add an additional 15.0 mil (380 micron) for scribeline area on each dimension for device 03.

10.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
01	A	A-1
03	B	A-2

10.2.5.3 Interface materials.

Device type	Top metalization	Backside metalization	Die Detail	Figure Number
01	TiN+Al+TiN, 8-10kÅ	None (backgrind)	A	A-1
03	Al/Cu, 6kÅ	None (backgrind)	B	A-2

10.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
01	Nitride	A	A-1
03	Oxide/Nitride	B	A-2

10.2.5.5 Wafer fabrication source.

Device type	Source	Die Detail	Figure Number
01	Matsushita Electronics Corp., Japan	A	A-1
03	Chartered Semiconductor, Singapore	B	A-2

10.3 Absolute maximum ratings.
See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.
See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specification, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

30. REQUIREMENTS.

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be specified in 10.2.5.1 and on figures A-1and A-2.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figures A-1and A-2.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figures A-1and A-2.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figures A-1and A-2.

30.2.5 Truth table(s). Where technically applicable, (for die) the truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

30.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

30.8.1 Unprogrammed die delivered to the user. All testing shall be verified through wafer probe test as defined in 40.2.

30.8.2 Manufacturer-programmed die delivered to the user. The programming integrity test shall be performed during programming. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria within MIL-STD-883 test method 5007.
b) 100% wafer probe (see paragraph 30.4)
c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

40.3.3 Programmability. See 4.4.1.e for packaged die.

40.3.4 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0536.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-HDBK-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

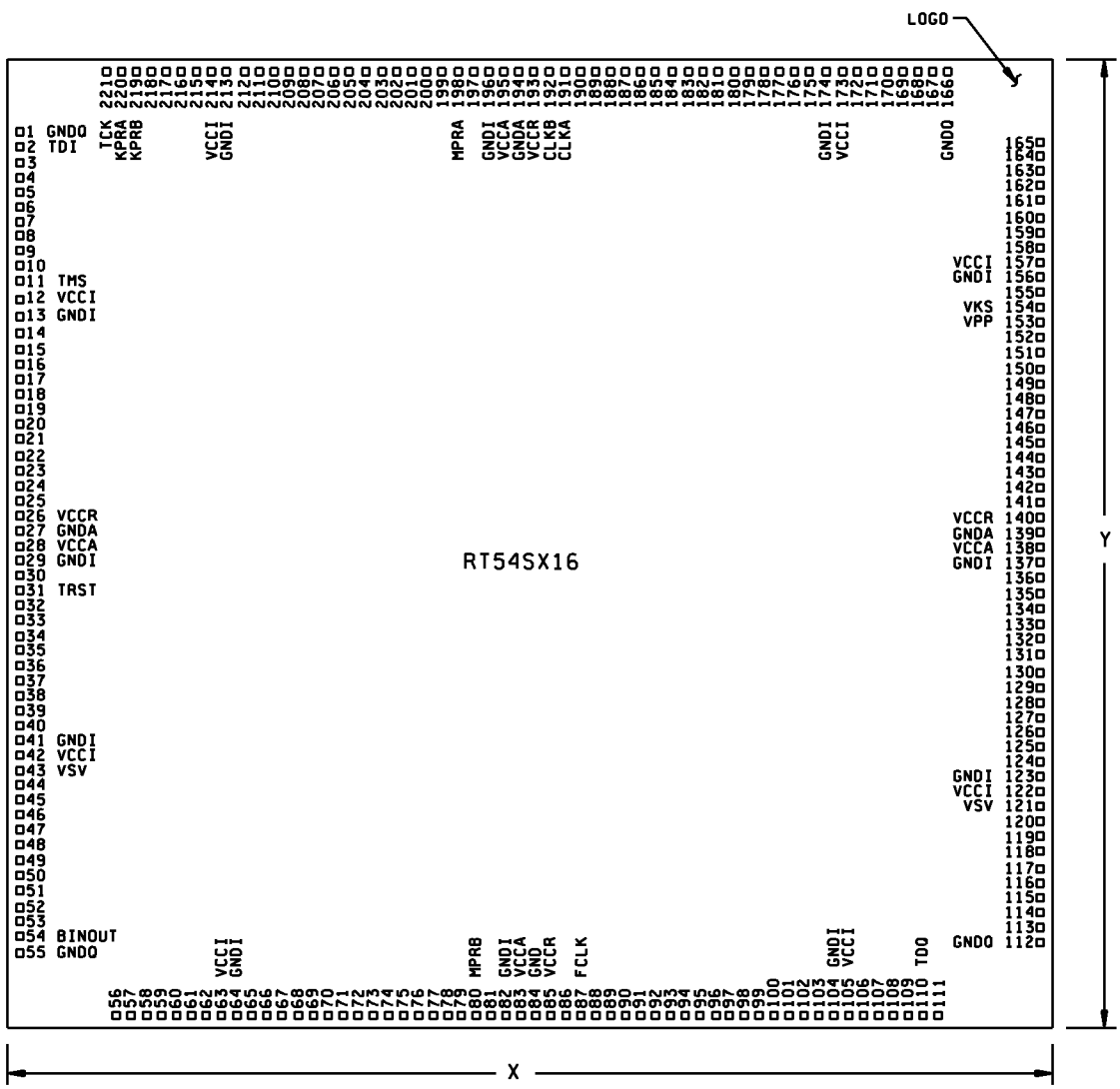


Figure A-1. Bond Pad Locations and Functions for Device 01

Pad#	Name	Center-X	Center-Y	Pad#	Name	Center-X	Center-Y
1	GNDQ	-3833	3351	46	I/O	-3833	-2211
2	TDI	-3833	3206	47	I/O	-3833	-2327
3	I/O	-3833	3074	48	I/O	-3833	-2443
4	I/O	-3833	2947	49	I/O	-3833	-2559
5	I/O	-3833	2831	50	I/O	-3833	-2675
6	I/O	-3833	2715	51	I/O	-3833	-2791
7	I/O	-3833	2599	52	I/O	-3833	-2907
8	I/O	-3833	2483	53	I/O	-3833	-3034
9	I/O	-3833	2367	54	BINGOUT	-3833	-3178
10	I/O	-3833	2251	55	GNDQ	-3833	-3351
11	TMS	-3833	2135	56	I/O	-3373	-3730
12	VCCI	-3833	2008	57	I/O	-3246	-3730
13	GNDI	-3833	1892	58	I/O	-3119	-3730
14	I/O	-3833	1776	59	I/O	-2992	-3730
15	I/O	-3833	1660	60	I/O	-2876	-3730
16	I/O	-3833	1544	61	I/O	-2760	-3730
17	I/O	-3833	1428	62	I/O	-2644	-3730
18	I/O	-3833	1312	63	VCCI	-2528	-3730
19	I/O	-3833	1196	64	GNDI	-2412	-3730
20	I/O	-3833	1080	65	I/O	-2296	-3730
21	I/O	-3833	964	66	I/O	-2180	-3730
22	I/O	-3833	848	67	I/O	-2064	-3730
23	I/O	-3833	732	68	I/O	-1948	-3730
24	I/O	-3833	616	69	I/O	-1832	-3730
25	I/O	-3833	500	70	I/O	-1716	-3730
26	VCCR	-3833	384	71	I/O	-1600	-3730
27	GNDA	-3833	210	72	I/O	-1484	-3730
28	VCCA	-3833	-22	73	I/O	-1368	-3730
29	GNDI	-3833	-196	74	I/O	-1252	-3730
30	I/O	-3833	-312	75	I/O	-1136	-3730
31	TRST	-3833	-428	76	I/O	-1020	-3730
32	I/O	-3833	-544	77	I/O	-904	-3730
33	I/O	-3833	-660	78	I/O	-788	-3730
34	I/O	-3833	-776	79	I/O	-672	-3730
35	I/O	-3833	-892	80	MPRB	-527	-3730
36	I/O	-3833	-1008	81	I/O	-386	-3730
37	I/O	-3833	-1124	82	GNDI	-270	-3730
38	I/O	-3833	-1240	83	VCCA	-96	-3730
39	I/O	-3833	-1356	84	GNDA	137	-3730
40	I/O	-3833	-1472	85	VCCR	311	-3730
41	GNDI	-3833	-1588	86	I/O	427	-3730
42	VCCI	-3833	-1704	87	FCLK	543	-3730
43	VSV	-3833	-1840	88	I/O	659	-3730
44	I/O	-3833	-1979	89	I/O	775	-3730
45	I/O	-3833	-2095	90	I/O	891	-3730

Figure A-1. Bond Pad Locations and Functions for Device 01 - Continued.

Pad#	Name	Center-X	Center-Y	Pad#	Name	Center-X	Center-Y
91	I/O	1007	-3730	136	I/O	3833	-447
92	I/O	1123	-3730	137	GNDI	3833	-331
93	I/O	1239	-3730	138	VCCA	3833	-157
94	I/O	1355	-3730	139	GNDA	3833	76
95	I/O	1471	-3730	140	VCCR	3833	250
96	I/O	1587	-3730	141	I/O	3833	366
97	I/O	1703	-3730	142	I/O	3833	482
98	I/O	1819	-3730	143	I/O	3833	598
99	I/O	1935	-3730	144	I/O	3833	714
100	I/O	2051	-3730	145	I/O	3833	830
101	I/O	2167	-3730	146	I/O	3833	946
102	I/O	2283	-3730	147	I/O	3833	1062
103	I/O	2399	-3730	148	I/O	3833	1178
104	GNDI	2515	-3730	149	I/O	3833	1294
105	VCCI	2631	-3730	150	I/O	3833	1410
106	I/O	2747	-3730	151	I/O	3833	1526
107	I/O	2863	-3730	152	I/O	3833	1642
108	I/O	2979	-3730	153	VPP	3833	1778
109	I/O	3106	-3730	154	VKS	3833	1917
110	TDO	3235	-3730	155	I/O	3833	2033
111	I/O	3373	-3730	156	GNDI	3833	2149
112	GNDQ	3833	-3351	157	VCCI	3833	2265
113	I/O	3833	-3211	158	I/O	3833	2381
114	I/O	3833	-3071	159	I/O	3833	2497
115	I/O	3833	-2926	160	I/O	3833	2613
116	I/O	3833	-2810	161	I/O	3833	2729
117	I/O	3833	-2694	162	I/O	3833	2845
118	I/O	3833	-2578	163	I/O	3833	2990
119	I/O	3833	-2462	164	I/O	3833	3130
120	I/O	3833	-2346	165	I/O	3833	3270
121	VSV	3833	-2210	166	GNDQ	3454	3730
122	VCCI	3833	-2071	167	I/O	3314	3730
123	GNDI	3833	-1955	168	I/O	3174	3730
124	I/O	3833	-1839	169	I/O	3029	3730
125	I/O	3833	-1723	170	I/O	2913	3730
126	I/O	3833	-1607	171	I/O	2797	3730
127	I/O	3833	-1491	172	I/O	2681	3730
128	I/O	3833	-1375	173	VCCI	2565	3730
129	I/O	3833	-1259	174	GNDI	2449	3730
130	I/O	3833	-1143	175	I/O	2333	3730
131	I/O	3833	-1027	176	I/O	2217	3730
132	I/O	3833	-911	177	I/O	2101	3730
133	I/O	3833	-795	178	I/O	1985	3730
134	I/O	3833	-679	179	I/O	1869	3730
135	I/O	3833	-562	180	I/O	1753	3730

Figure A-1. Bond Pad Locations and Functions for Device 01 - Continued.

Pad#	Name	Center-X	Center-Y	Pad#	Name	Center-X	Center-Y
181	I/O	1637	3730	202	I/O	-1085	3730
182	I/O	1521	3730	203	I/O	-1201	3730
183	I/O	1405	3730	204	I/O	-1317	3730
184	I/O	1289	3730	205	I/O	-1433	3730
185	I/O	1173	3730	206	I/O	-1549	3730
186	I/O	1057	3730	207	I/O	-1665	3730
187	I/O	941	3730	208	I/O	-1781	3730
188	I/O	825	3730	209	I/O	-1897	3730
189	I/O	709	3730	210	I/O	-2013	3730
190	I/O	593	3730	211	I/O	-2129	3730
191	CLKA	477	3730	212	I/O	-2245	3730
192	CLKB	361	3730	213	GNDI	-2361	3730
193	VCCR	245	3730	214	VCCI	-2477	3730
194	GNDA	71	3730	215	I/O	-2593	3730
195	VCCA	-161	3730	216	I/O	-2709	3730
196	GNDI	-335	3730	217	I/O	-2825	3730
197	I/O	-451	3730	218	I/O	-2941	3730
198	MPRA	-596	3730	219	KPRB	-3081	3730
199	I/O	-737	3730	220	KPRA	-3221	3730
200	I/O	-853	3730	221	TCK	-3363	3730
201	I/O	-969	3730				

Note:
1. All dimensions are in micrometer
2. The die center is the coordinate origin (0,0).
3. VSV, VKS and Vpp pins are used for programming. For normal operation, these pins should be connected to Vcc or GND.
4. Minimum pad openning (glass free) is 85 micron by 85 micron.

Figure A-1. Bond Pad Locations and Functions for Device 01 - Continued.

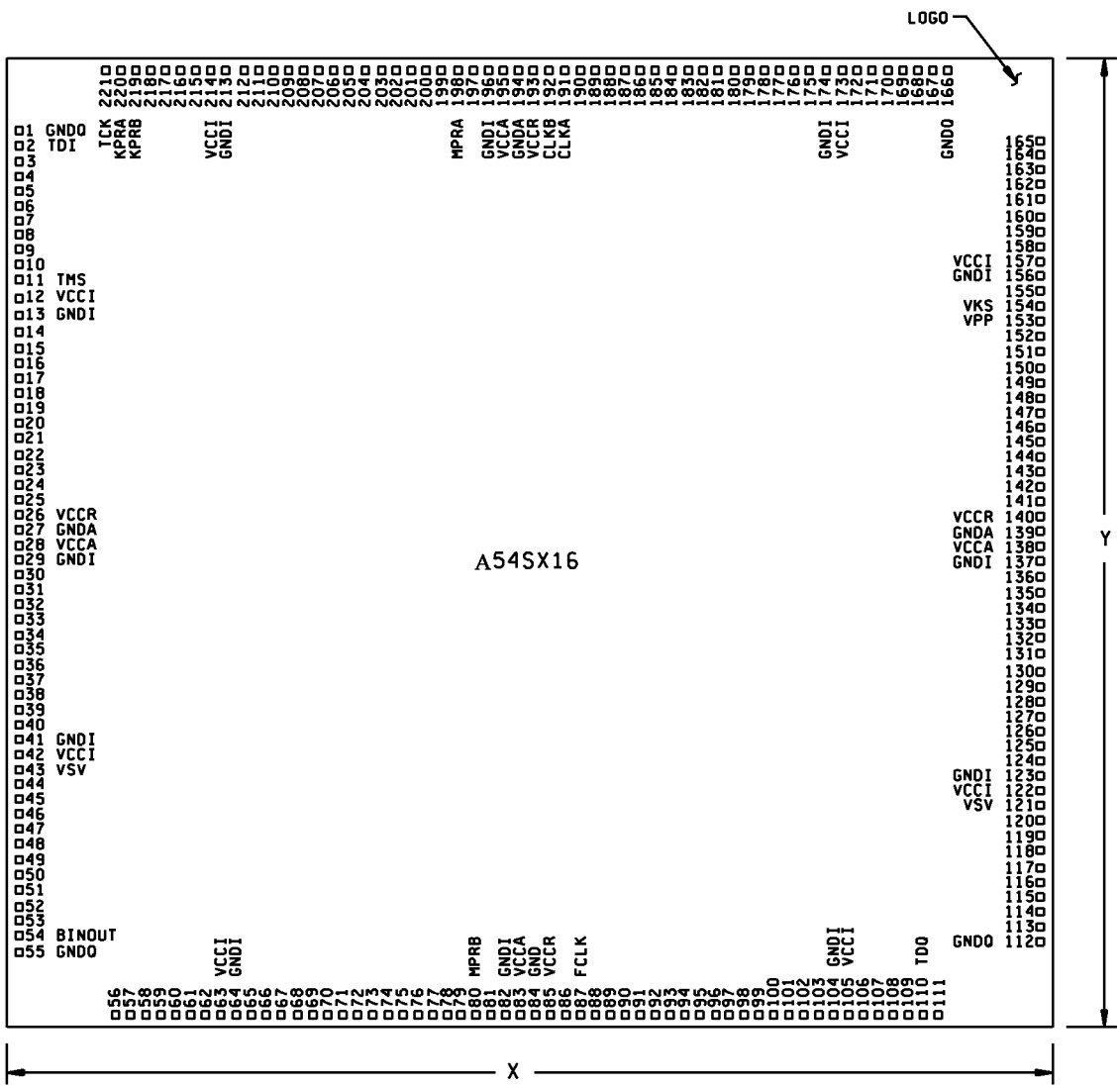


Figure A-2. Bond Pad Locations and Functions for Device 03

Pad#	Name	Center-X	Center-Y		Pad#	Name	Center-X	Center-Y
1	GNDQ	-2491	2178		46	I/O	-2491	-1437
2	TDI	-2491	2084		47	I/O	-2491	-1512
3	I/O	-2491	1998		48	I/O	-2491	-1588
4	I/O	-2491	1916		49	I/O	-2491	-1663
5	I/O	-2491	1840		50	I/O	-2491	-1739
6	I/O	-2491	1765		51	I/O	-2491	-1814
7	I/O	-2491	1689		52	I/O	-2491	-1889
8	I/O	-2491	1614		53	I/O	-2491	-1972
9	I/O	-2491	1539		54	BINGOUT	-2491	-2066
10	I/O	-2491	1463		55	GNDQ	-2491	-2178
11	TMS	-2491	1388		56	I/O	-2192	-2425
12	VCCI	-2491	1305		57	I/O	-2110	-2425
13	GNDI	-2491	1230		58	I/O	-2027	-2425
14	I/O	-2491	1155		59	I/O	-1944	-2425
15	I/O	-2491	1079		60	I/O	-1869	-2425
16	I/O	-2491	1004		61	I/O	-1794	-2425
17	I/O	-2491	928		62	I/O	-1718	-2425
18	I/O	-2491	853		63	VCCI	-1643	-2425
19	I/O	-2491	778		64	GNDI	-1567	-2425
20	I/O	-2491	702		65	I/O	-1492	-2425
21	I/O	-2491	627		66	I/O	-1417	-2425
22	I/O	-2491	551		67	I/O	-1341	-2425
23	I/O	-2491	476		68	I/O	-1266	-2425
24	I/O	-2491	401		69	I/O	-1190	-2425
25	I/O	-2491	325		70	I/O	-1115	-2425
26	VCCR	-2491	250		71	I/O	-1040	-2425
27	GNDA	-2491	137		72	I/O	-964	-2425
28	VCCA	-2491	-14		73	I/O	-889	-2425
29	GNDI	-2491	-127		74	I/O	-813	-2425
30	I/O	-2491	-203		75	I/O	-738	-2425
31	I/O	-2491	-278		76	I/O	-663	-2425
32	I/O	-2491	-353		77	I/O	-587	-2425
33	I/O	-2491	-429		78	I/O	-512	-2425
34	I/O	-2491	-504		79	I/O	-436	-2425
35	I/O	-2491	-580		80	MPRB	-342	-2425
36	I/O	-2491	-655		81	I/O	-251	-2425
37	I/O	-2491	-730		82	GNDI	-175	-2425
38	I/O	-2491	-806		83	VCCA	-62	-2425
39	I/O	-2491	-881		84	GNDA	89	-2425
40	I/O	-2491	-957		85	VCCR	202	-2425
41	GNDI	-2491	-1032		86	I/O	277	-2425
42	VCCI	-2491	-1107		87	FCLK	353	-2425
43	VSV	-2491	-1196		88	I/O	428	-2425
44	I/O	-2491	-1286		89	I/O	503	-2425
45	I/O	-2491	-1362		90	I/O	579	-2425

Figure A-2. Bond Pad Locations and Functions for Device 03 - Continued.

Pad#	Name	Center-X	Center-Y	Pad#	Name	Center-X	Center-Y
91	I/O	654	-2425	136	I/O	2491	-290
92	I/O	730	-2425	137	GNDI	2491	-215
93	I/O	805	-2425	138	VCCA	2491	-102
94	I/O	880	-2425	139	GNDA	2491	49
95	I/O	956	-2425	140	VCCR	2491	162
96	I/O	1031	-2425	141	I/O	2491	238
97	I/O	1107	-2425	142	I/O	2491	313
98	I/O	1182	-2425	143	I/O	2491	388
99	I/O	1257	-2425	144	I/O	2491	464
100	I/O	1333	-2425	145	I/O	2491	539
101	I/O	1408	-2425	146	I/O	2491	615
102	I/O	1484	-2425	147	I/O	2491	690
103	I/O	1559	-2425	148	I/O	2491	765
104	GNDI	1634	-2425	149	I/O	2491	841
105	VCCI	1710	-2425	150	I/O	2491	916
106	I/O	1785	-2425	151	I/O	2491	992
107	I/O	1861	-2425	152	I/O	2491	1067
108	I/O	1936	-2425	153	VPP	2491	1156
109	I/O	2019	-2425	154	VKS	2491	1246
110	TDO	2103	-2425	155	I/O	2491	1321
111	I/O	2192	-2425	156	GNDI	2491	1397
112	GNDQ	2491	-2178	157	VCCI	2491	1472
113	I/O	2491	-2087	158	I/O	2491	1547
114	I/O	2491	-1996	159	I/O	2491	1623
115	I/O	2491	-1902	160	I/O	2491	1698
116	I/O	2491	-1826	161	I/O	2491	1774
117	I/O	2491	-1751	162	I/O	2491	1849
118	I/O	2491	-1676	163	I/O	2491	1944
119	I/O	2491	-1600	164	I/O	2491	2035
120	I/O	2491	-1525	165	I/O	2491	2126
121	VSV	2491	-1436	166	GNDQ	2245	2425
122	VCCI	2491	-1346	167	I/O	2154	2425
123	GNDI	2491	-1270	168	I/O	2063	2425
124	I/O	2491	-1195	169	I/O	1969	2425
125	I/O	2491	-1120	170	I/O	1893	2425
126	I/O	2491	-1044	171	I/O	1818	2425
127	I/O	2491	-969	172	I/O	1742	2425
128	I/O	2491	-893	173	VCCI	1667	2425
129	I/O	2491	-818	174	GNDI	1592	2425
130	I/O	2491	-743	175	I/O	1516	2425
131	I/O	2491	-667	176	I/O	1441	2425
132	I/O	2491	-592	177	I/O	1365	2425
133	I/O	2491	-516	178	I/O	1290	2425
134	I/O	2491	-441	179	I/O	1215	2425
135	I/O	2491	-366	180	I/O	1139	2425

Figure A-2. Bond Pad Locations and Functions for Device 03 - Continued.

Pad#	Name	Center-X	Center-Y	Pad#	Name	Center-X	Center-Y
181	I/O	1064	2425	202	I/O	-706	2425
182	I/O	988	2425	203	I/O	-781	2425
183	I/O	913	2425	204	I/O	-856	2425
184	I/O	838	2425	205	I/O	-932	2425
185	I/O	762	2425	206	I/O	-1007	2425
186	I/O	687	2425	207	I/O	-1083	2425
187	I/O	611	2425	208	I/O	-1158	2425
188	I/O	536	2425	209	I/O	-1233	2425
189	I/O	461	2425	210	I/O	-1309	2425
190	I/O	385	2425	211	I/O	-1384	2425
191	CLKA	310	2425	212	I/O	-1459	2425
192	CLKB	234	2425	213	GNDI	-1535	2425
193	VCCR	159	2425	214	VCCI	-1610	2425
194	GNDA	46	2425	215	I/O	-1686	2425
195	VCCA	-105	2425	216	I/O	-1761	2425
196	GNDI	-218	2425	217	I/O	-1836	2425
197	I/O	-293	2425	218	I/O	-1912	2425
198	MPRA	-387	2425	219	KPRB	-2003	2425
199	I/O	-479	2425	220	KPRA	-2094	2425
200	I/O	-555	2425	221	TCK	-2186	2425
201	I/O	-630	2425				

Note:
1. All dimensions are in micrometer
2. The die center is the coordinate origin (0,0).
3. VSV, VKS and Vpp pins are used for programming. For normal operation, these pins should be connected to Vcc or GND.
4. Minimum pad openning (glass free) is 85 micron by 85 micron.

Figure A-2. Bond Pad Locations and Functions for Device 03 - Continued.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-11-10

Approved sources of supply for SMD 5962-99569 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar 2/ PIN
5962-9956901QXC	0J4Z0	RT54SX16-CQ256B
5962-9956901QYC	0J4Z0	RT54SX16-CQ208B
5962-9956902QXC	0J4Z0	RT54SX16-1CQ256B
5962-9956902QYC	0J4Z0	RT54SX16-1CQ208B
5962-9956901Q9A	0J4Z0	RT54SX16-DIE
5962-9956903QXC	0J4Z0	A54SX16-CQ256B
5962-9956903QYC	0J4Z0	A54SX16-CQ208B
5962-9956904QXC	0J4Z0	A54SX16-1CQ256B
5962-9956904QYC	0J4Z0	A54SX16-1CQ208B
5962-9956903Q9B	0J4Z0	A54SX16-DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086