3.3V/5V 2.5GHz PECL/ECL 1:4 FANOUT BUFFER WITH 2:1 INPUT MUX

FEATURES

- **High-speed 1:4 PECL/ECL fanout buffer**
- **2:1 multiplexer input**
- **Guaranteed AC parameters over temp/voltage:**
  - **> 2.5GHz f_{MAX} (toggle)**
  - **< 225ps rise/fall times**
  - **< 25ps within device skew**
  - **< 425ps propagation delay (CLK-to-Q)**
- **Low jitter design:**
  - **< 1ps (rms) cycle-to-cycle jitter**
  - **< 1ps (pk-pk) total jitter**
- **Flexible power supply: 3.3V/5V**
- **Wide operating temperature range: –40°C to +85°C**
- **V_{BB} reference for AC-coupled or single-ended applications**
- **Output enable/disable function**
- **100K PECL/ECL compatible logic**
- **Input accepts PECL/LVPECL/ECL/HSTL logic levels**
- **Available in a 16-Pin TSSOP package**

DESCRIPTION

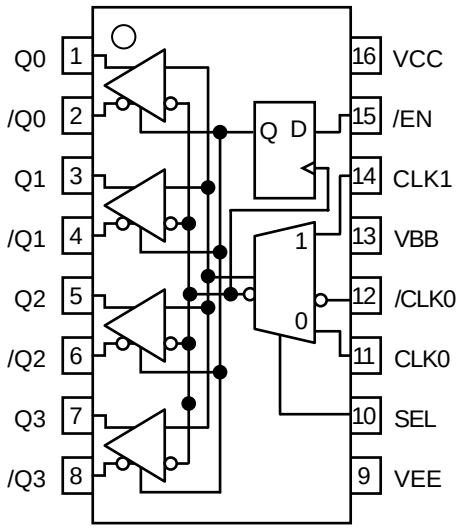
The SY100EP15V is a high-speed, low-skew, PECL/ECL 1:4 precision fanout buffer with a 2:1 mux front end in a small 16-pin TSSOP package. The 2:1 mux input accepts a single-ended PECL/ECL source (CLK1) and a differential PECL/ECL/HSTL source (CLK0). All I/O pins are 100K EP PECL/ECL logic compatible.

AC performance is guaranteed over the industrial –40°C to +85°C temperature range and 3.3V to 5V supply voltage. This device will operate in PECL/LVPECL or ECL/LVECL mode. For clock applications, the high-speed design combined with an extremely fast rise/fall time of less than 225ps produces a toggle frequency as high as 2.5GHz (~400mV_{PP} swing).

A V_{BB} output reference pin is available for AC–coupled and single-ended input applications. In addition, a synchronous output enable function is provided.

The SY100EP15V is part of Micrel's high-speed, precision edge timing and distribution family. For applications that require a different I/O combination, consult Micrel's website at *www.micrel.com*, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock dividers.

PIN CONFIGURATION/BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Pin Number	Function
1, 2, 3, 4 5, 6, 7, 8	Q0 – Q3 /Q0 – /Q3	Outputs 0 through 3: 100KEP (LV)PECL/(LV)ECL compatible differential outputs. Terminate with 50Ω to V_{CC}–2V. Unused output pairs may be left floating, or pulled-down with a 2kΩ resistor to the most negative supply. Unused single-ended outputs must have a balanced load. For AC-coupled applications, the output stage emitter follower must have a DC current path to ground. See "Termination" section.
9	VEE	Negative Power Supply: For PECL/LVPECL applications, connect to GND.
10	SEL	100KEP (LV)PECL/(LV)ECL Compatible 2:1 Mux Input Select Control. See "Truth Table." The select (SEL) pin includes an internal 75kΩ pull-down resistor. Default condition when left floating is LOW, and CLK0 input is selected.
11, 12	CLK0, /CLK0	Differential (LV)PECL/(LV)ECL/HSTL Compatible Input: The inputs include an internal 75kΩ pull-down resistor on CLK0 and internal 75kΩ pull-up and pull-down on /CLK0. Default condition for CLK0 is LOW when left floating and V_{CC}/2 for /CLK0 when left floating.
13	VBB	Reference Output Voltage: This reference is typically used to bias the unused inverting input for single-ended input applications, or as the termination point for AC-coupled differential input applications. V_{BB} reference value is approximately V_{CC}–1.3V, and tracks Vcc 1:1. Maximum sink/source capability for V_{BB} is 0.50mA. For single ended inputs, connect to the unused input through a 50Ω resistor. Decouple the V_{BB} pin with a 0.01µF capacitor to V_{CC}.
14	CLK1	Single-Ended (LV)PECL/(LV)ECL Compatible Input: This pin includes an internal 75kΩ pull-down resistor. Default condition is LOW when left floating.
15	/EN	100KEP (LV)PECL/(LV)ECL Compatible Input: This synchronous pin controls the output state. See "Truth Table." To ensure proper synchronous operation, adhere to the Set-up and Hold times, as described in the AC electrical table. When /EN pin goes HIGH, Q outputs go LOW, and /Q outputs go HIGH on the next falling clock transition. This synchronous operation avoids any chance of generating a runt pulse.
16	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.

TRUTH TABLE(1)

CLK0	CLK1	SEL	/EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
↓	X	L	H	L
X	↓	H	H	L

NOTE:

1. ↓ = Negative edge.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
$V_{CC} - V_{EE}$	Power Supply Voltage		6.0	V
V_{IN}	Input Voltage (V_{CC} = 0V, V_{IN} not more negative than V_{EE}) Input Voltage (V_{EE} = 0V, V_{IN} not more positive than V_{CC})		–6.0 to 0 +6.0 to 0	V
I_{OUT}	Output Current	–Continuous –Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current[2]		±0.5	mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STORE}	Storage Temperature Range		–65 to +150	°C
θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)	–Still-Air (single-layer PCB) –Still-Air (multi-layer PCB) –500lfpm (multi-layer PCB)	115 75 65	°C/W
θ_{JC}	Package Thermal Resistance (Junction-to-Case)		21	°C/W

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Due to the limited drive capability, use for inputs of same package only.

DC ELECTRICAL CHARACTERISTICS[1]

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Power Supply Voltage										V	
	(PECL)	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5		
	(LVPECL)	2.97	3.3	3.63	2.97	3.3	3.63	2.97	3.3	3.63		
	(ECL)	–5.5	–5.0	–4.5	–5.5	–5.0	–4.5	–5.5	–5.0	–4.5		
	(LVECL)	–3.63	–3.3	–2.97	–3.63	–3.3	–2.97	–3.63	–3.3	–2.97		
I_{CC}	Power Supply Current	—	—	70	—	52	72	—	—	75	mA	
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	$V_{IN} = V_{IH}$
I_{IL}	Input LOW Current											
	CLK0, CLK1	0.5	—	—	0.5	—	—	0.5	—	—	µA	$V_{IN} = V_{IL}$
	/CLK0	–150	—	—	–150	—	—	–150	—	—	µA	$V_{IN} = V_{IL}$
C_{IN}	Input Capacitance (TSSOP)	—	—	—	—	1.0	—	—	—	—	pF	

NOTE:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.0V ±10%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	1355	—	1675	1355	—	1675	1355	—	1675	mV	V_{CC} = 3.3V
V_{IH}	Input HIGH Voltage (Single-Ended)	2075	—	2420	2075	—	2420	2075	—	2420	mV	V_{CC} = 3.3V
V_{OL}	Output LOW Voltage	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV	V_{CC} = 3.3V
V_{OH}	Output HIGH Voltage	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV	V_{CC} = 3.3V
V_{BB}	Reference Voltage[2]	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV	V_{CC} = 3.3V
V_{IHCMR}	Input HIGH Voltage Common Mode Range[3]	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters varies 1:1 with V_{CC}. Output load is 50Ω to V_{CC}–2V.
2. V_{BB} varies 1:1 with V_{CC}.
3. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100KEP) PECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 5.0V ±10%, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-Ended)	3055	—	3375	3055	—	3375	3055	—	3375	mV	V_{CC} = 5V
V_{IH}	Input HIGH Voltage (Single-Ended)	3775	—	4120	3775	—	4120	3775	—	4120	mV	V_{CC} = 5V
V_{OL}	Output LOW Voltage	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV	V_{CC} = 5V
V_{OH}	Output HIGH Voltage	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV	V_{CC} = 5V
V_{BB}	Output Voltage Reference[2]	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV	V_{CC} = 5V
V_{IHCMR}	Input HIGH Voltage[3] Common Mode Range	1.2	—	V_{CC}	1.2	—	V_{CC}	1.2	—	V_{CC}	V	

NOTES:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained. Input and output parameters vary 1:1 with V_{CC}. Output load is 50Ω to V_{CC} –2V.
2. V_{BB} varies 1:1 with V_{CC}.
3. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100KEP) LVECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V, V_{EE} = –2.97V to –3.63V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage (Single-ended)	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV	
V_{IH}	Input HIGH Voltage (Single-ended)	–1165	—	–880	–1165	—	–880	–1165	—	–880	mV	
V_{OL}	Output LOW Voltage	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV	50Ω to V_{CC}–2V
V_{BB}	Output Reference Voltage	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV	
V_{IHCMR}	Input HIGH Voltage Common Mode Range[2]	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V	

NOTES:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100K) ECL DC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 0V, V_{EE} = –4.5V to –5.5V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{IL}	Input LOW Voltage	–1945	—	–1625	–1945	—	–1625	–1945	—	–1625	mV	
V_{IH}	Input HIGH Voltage	–1225	—	–880	–1225	—	–880	–1225	—	–880	mV	
V_{OL}	Output LOW Voltage	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV	50Ω to V_{CC}–2V
V_{OH}	Output HIGH Voltage	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV	50Ω to V_{CC}–2V
V_{BB}	Output Reference Voltage	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV	
V_{IHCMR}	Input HIGH Voltage Common Mode Range[2]	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V_{EE} +1.2	—	0.0	V	

NOTES:

1. 100KEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. The V_{IHCMR} is referenced to the most positive side of the differential input signal.

HSTL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.97V to 3.63V, V_{EE} = 0V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	1200	—	—	1200	—	—	1200	—	—	mV
V_{IL}	Input LOW Voltage	—	—	400	—	—	400	—	—	400	mV

AC ELECTRICAL CHARACTERISTICS

LVPECL: V_{CC} = 2.97V to 3.63V, V_{EE} = 0V; PECL: V_{CC} = 4.5V to 5.5V, V_{EE} = 0V
ECL: V_{CC} = 0V, V_{EE} = –4.5V to –5.5V; LVECL: V_{CC} = 0V, V_{EE} = –2.97V to –3.63V

Symbol	Parameter	T_A = –40°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}[1]	Maximum Frequency	2.5	—	—	2.5	—	—	2.5	—	—	GHz
t_{PD}	PropagationDelay to Output PECL/ECL										
	Diff. IN-to-Q	275	—	425	275	375	425	275	—	425	ps
	IN (Single-Ended)-to-Q	250	—	450	250	400	450	250	—	450	ps
	SEL-to-Q	250	—	450	250	400	450	250	—	450	ps
	LVPECL/LVECL										
	Diff. IN-to-Q	275	—	425	275	375	425	275	—	425	ps
	IN (Single-Ended)-to-Q	250	—	450	250	400	450	250	—	450	ps
	SEL-to-Q	250	—	450	250	400	450	250	—	450	ps
t_{SKEW}[2]	Within-Device Skew (Diff.)	—	—	25	—	15	25	—	—	25	ps
	Part-to-Part Skew (Diff.)	—	—	150	—	100	150	—	—	150	ps
t_S[3]	Set-Up Time /EN to CLK	100	0	—	100	0	—	100	0	—	ps
t_H[3]	Hold Time /EN to CLK	200	50	—	200	50	—	200	50	—	ps
t_{JITTER}	Cycle-to-Cycle Jitter[4]	—	0.2	1	—	0.2	1	—	0.2	1	ps(rms)
	Total Jitter (622MHz clock)[5]	—	<1	—	—	<1	—	—	<1	—	ps(pk-pk)
V_{ID}	Input Voltage Range	150	800	1200	150	800	1200	150	800	1200	mV
t_r, t_f	Output Rise/Fall Times (20% to 80%)	75	—	225	75	130	225	85	—	225	ps

NOTES:

1. f_{MAX} is defined as the maximum toggle frequency. Measured with 750mV input signal, 50% duty cycle, output swing ≥ 400mV(diff), all loading with 50Ω to V_{CC}–2V.
2. Skew is measured between outputs under identical transitions.
3. Set-up and hold times apply to synchronous applications that intend to enable/disable before then ext clock cycle. For asynchronous applications, set-up and hold time does not apply.
4. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n – T_{n+1}$ where T is the time between rising edges of the output signal.
5. Total jitter definition: with an ideal clock input, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Package Marking
SY100EP15VK4I	K4-16-1	Industrial	XEP15V
SY100EP15VK4ITR*	K4-16-1	Industrial	XEP15V

*Tape and Reel

TERMINATION RECOMMENDATIONS

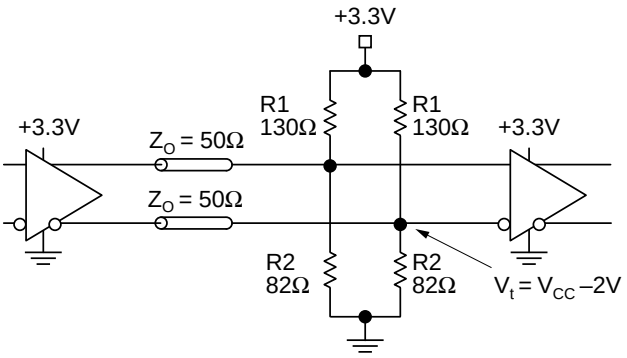


Figure 1. Parallel Termination–Thevenin Equivalent

NOTES:

1. For +2.5V systems:
   R1 = 250Ω
   R2 = 62.5Ω
2. For +5.0V systems:
   R1 = 82Ω
   R2 = 130Ω

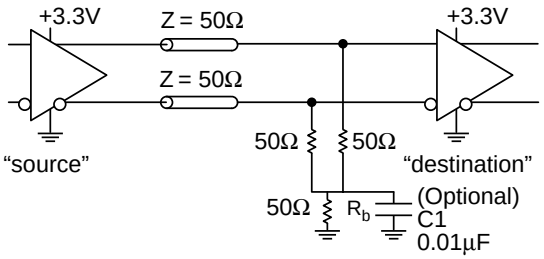


Figure 2. Three-Resistor "Y–Termination"

NOTES:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +5V systems, R_b = 110Ω.
4. C1 is an optional bypass capacitor intended to compensate for any tr/tf mismatches.

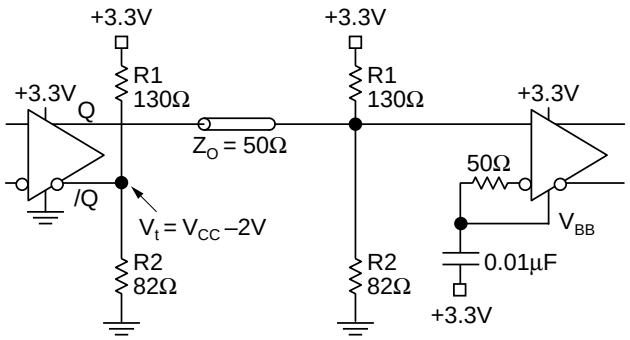
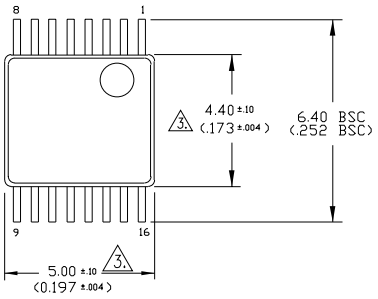


Figure 3. Terminating Unused I/O

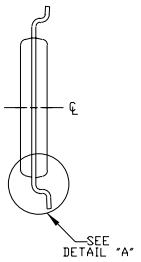
NOTES:

1. Unused output (/Q) must be terminated to balance the output.
2. Micrel's differential I/O logic devices include a V_{BB} reference pin .
3. Connect unused input through 50Ω to V_{BB}. Bypass with a 0.01µF capacitor to V_{CC}, not GND.
4. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω.

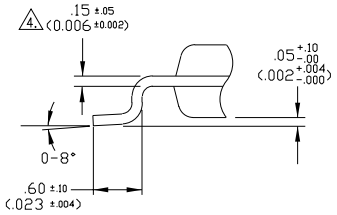
16 LEAD TSSOP (K4-16-1)



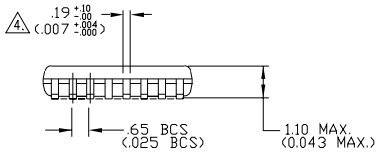
TOP VIEW



END VIEW



DETAIL 'A'
(VIEW ROTATED 90° C.W.)



SIDE VIEW

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 01

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