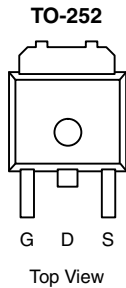


PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a
20	0.0060 at $V_{GS} = 10$ V	26
	0.0095 at $V_{GS} = 4.5$ V	21



Drain Connected to Tab

Ordering Information: SUD50N02-06P-E3 (Lead (Pb) free)

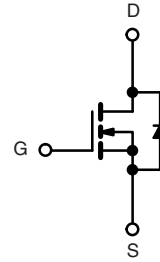
FEATURES

- TrenchFET[®] Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Synchronous Buck DC/DC Conversion
 - Desktop
 - Server



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_A = 25$ °C	26 ^a
		$T_C = 25$ °C	50 ^b
Pulsed Drain Current	I_{DM}	100	A
Continuous Source Current (Diode Conduction) ^a	I_S	26	
Avalanche Current	I_{AS}	45	
Single Pulse Avalanche Energy	E_{AS}	101	mJ
Maximum Power Dissipation	P_D	$T_A = 25$ °C	6.8 ^a
		$T_C = 25$ °C	65
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	18	22	°C/W
		Steady State	40	50	
Maximum Junction-to-Case	R_{thJC}	1.9	2.3		

Notes:

a. Surface mounted on FR4 board, $t \leq 10$ s.

b. Limited by package.

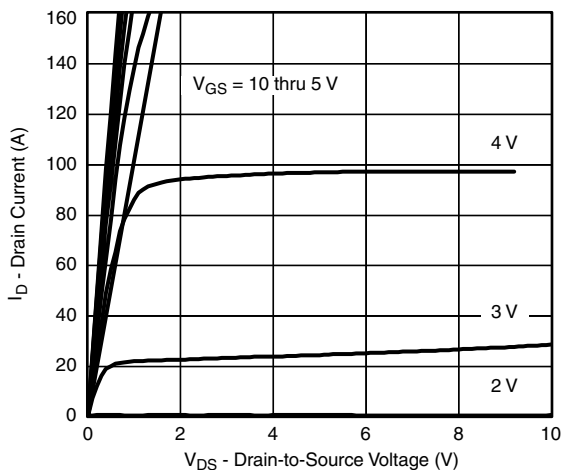
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.8		3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0046	0.006	Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.0084	
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		0.0073	0.0095	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$	15			S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 10\text{ V}, f = 1\text{ MHz}$		2550		μF
Output Capacitance	C_{oss}			900		
Reverse Transfer Capacitance	C_{rss}			415		
Total Gate Charge ^c	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$		19	30	nC
Gate-Source Charge ^c	Q_{gs}			7.5		
Gate-Drain Charge ^c	Q_{gd}			6		
Gate Resistance	R_g		0.5	1.5	2.4	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		11	20	ns
Rise Time ^c	t_r			10	15	
Turn-Off Delay Time ^c	$t_{d(off)}$			24	35	
Fall Time ^c	t_f			9	15	
Source-Drain Diode Ratings and Characteristic ($T_C = 25\text{ }^\circ\text{C}$)						
Pulsed Current	I_{SM}				100	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 50\text{ A}, V_{GS} = 0\text{ V}$		1.2	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		35	70	ns

Notes:

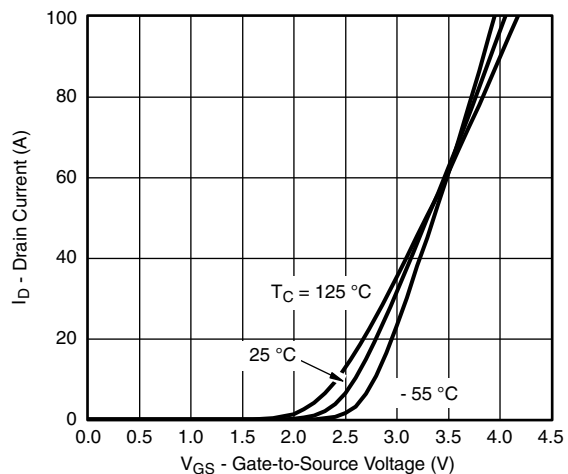
- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C unless noted)

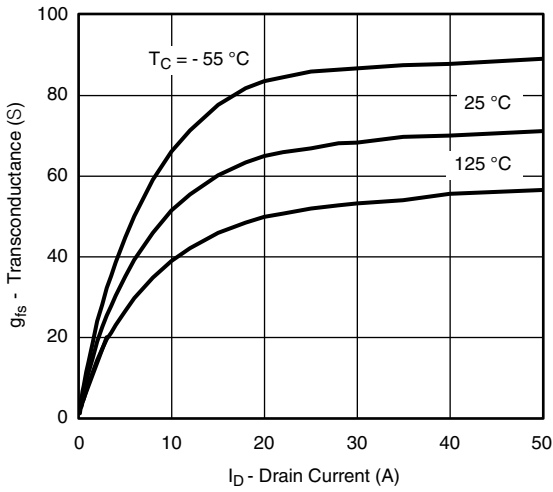


Output Characteristics

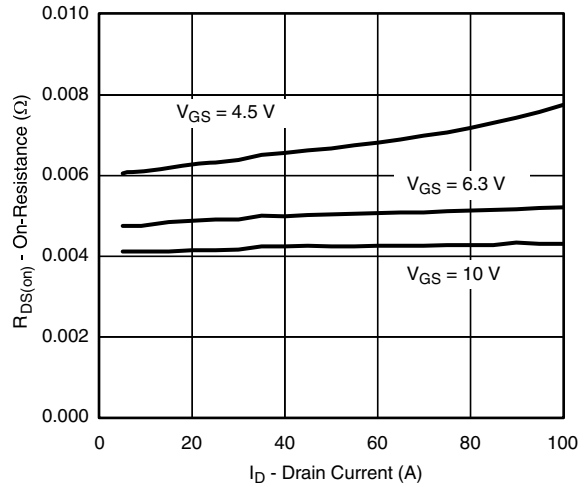


Transfer Characteristics

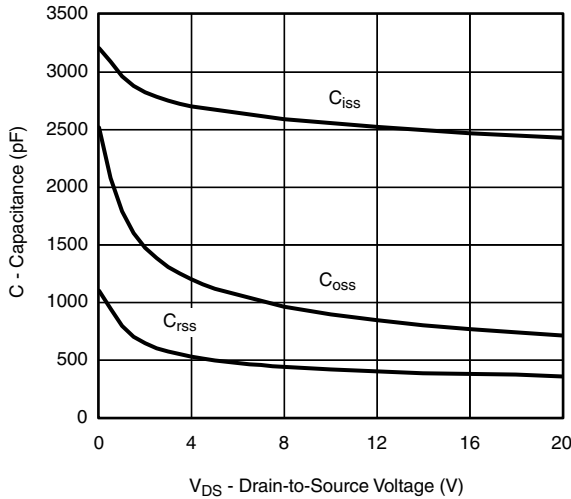
TYPICAL CHARACTERISTICS (25 °C unless noted)



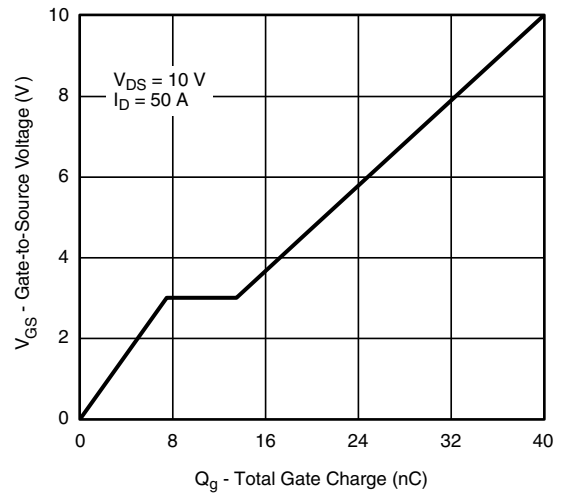
Transconductance



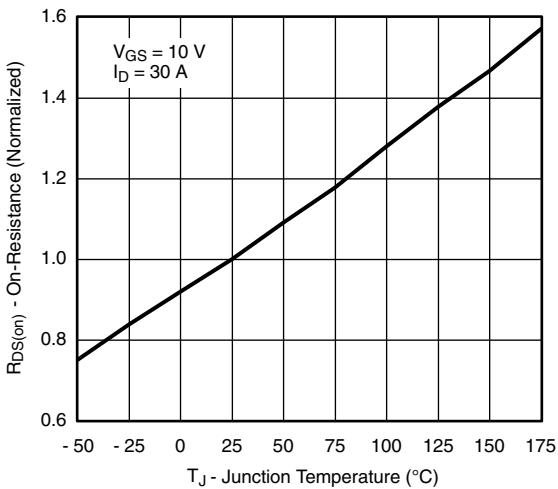
On-Resistance vs. Drain Current



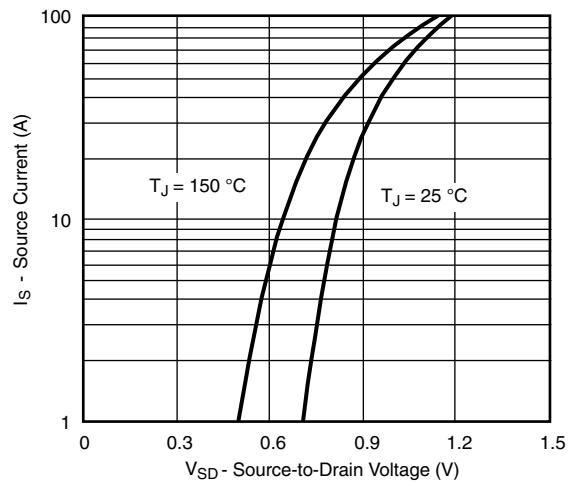
Capacitance



Gate Charge

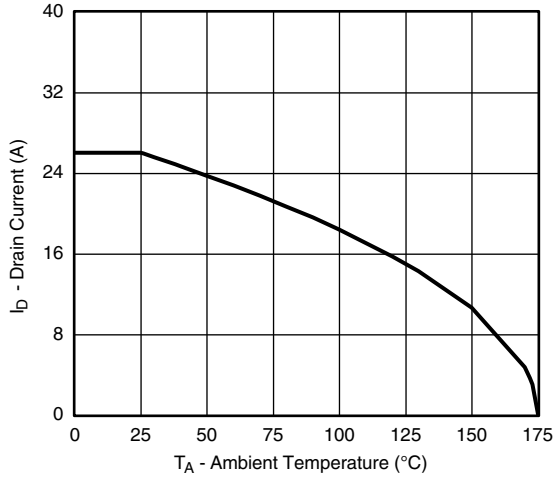


On-Resistance vs. Junction Temperature

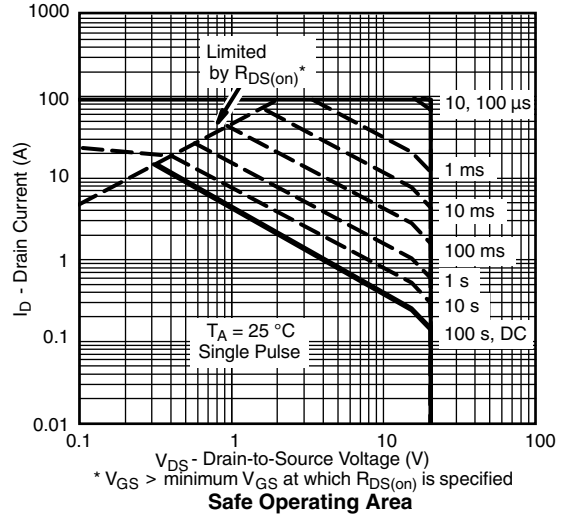


Source-Drain Diode Forward Voltage

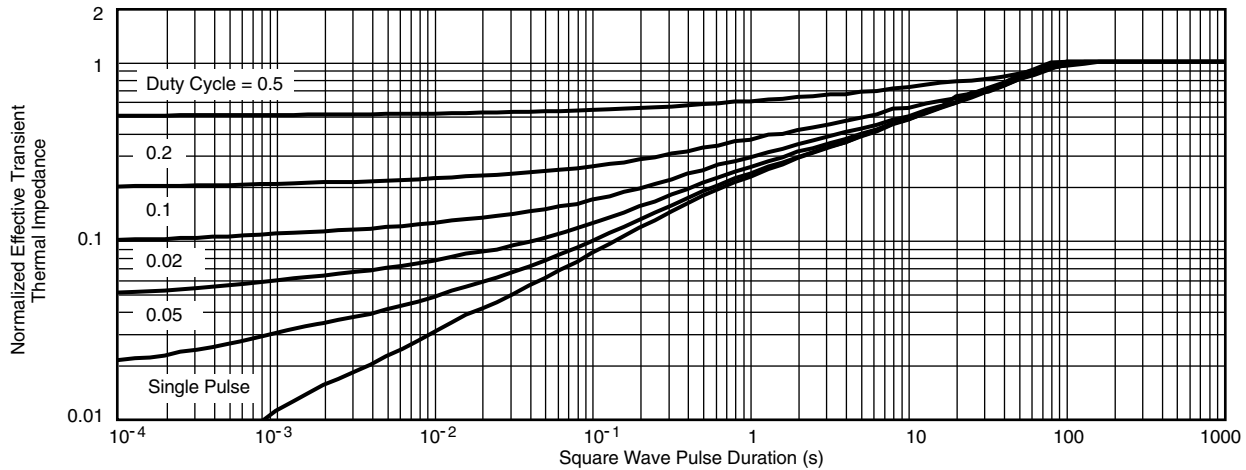
THERMAL RATINGS



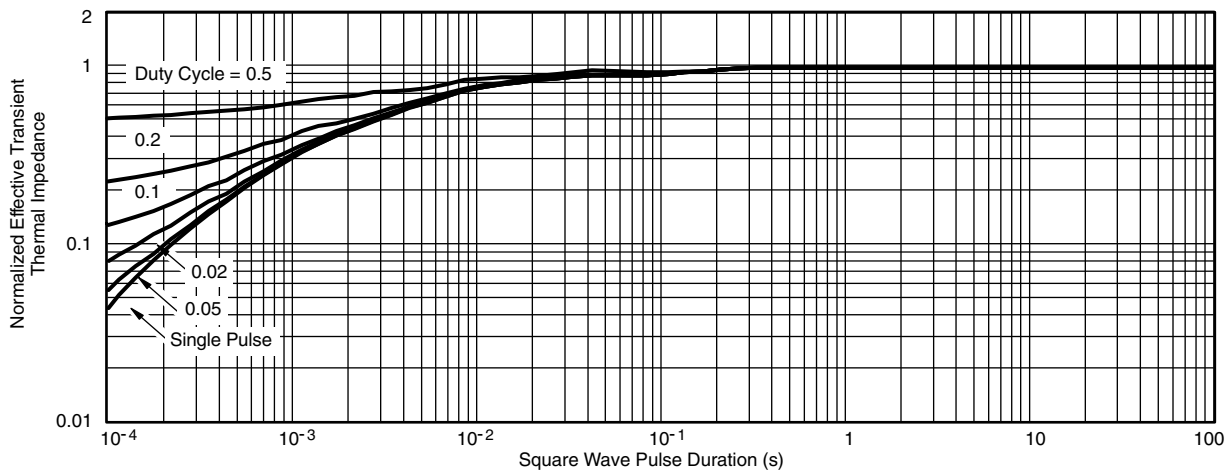
Maximum Drain Current vs. Ambient Temperature



Safe Operating Area

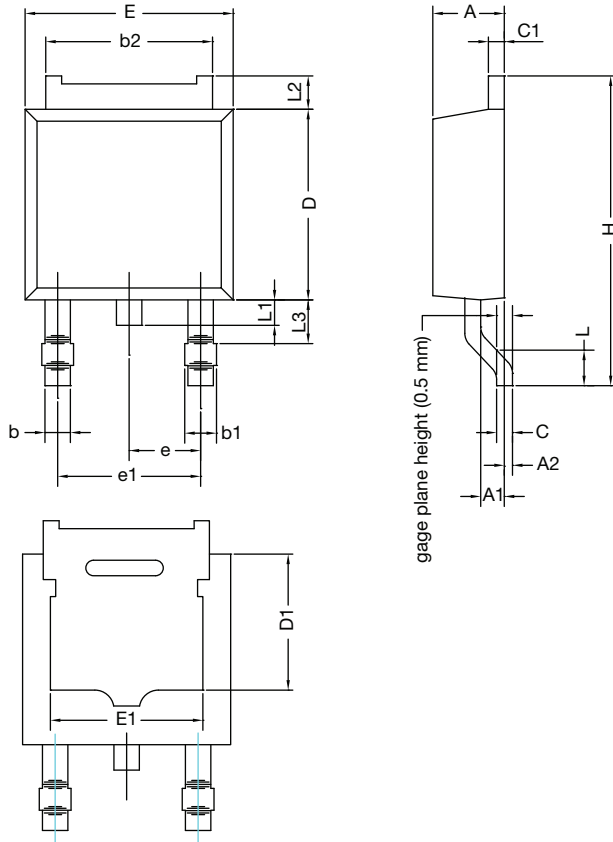


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

TO-252AA CASE OUTLINE



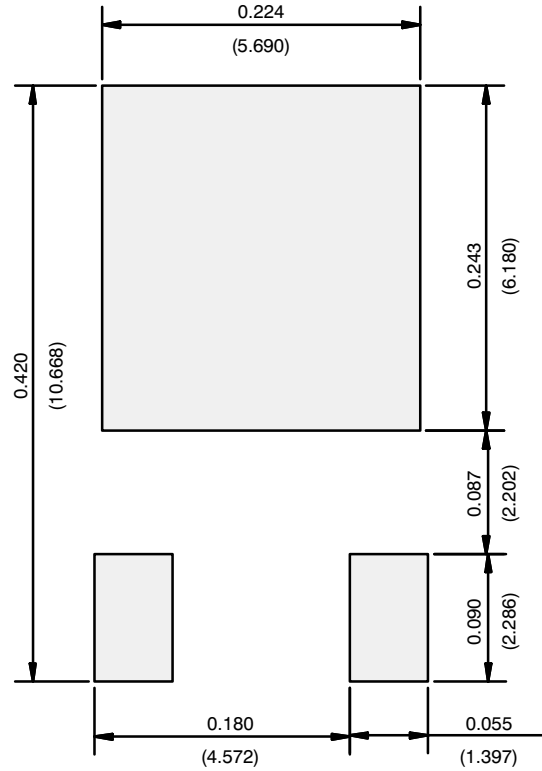
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
A2	0.030	0.127	0.001	0.005
b	0.71	0.88	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.44	0.206	0.214
C	0.46	0.58	0.018	0.023
C1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
D1	4.10	4.45	0.161	0.175
E	6.48	6.73	0.255	0.265
E1	4.49	5.50	0.177	0.217
e	2.28 BSC		0.090 BSC	
e1	4.57 BSC		0.180 BSC	
H	9.65	10.41	0.380	0.410
L	1.40	1.78	0.055	0.070
L1	0.64	1.02	0.025	0.040
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.040	0.060

ECN: T11-0110-Rev. L, 18-Apr-11
DWG: 5347

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
 Dimensions in Inches/(mm)

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