SPT7862

10-BIT, 40 MSPS, DUAL-CHANNEL A/D CONVERTER

FEATURES

- Dual-channel, 10-Bit, 40 MSPS analog-to-digital converter
- Low power dissipation: 320 mW (typical)
- Internal track-and-hold
- Single +5 volt supply
- Tri-state, TTL/CMOS-compatible outputs
- Selectable +3 or +5 V logic I/O
- High ESD protection of 3,500 volts minimum

APPLICATIONS

- Video set-top boxes
- Cellular base stations
- QPSK/QAM RF demodulation
- S-video digitizers
- Composite video digitizers
- Portable and handheld instrumentation
- Medical ultrasound
- Cable modems
- Video frame grabbers

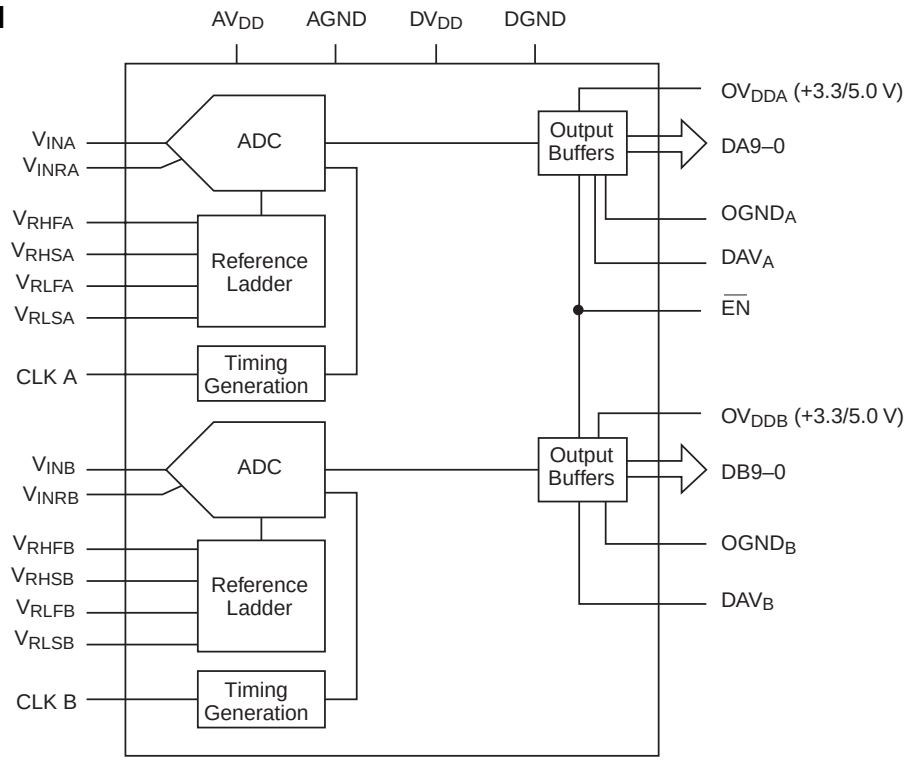
GENERAL DESCRIPTION

The SPT7862 contains two separate 10-bit CMOS analog-to-digital converters that have sampling rates of up to 40 MSPS. Each device has its own separate clock and reference inputs so that they can be used independently in multichannel applications or can be driven from the same inputs for demanding quadrature demodulation and S-video applications. On-chip track-and-hold and advanced proprietary circuit design in a CMOS process technology provide very good dynamic performance.

The SPT7862 operates from a single +5 V supply. Digital data outputs are user selectable at +3 or +5 V. Output data format is straight binary.

The SPT7862 is available in a 64-lead TQFP package (10 x 10 mm) over the industrial temperature range of –40 °C to +85 °C.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... –0.5 V to AV_{DD} +0.5 V
V_{REF} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
$AV_{DD} – DV_{DD}$ ..... ±100 mV
AGND – DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... –40 to +85 °C
Junction Temperature ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... –65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}=OV_{DD}=+5.0$ V, $V_{IN}=0$ to 4 V, f_S=40 MSPS, $V_{RHS}=4.0$ V, $V_{RLS}=0.0$ V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7862 MIN	SPT7862 TYP	SPT7862 MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		V		±1.0		LSB
Differential Nonlinearity		V		±0.5		LSB
Analog Input						
Input Voltage Range		IV	V_{RLS}		V_{RHS}	V
Input Resistance		V		29		kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V		250		MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		V		500		Ω
Voltage Range						
V_{RLS}		IV	0	–	2.0	V
V_{RHS}		IV	3.0	–	AV_{DD}	V
$V_{RHS} – V_{RLS}$		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} – V_{RHS})$		V		90		mV
$\Delta(V_{RLS} – V_{RLF})$		V		75		mV
Conversion Characteristics						
Maximum Conversion Rate		VI	40			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		4.0		ns
Aperture Jitter Time		V		7		ps(rms)
Dynamic Performance						
Effective Number of Bits						
f_{IN} = 3.58 MHz		V		9.1		Bits
f_{IN} = 10.0 MHz		VI	7.8	8.3		Bits
Signal-to-Noise Ratio (without Harmonics)						
f_{IN} = 3.58 MHz		V		57.9		dB
f_{IN} = 10.0 MHz	T_A = +25 °C	I	52	54.2		dB
f_{IN} = 10.0 MHz	$T_A = T_{MIN}$ to T_{MAX}	IV	47			dB

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, AV_{DD}=DV_{DD}=OV_{DD}=+5.0 V, V_{IN}=0 to 4 V, f_S=40 MSPS, V_{RHS}=4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7862 MIN	SPT7862 TYP	SPT7862 MAX	UNITS
Dynamic Performance						
Harmonic Distortion	9 Distortion bins from					
f_{IN} = 3.58 MHz	1024 pt FFT	V		–63		dB
f_{IN} = 10.0 MHz	T_A = +25 °C	I		–55.7	–52	dB
f_{IN} = 10.0 MHz	T_A = T_{MIN} to T_{MAX}	IV			–52	dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN} = 3.58 MHz		V		56.7		dB
f_{IN} = 10.0 MHz	T_A = +25 °C	I	49	51.8		dB
f_{IN} = 10.0 MHz	T_A = T_{MIN} to T_{MAX}	IV	46			dB
Spurious Free Dynamic Range						
f_{IN} = 10.0 MHz		V	56.8	58.3	60	dB
Differential Phase		V		±0.3		Degree
Differential Gain		V		±0.3		%
Channel-to-Channel Crosstalk						
f_{IN} = 3.58 MHz		V		74		dB
f_{IN} = 10.0 MHz		V		67		dB
Inputs						
Logic 1 Voltage		VI	2.1			V
Logic 0 Voltage		VI			0.8	V
Maximum Input Current Low		VI	–10		+10	µA
Maximum Input Current High		VI	–10		+10	µA
Input Capacitance		V		+5		pF
Digital Outputs						
Logic 1 Voltage	I_{OH} = 0.5 mA	VI	OV_{DD} –0.5			V
Logic 0 Voltage	I_{OL} = 1.6 mA	VI			0.44	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data						
Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages OV_{DD}		IV	3.0		5.0	V
DV_{DD}		IV		5.0		V
AV_{DD}		IV		5.0		V
Currents AI_{DD} + DI_{DD}		VI		52	62	mA
OI_{DD}		VI		12	14	mA
Power Dissipation		VI		320	380	mW
Power Supply Refection Ratio		V		70		dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1a – Timing Diagram 1

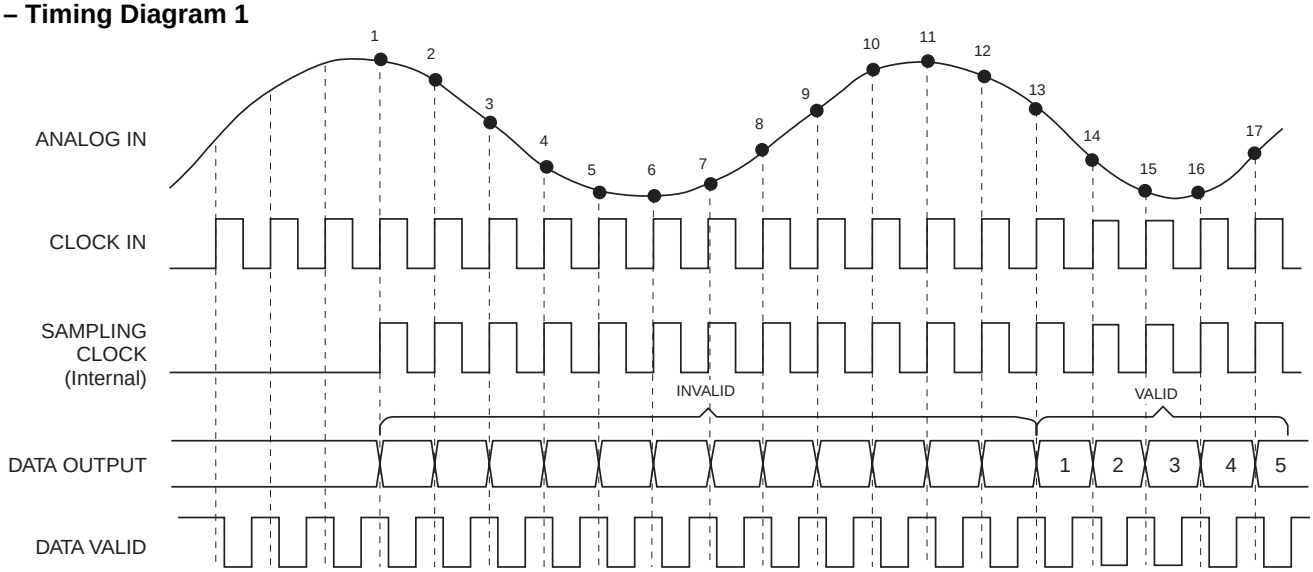


Figure 1b – Timing Diagram 2

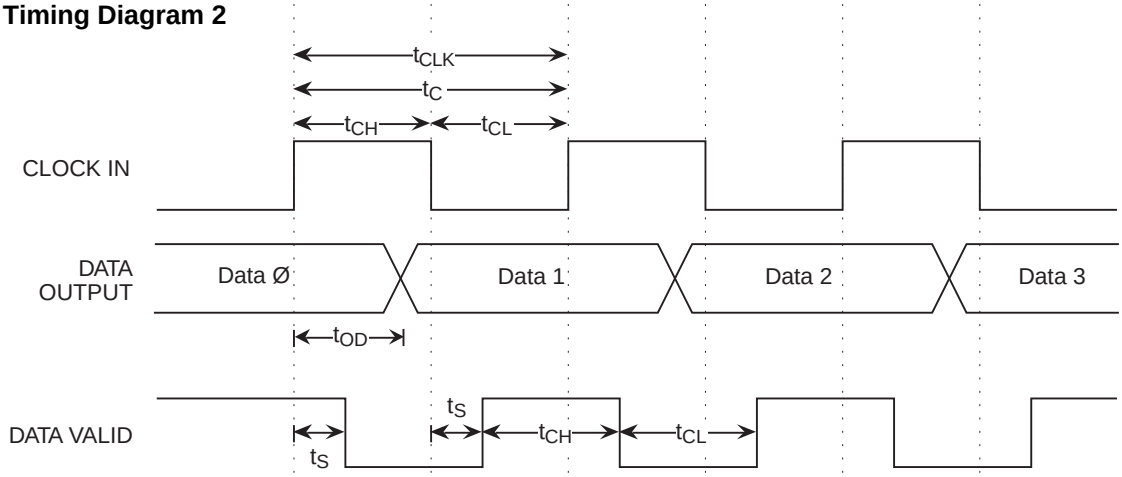
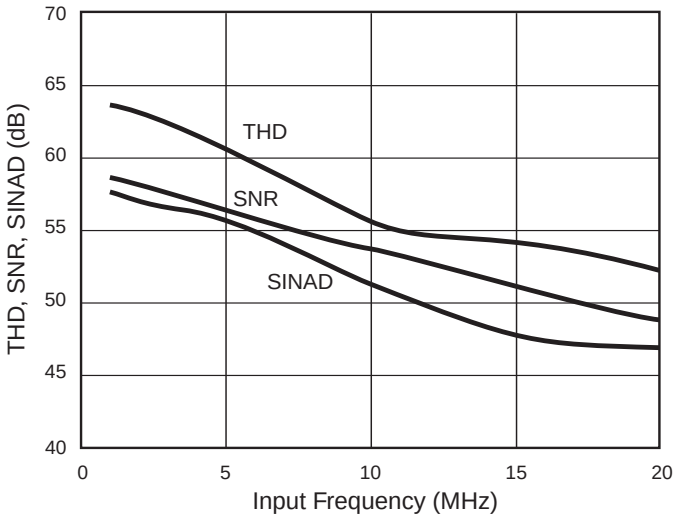


Table I – Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_C	t_{CLK}			ns
Clock Period	t_{CLK}	25			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Clock to Output Delay (30 pF Load)	t_{OD}		17	20	ns
Clock to DAV (30 pF load)	t_S		10	16	ns

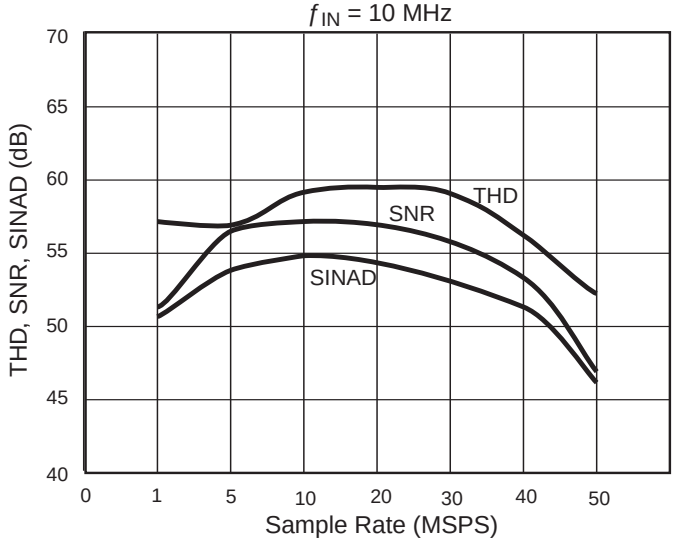
TYPICAL PERFORMANCE CHARACTERISTICS

THD, SNR, SINAD vs Input Frequency



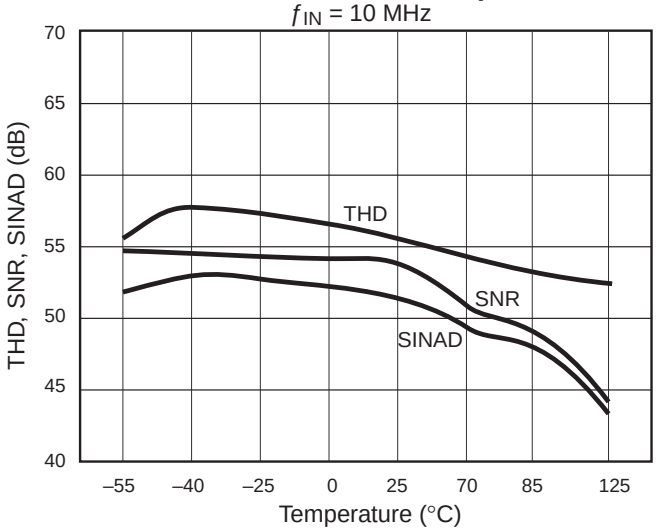
THD, SNR, SINAD vs Sample Rate

f_{IN} = 10 MHz



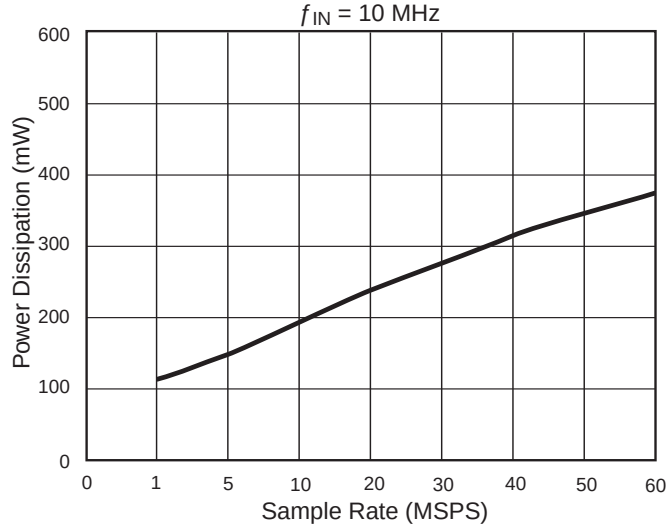
THD, SNR, SINAD vs Temperature

f_{IN} = 10 MHz



Power Dissipation vs Sample Rate

f_{IN} = 10 MHz



Spectral Response

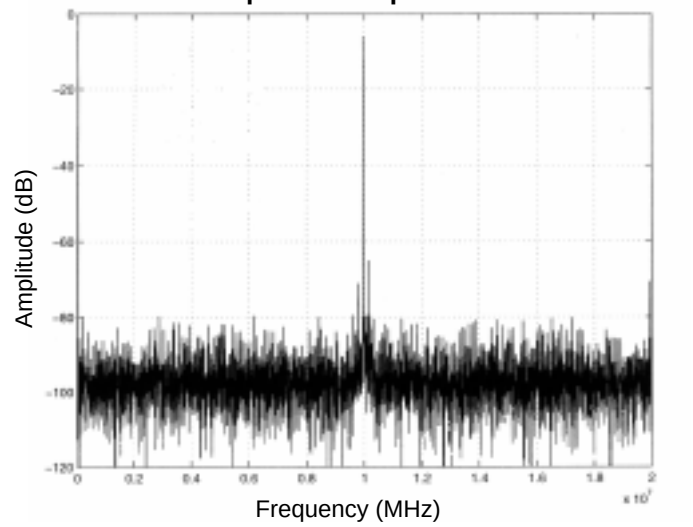
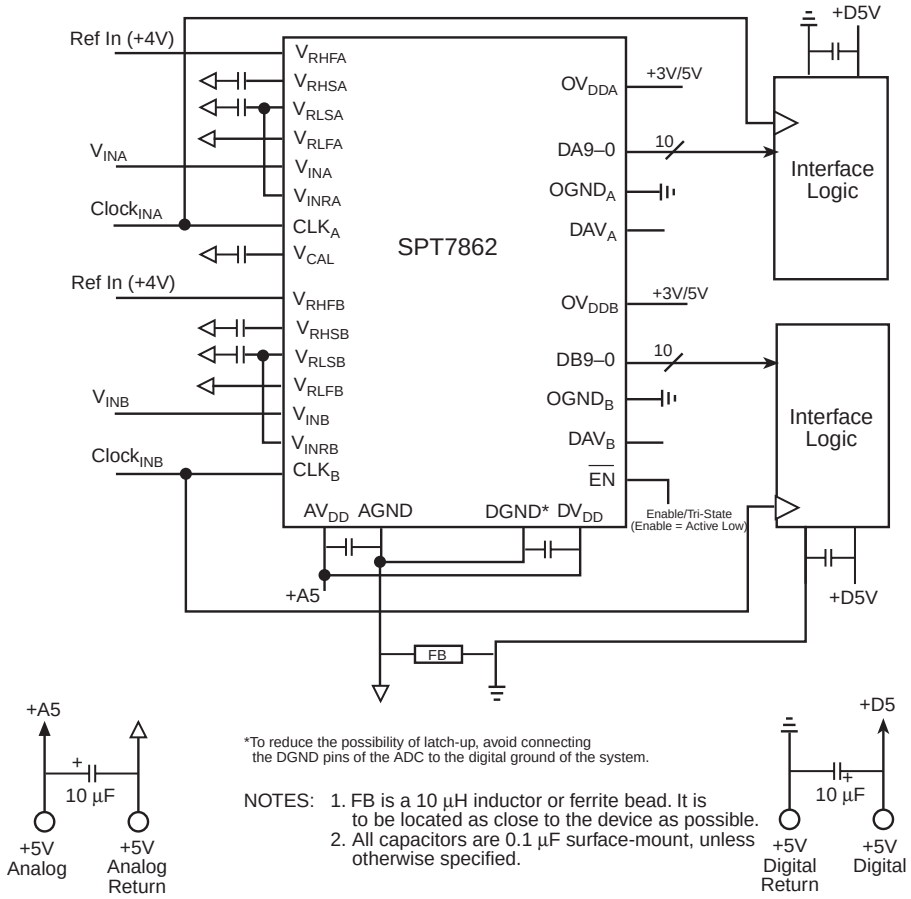


Figure 2 – Typical Interface Circuit



TYPICAL INTERFACE CIRCUIT

Very few external components are required to achieve the stated device performance. Figure 2 shows the typical interface requirements when using the SPT7862 in normal circuit operation. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

SPT suggests that both the digital and the analog supply voltages on the SPT7862 be derived from a single analog supply as shown in figure 2. A separate digital supply should be used for all interface circuitry. SPT suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the dual CMOS ADC is shown in the block diagram. Each ADC design contains 16 identical successive approximation (SAR) ADC sections (all operating in parallel), a 16-phase clock generator, an 11-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each SAR ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Table II – Clock Cycles

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5–15	11-bit SAR conversion
16	Data transfer

The 16-phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent SAR ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one SAR ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparator's response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each SAR ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low, since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

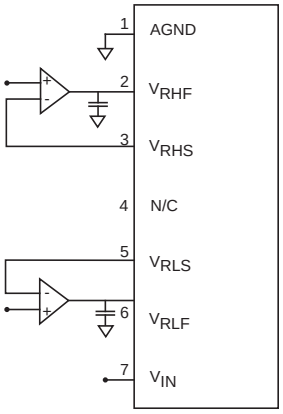
The SPT7862 requires the use of a single external voltage reference for driving the high side of each reference ladder. Each ladder is totally independent and may operate at different voltage levels. The high side of the reference ladder must operate within a range of 3 V to 5 V. The lower side of each ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 3, offset and gain errors of less than ±2 LSB can be obtained.

In cases in which wider variations in offset and gain can be tolerated, the external reference can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 4. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

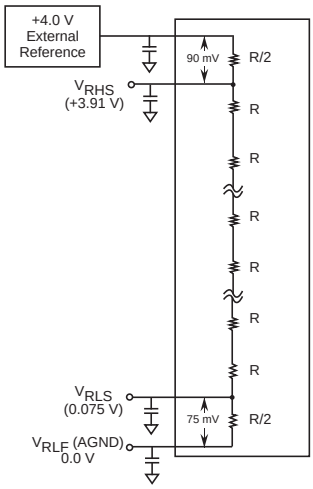
The reference ladder circuit shown in figure 4 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Figure 3 – Ladder Force/Sense Circuit for Each ADC



All capacitors are 0.01 µF

Figure 4 – Simplified Reference Ladder Drive Circuit Without Force/Sense Circuit



R=30 Ω (typ)
All capacitors are 0.01 µF

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS}$ = 2.25 % of ($V_{RHF} - V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF}$ = 1.9 % of ($V_{RHF} - V_{RLF}$) (typical).

Figure 4 shows an example of expected voltage drops for a specific case. V_{REF} of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

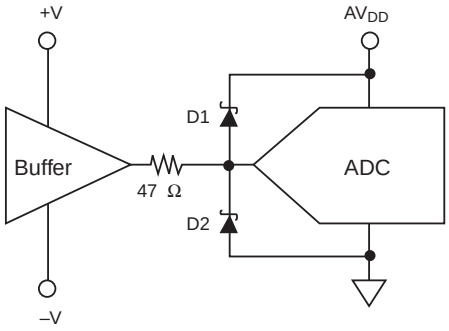
ANALOG INPUT

V_{INA} and V_{INB} are the analog inputs and V_{INRA} and V_{INRB} are the respective input returns. Each input return is typically tied to its respective low side reference ladder sense line. (See Figure 2.) The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See the Voltage Reference section.)

The drive requirements for the analog inputs are very minimal, when compared to most other converters, due to the SPT7862's extremely low input capacitance of only 5 pF and a high input resistance in excess of 29 kΩ.

Each analog input should be protected through a series resistor and diode clamping circuit as shown in figure 5.

Figure 5 – Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

CALIBRATION

The SPT7862 uses a user-transparent, auto-calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation.

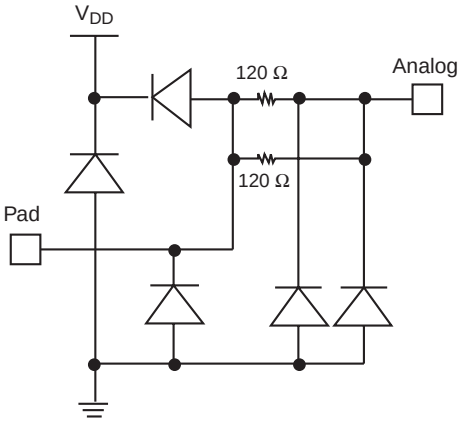
Upon power up, the SPT7862 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon power up of 250 µsec (for a 40 MHz clock). Once calibrated, the SPT7862 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7862 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 6. This circuit provides ESD robustness and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 6 – On-Chip Protection Circuit



CLOCK INPUT

Each ADC is driven independently from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, each ADC can operate over a wide range of input clock duty cycles without degrading the dynamic performance.

DIGITAL OUTPUTS

The digital outputs (DA9–0 and DB9–0) are driven by separate supplies (OV_{DDA} and OV_{DDB}) ranging from +3 V to +5 V. This feature makes it possible to drive the SPT7862's TTL/CMOS-compatible outputs with the user's logic system supply. Each digital output supply may be driven independently. The format of the output data (D0–D9) is straight binary. (See Table III.) The outputs are latched on the rising edge of CLK. The $\overline{EN}$ pin controls tri-stating of both data output ports. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table III – Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. –1/2 LSB	0	11 1111 111Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	00 0000 000Ø
0.0 V	0	00 0000 0000

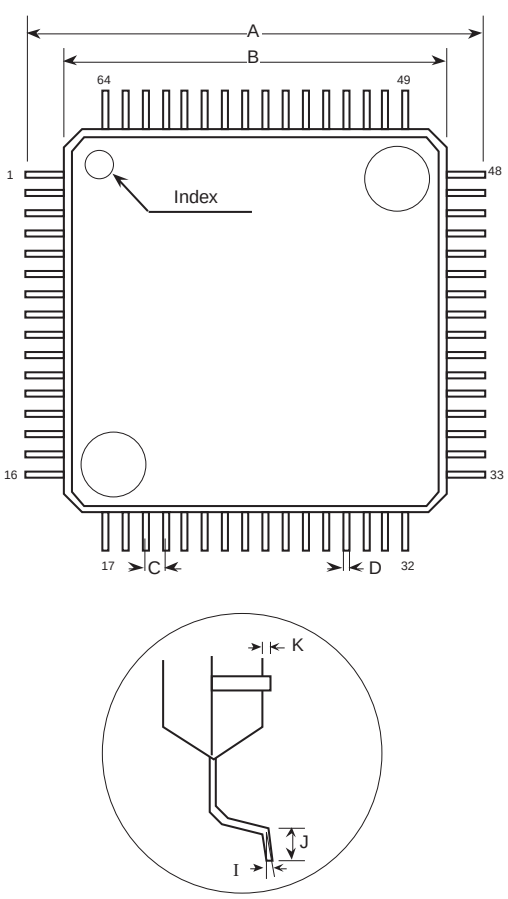
(Ø indicates the flickering bit between logic 0 and 1)

EVALUATION BOARD

The EB7862 evaluation board is available to aid designers in demonstrating the full performance of the SPT7862. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7862 is also available. Contact the factory for price and availability.

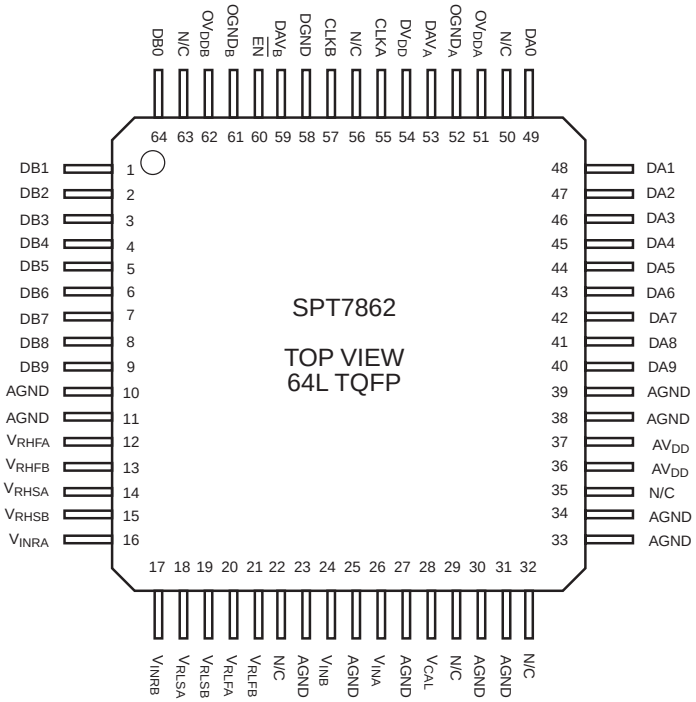
PACKAGE OUTLINE

64-Lead TQFP



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.465	0.480	11.80	12.20
B	0.390	0.398	9.90	10.10
C	0.017	0.023	0.42	0.58
D	0.006	0.010	0.15	0.26
E	0.295 typ		7.5 typ	
F	0.433 typ	0.000	11 typ	
G	0.055	0.067	1.40	1.70
H	0.005	0.005	0.125	0.132
I	0-10°		0-10°	
J	0.012	0.028	0.30	0.70
K	0.000	0.008	0.00	0.20

PIN ASSIGNMENTS



PIN FUNCTIONS

Pin Name	Description
V_{INA}	Analog Input (A)
V_{INB}	Analog Input (B)
V_{INRA}	Analog Input Return (A)
V_{INRB}	Analog Input Return (B)
$V_{RHFA/B}$	V_{REF} High Force Input A/B
$V_{RHSA/B}$	V_{REF} High Sense Input A/B
$V_{RLFA/B}$	V_{REF} Low Force Input A/B
$V_{RLSA/B}$	V_{REF} Low Sense Input A/B
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
OV_{DD} A/B	Digital Output Power Supply +3.3 V to +5.0 V
AGND	Analog Ground
DGND	Digital Ground
OGND A/B	Digital Output Ground
CLK A/B	Input Clock A/B (separate)
$\overline{EN}$	Enable Outputs (Active Low)
D0–9A	Data Outputs A (10 bits)
D0–9B	Data Outputs B (10 bits)
DAV A/B	Data Available A/B
V_{CAL}	Decoupling Pin

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE
SPT7862SIT	–40 to +85 °C	64-Lead TQFP

Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.