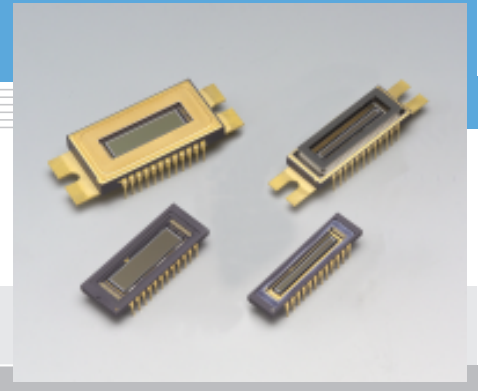


# CCD area image sensor S9972/S9973 series

Front-illuminated FFT-CCD, high near IR sensitivity



The S9972/S9973 series are families of FFT-CCD image sensors specifically designed for low-light-level detection in scientific applications. By using the binning operation, the S9972/S9973 series can be used as a linear image sensor having a long aperture in the direction of the device length. This makes the S9972/S9973 series ideally suited for use in spectrophotometry. The binning operation offers significant improvement in S/N and signal processing speed compared with conventional methods by which signals are digitally added by an external circuit. The S9972/S9973 series also feature low noise and low dark signal (MPP mode operation). This enables low-light-level detection and long integration time, thus achieving a wide dynamic range.

The S9972/S9973 series have an effective pixel size of  $24 \times 24 \mu\text{m}$  and are available in image areas of  $24.576 \text{ (H)} \times 2.976 \text{ (V)} \text{ mm}^2$  ( $1024 \times 124$  pixels) and  $24.576 \text{ (H)} \times 6.048 \text{ (V)} \text{ mm}^2$  ( $1024 \times 252$  pixels). The S9972/S9973 series are pin compatible with the S9970/S9971 series. (Operating conditions and characteristics are a little bit different from the S9970/S9971 series.)

### Features

- $1024 \text{ (H)} \times 124 \text{ (V)}$  and  $1024 \text{ (H)} \times 252 \text{ (V)}$  pixel format
- Pixel size:  $24 \times 24 \mu\text{m}$
- Line/pixel binning
- 100% fill factor
- Wide dynamic range
- Low dark signal
- Low readout noise
- MPP operation
- High near IR sensitivity

### Applications

- Fluorescence spectrometer, ICP
- Raman spectrometer
- Industrial inspection requiring
- Semiconductor inspection
- DNA sequencer
- Low-light-level detection

### Selection guide

Type no.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]	Suitable multichannel detector head
S9972-1007	Non-cooled	$1044 \times 128$	$1024 \times 124$	$24.576 \times 2.976$	C7020-02
S9972-1008		$1044 \times 256$	$1024 \times 252$	$24.576 \times 6.048$	
S9973-1007	One-stage	$1044 \times 128$	$1024 \times 124$	$24.576 \times 2.976$	C7021-02
S9973-1008	TE-cooled	$1044 \times 256$	$1024 \times 252$	$24.576 \times 6.048$	C7025-02

### General ratings

Parameter	S9972 series	S9973 series
Pixel size	$24 \text{ (H)} \times 24 \text{ (V)} \mu\text{m}$	
Vertical clock phase	2-phase	
Horizontal clock phase	2-phase	
Output circuit	One-stage MOSFET source follower	
Package	24-pin ceramic DIP (refer to dimensional outlines)	
Window*1	Quartz glass	S9973-1007: sapphire S9973-1008: AR-coated sapphire

\*1: Temporary window type (ex. S9972-1007N) and UV coat type (ex. S9972-1007UV) are available upon request. (On the temporary window type, a window is temporarily attached by tape to protect the CCD chip and wires.)

■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-15	-	+15	V
IGH voltage	VIG1H, VIG2H	-15	-	+15	V
SG voltage	VSG	-15	-	+15	V
OG voltage	VOG	-15	-	+15	V
RG voltage	VRG	-15	-	+15	V
TG voltage	VTG	-15	-	+15	V
Vertical clock voltage	VP1V, VP2V	-15	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	18	20	22	V	
Reset drain voltage	VRD	12	13	14	V	
Output gate voltage	VOG	-0.5	0	2	V	
Substrate voltage	VSS	-	0	-	V	
Test point (vertical input source)	VISV	-	VRD	-	V	
Test point (horizontal input source)	VISH	-	VRD	-	V	
Test point (vertical input gate)	VIG1V, VIG2V	-8	0	-	V	
Test point (horizontal input gate)	VIG1H, VIG2H	-8	0	-	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	0	4	6	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	0	4	6	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	0	4	6	V
	Low	VSSL	-9	-8	-7	
Reset gate voltage	High	VRGH	0	4	6	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	0	4	6	V
	Low	VTGL	-9	-8	-7	
External load resistance	RL	9	10	11	kΩ	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	0.1	1	MHz
Vertical shift register capacitance	S9972/S9973-1007	-	1600	-	pF
	S9972/S9973-1008	-	3200	-	
Horizontal shift register capacitance	CP1H, CP2H	-	180	-	pF
Summing gate capacitance	CSG	-	7	-	pF
Reset gate capacitance	CRG	-	7	-	pF
Transfer gate capacitance	CTG	-	100	-	pF
Transfer efficiency*2	CTE	0.99995	0.99999	-	-
DC output level	Vout	12	15	18	V
Output impedance	Zo	-	3	-	kΩ
Power dissipation*3	P	-	15	-	mW

\*2: Charge transfer efficiency per pixel, measured at half of the full well capacity

\*3: Power dissipation of the on-chip amplifier plus load resistance

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	120	240	-	ke <sup>-</sup>
	Horizontal		240	480	-	
CCD node sensitivity*4		Sv	-	2.8	-	μV/e <sup>-</sup>
Dark current*5 (MPP mode)	+25 °C	DS	-	2000	30000	e <sup>-</sup> /pixel/s
	0 °C		-	100	1500	
Readout noise*6		Nr	-	4	18	e <sup>-</sup> rms
Dynamic range*7	Line binning	-	60000	120000	-	-
	Area scanning		30000	60000	-	
Spectral response range		λ	-	400 to 1100	-	nm
Photo response non-uniformity*8		PRNU	-	-	±10	%
Blemish	Point defects*9	-	-	-	0	-
	Cluster defects*10		-	-	0	
	Column defects*11		-	-	0	

\*4: V<sub>OD</sub>=20 V , Load resistance=10 kΩ

\*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

\*6: -40 °C, operating frequency is 80 kHz.

\*7: Dynamic range (DR) = Full well capacity / Readout noise

\*8: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 560 nm)

$$\text{Photo response non-uniformity} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100 \text{ [%]}$$

\*9: White spots

Pixels that generate dark current higher than 3% of the saturation. (Measured at 0 °C, T<sub>s</sub>=1 s)

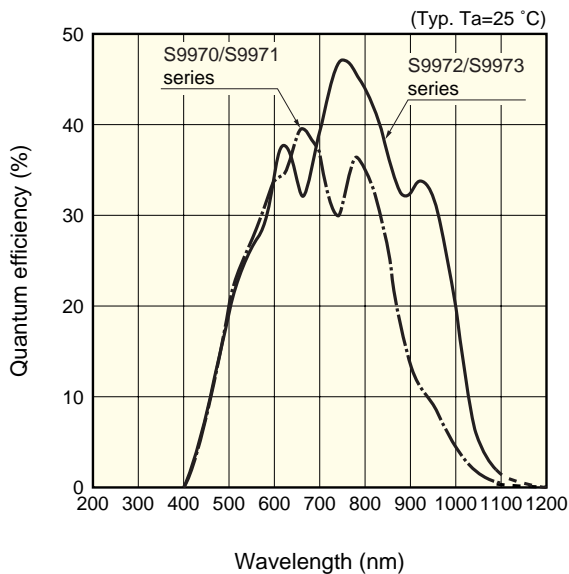
Black spots

Pixels whose sensitivity is lower than one-half of the average pixel output (Measured with uniform light producing one-half of the saturation charge)

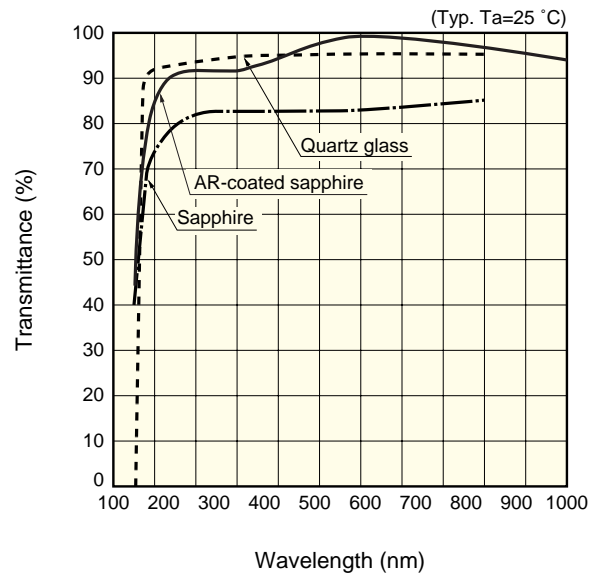
\*10: 2 to 9 contiguous defective pixels

\*11: 10 or more contiguous defective pixels

■ Spectral response (without window)\*12



■ Spectral transmittance characteristics of window material

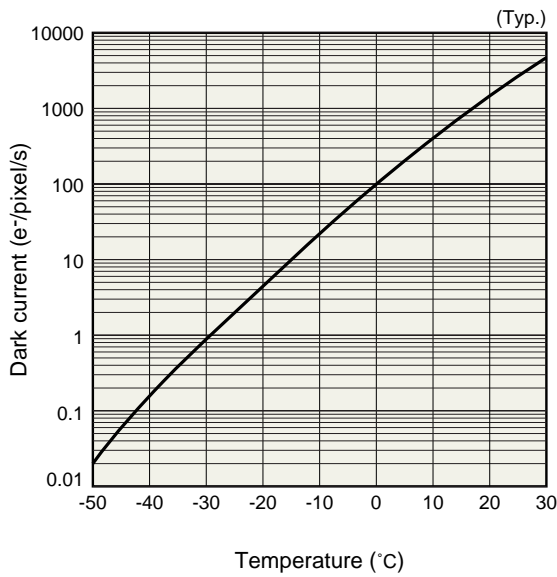


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\*12: Spectral response with sapphire or AR-coated sapphire is decreased according to the spectral transmittance characteristic of window material.

### ■ Dark current vs. temperature



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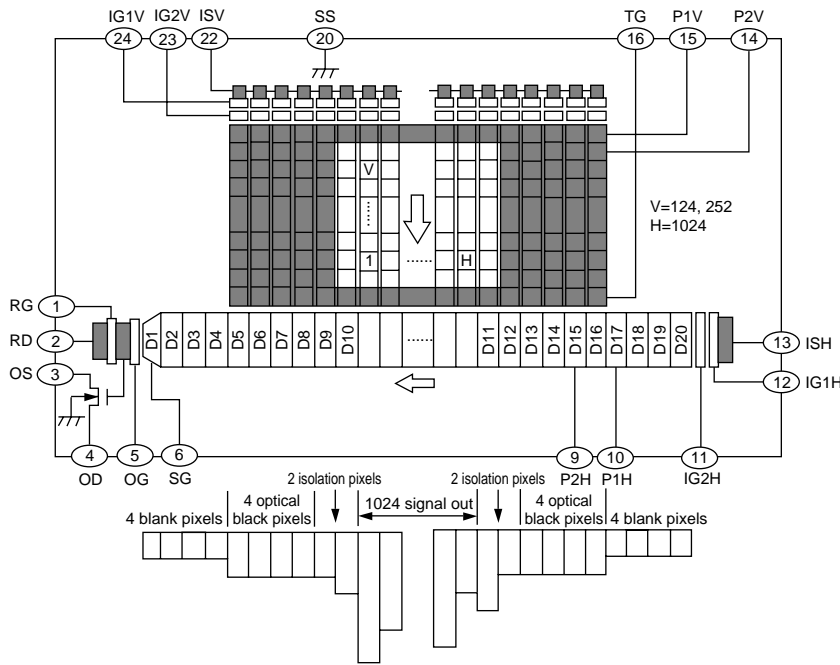
### ■ Window material

Type No.	Window material
S9972 series	Quartz glass*13 (option: window-less)
S9973-1007	Sapphire*14 (option: window-less)
S9973-1008	AR-coated sapphire*14 (option: window-less)

\*13: Resin sealing

\*14: Hermetic sealing

### ■ Device structure (conceptual drawing of top view in dimensional outlines)



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### Pixel format

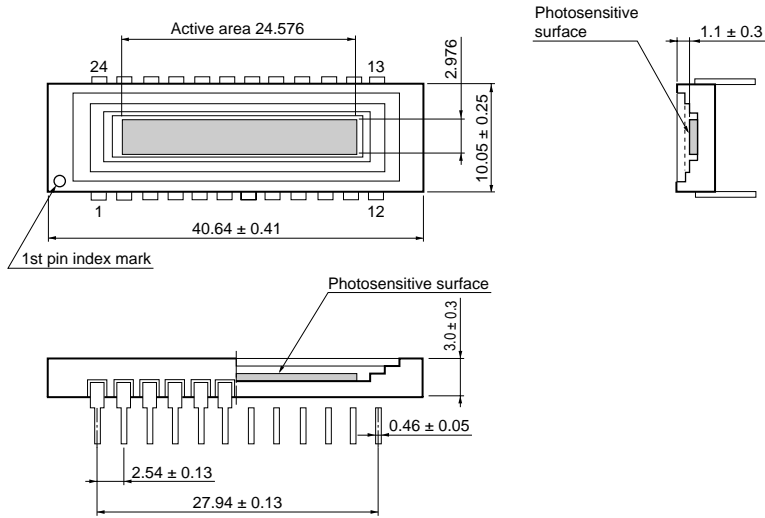
Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	2	1024	2	4	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
2	124 or 252	2

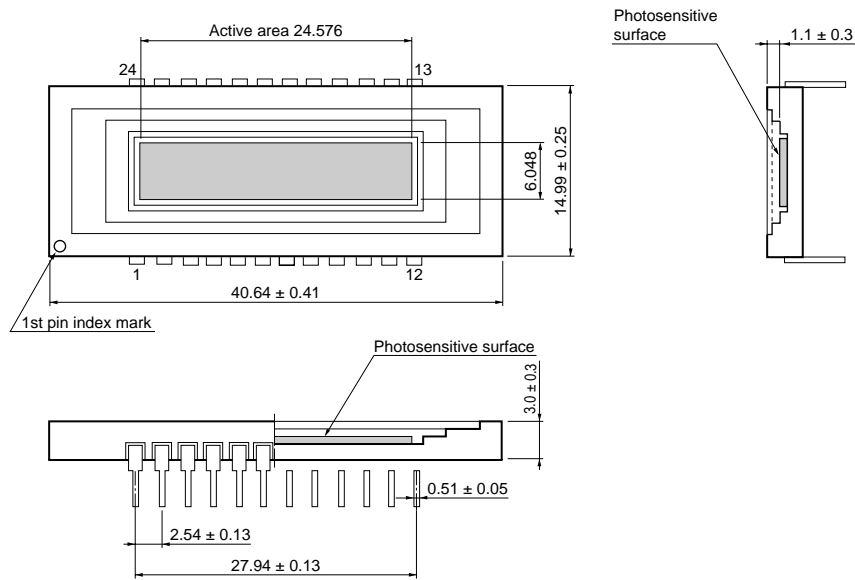


■ Dimensional outlines (unit: mm)

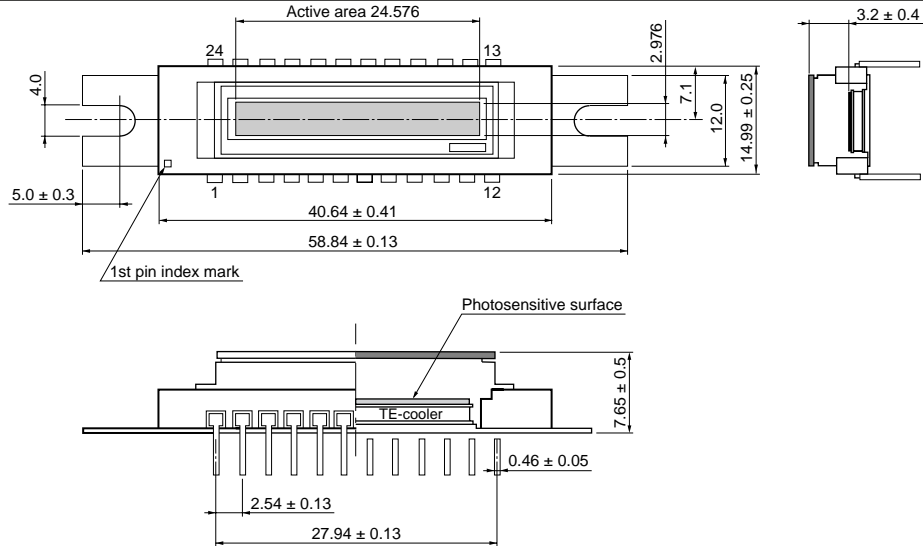
## S9972-1007



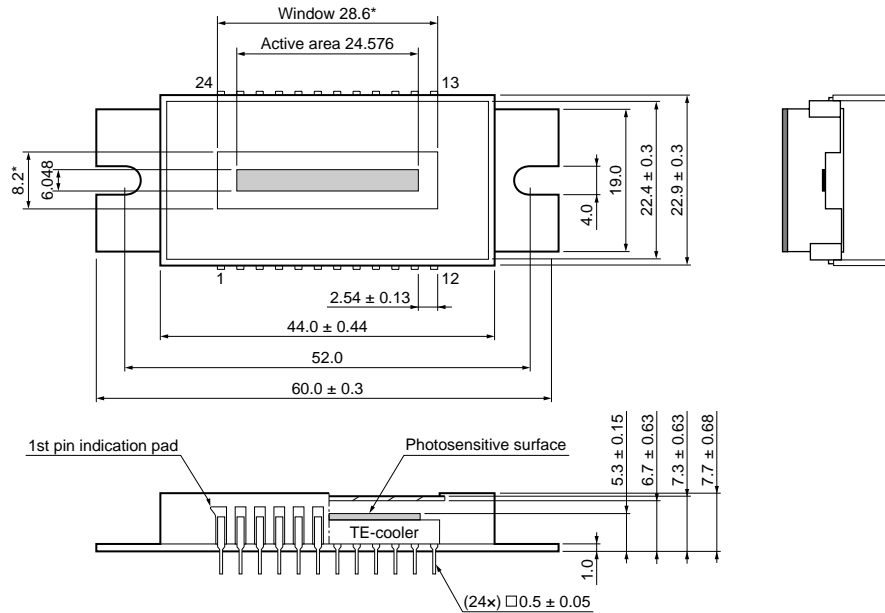
## S9972-1008



## S9973-1007



## S9973-1008



\* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics of window material" graph

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### Pin connections

Pin No.	S9972 series		S9973 series		Remark (standard operation)
	Symbol	Description	Symbol	Description	
1	RG	Reset gate	RG	Reset gate	
2	RD	Reset drain	RD	Reset drain	+13 V
3	OS	Output transistor source	OS	Output transistor source	RL=10 kΩ
4	OD	Output transistor drain	OD	Output transistor drain	+20 V
5	OG	Output gate	OG	Output gate	0 V
6	SG	Summing gate	SG	Summing gate	Same timing as P2H
7	-		Th1	Thermistor	
8	-		Th2	Thermistor	
9	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	0 V
12	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	0 V
13	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Shorted to RD
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	TG <sup>*16</sup>	Transfer gate	TG <sup>*16</sup>	Transfer gate	Same timing as P2V
17	-		-		
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	-		-		
22	ISV	Test point (vertical input source)	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	IG2V	Test point (vertical input gate-2)	0 V
24	IG1V	Test point (vertical input gate-1)	IG1V	Test point (vertical input gate-1)	0 V

\*16: TG is an isolation gate between vertical register and horizontal register. In standard operation, the same pulse as P2V should be applied to TG.

## ■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	S9973-1007	S9973-1008	Unit
Internal resistance	R <sub>int</sub>	T <sub>a</sub> =25 °C	6.0	1.2	Ω
Maximum current* <sup>17</sup>	I <sub>max</sub>	T <sub>c</sub> * <sup>18</sup> =T <sub>h</sub> * <sup>19</sup> =25 °C	1.5	3.0	A
Maximum voltage	V <sub>max</sub>	T <sub>c</sub> * <sup>18</sup> =T <sub>h</sub> * <sup>19</sup> =25 °C	8.8	3.6	V
Maximum heat absorption* <sup>20</sup>	Q <sub>max</sub>		6.7	5.1	W
Maximum temperature of hot side	-		70		°C

\*17: If the current is greater than I<sub>max</sub>, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.

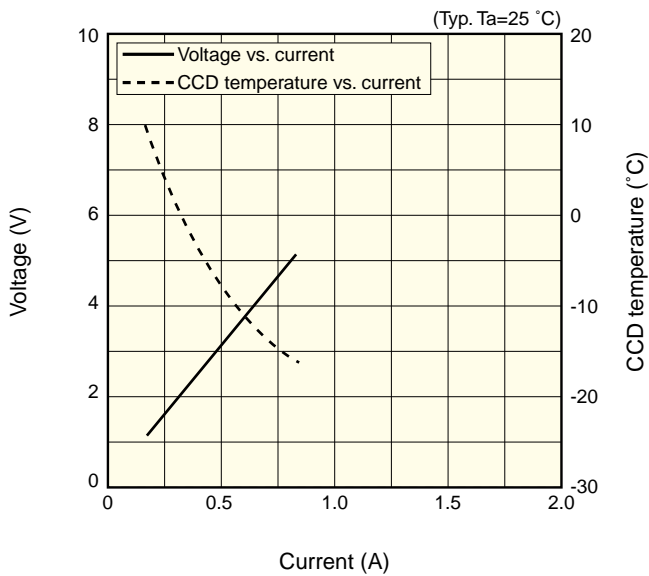
\*18: Temperature of cool side of thermoelectric cooler

\*19: Temperature of hot side of thermoelectric cooler

\*20: This is a heat absorption when the maximum current is supplied to the TE-cooler.

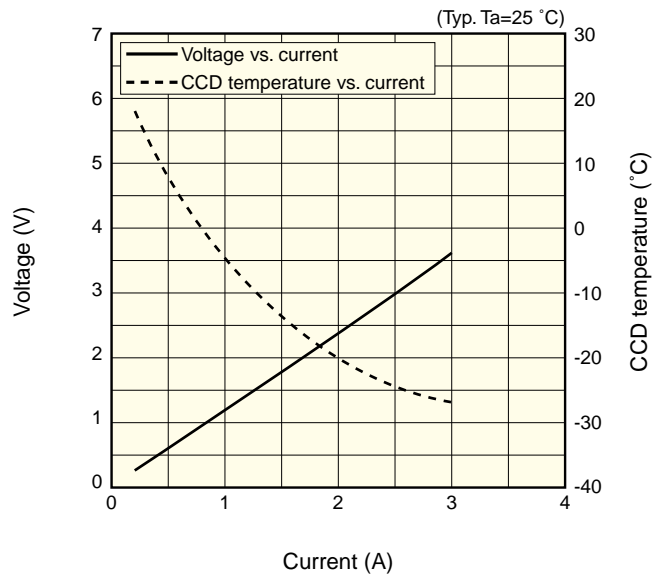
## ■ TE-cooler characteristics

S9973-1007



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S9973-1008



KMPD80179EB



■ Specifications of built-in temperature sensor

A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$$

$R_{T1}$ : Resistance at absolute temperature T1 [K]

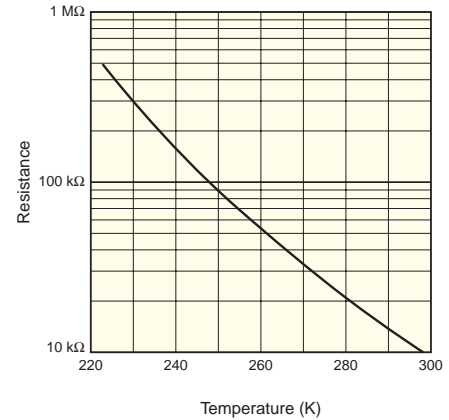
$R_{T2}$ : Resistance at absolute temperature T2 [K]

$B_{T1/T2}$ : B constant [K]

The characteristics of the thermistor used are as follows.

$R_{298}=10\text{ k}\Omega$

$B_{298/323}=3450\text{ K}$



KMPD8011EB

■ Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist strap, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature gradient rate

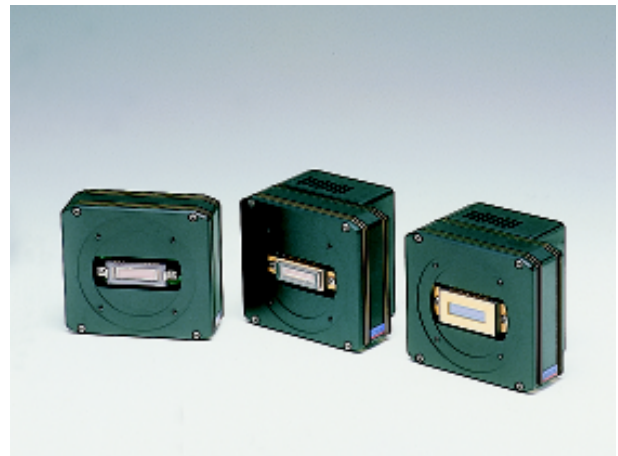
When using an external cooler, the element cooling/heating temperature gradient rate should be set at less than 5 K/min.

Multichannel detector head (C7020-02, C7021-02, C7025-02)



**Features**

- C7020-02: for S9972 series  
C7021-02: for S9973-1007  
C7025-02: for S9973-1008
- Area scanning or full line-binning operation
- Readout frequency: 250 kHz
- Readout noise: 20 e<sup>-</sup>rms
- ΔT=50 °C (ΔT changes by radiation method.)

Input	Symbol	Value
Supply voltage	V <sub>D1</sub>	+5 Vdc, 200 mA
	V <sub>A1+</sub>	+15 Vdc, +100 mA
	V <sub>A1-</sub>	-15 Vdc, -100 mA
	V <sub>A2</sub>	+24 Vdc, 30 mA
	V <sub>D2</sub>	+5 Vdc, 30 mA (C7021-02, C7025-02)
	V <sub>p</sub>	+5 Vdc, 2.5 A (C7021-02, C7025-02)
	V <sub>F</sub>	+12 Vdc, 100 mA (C7021-02, C7025-02)
Master start	φ <sub>ms</sub>	HCMOS logic compatible
Master clock	φ <sub>mc</sub>	HCMOS logic compatible, 1 MHz



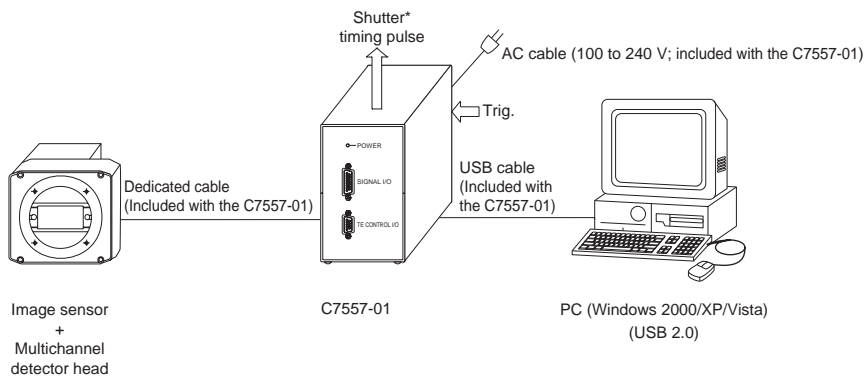
## Multichannel detector head controller

Type no.	Interface	Photo	Accessories
S7557	SCSI		<ul style="list-style-type: none"> <li>·SCSI terminator</li> <li>·Fuse (2.5 A)</li> <li>·Detector head connection cable</li> <li>·AC cable</li> <li>·Software (compatible OS: Windows 98/ME*21)</li> <li>·Operation manual</li> </ul>
S7557-01	USB2.0		<ul style="list-style-type: none"> <li>·USB cable</li> <li>·Fuse (2.5 A)</li> <li>·Detector head connection cable</li> <li>·AC cable</li> <li>·Software (compatible OS: Windows 2000/XP/Vista)</li> <li>·Operation manual</li> <li>·MOS adapter</li> </ul>

Note: SCSI cable and SCSI board (card) are not supplied with the C7557

\*21: This software may be run on Windows 2000/NT/XP with a simple task. For information on how to do this, please consult with our sales office.

### ■ Connection example



\* Shutter, etc. are not available.

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