PS6009

HYBRID - HIGH RELIABILITY DC/DC CONVERTER

FEATURES

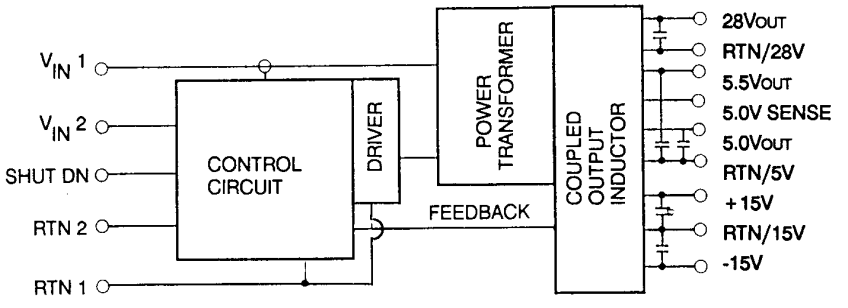
- Continuous short circuit protection with low power dissipation
- Input/output isolation
- 250 kHz current mode switching technology
- Nonlatching overvoltage protection
- 28V, +5V, +15V, -15V output voltages
- External shutdown
- Military screening

DESCRIPTION

The PS6009 is a multiple-output DC/DC converter with 80 watts of power output. It meets or exceeds the requirements of MIL-STD-704D for a 28V DC system voltage transient range. The input voltage range is 14.5V to 50V with a 14.5V minimum start-up voltage. It has very low ripple and noise content on the output and operates with an efficiency rating of 70% minimum. It protects the circuitry by dropping to low power drain during overcurrent short circuit or overvoltage (output) conditions with low power dissipation.

The converter is manufactured with mil spec components to operate reliably under adverse environmental conditions. It is packaged in a 3.50" x 2.42" hermetically sealed case and is only .64" high.

BLOCK DIAGRAM



Capacitors are external, and are shown here for convenience.

External capacitors required

CSR-21 type Ceramic*	
18μF/50V	& 2μF
120μF/10V	& 2μF
120μF/10V	& 2μF
47μF/35V	& 2μF
47μF/35V	& 2μF

* AVX super capacitor SM-5 type or CKR06 X2 (1μF/50V)

SPECIFICATIONS

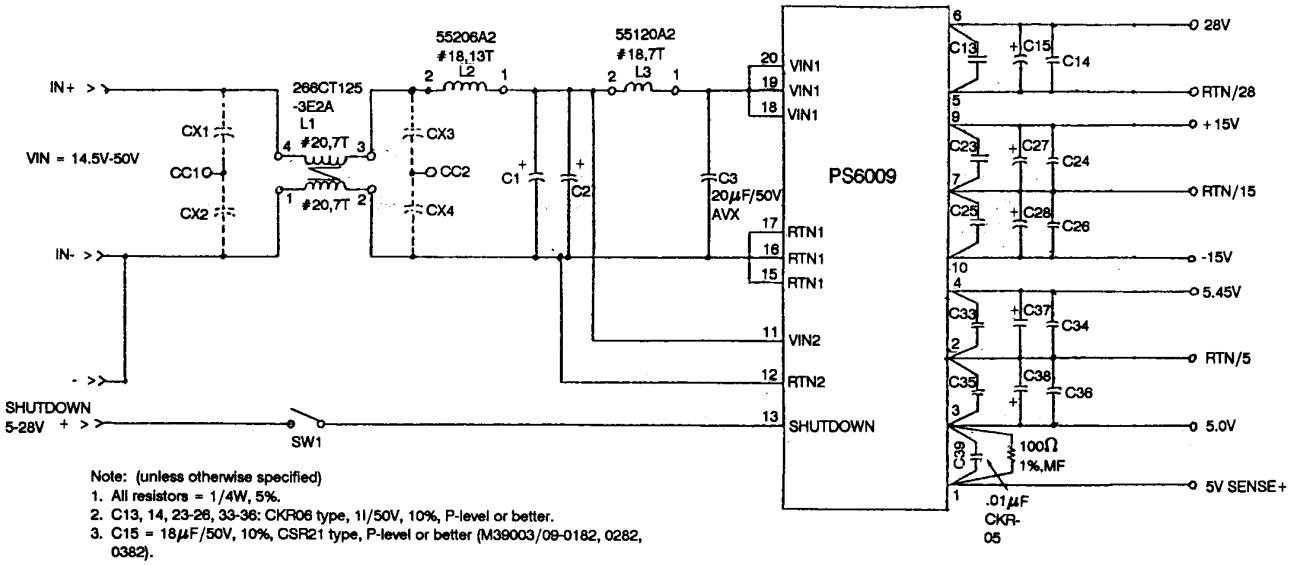
Ta = -55 °C ≤ Te baseplate ≤ 95 °C

ABSOLUTE MAXIMUM RATINGS	Min	Typ	Max	Unit
Thermal Characteristics				
Operating temperature range - Baseplate	-55		+95	°C
Storage temperature range	-55		+125	°C
Soldering Temperature , 10 sec. max.			300	°C
Environmental Considerations				
MTBF 95 °C baseplate AuF (converter only)	50			Khrs
EMI/RFI designed to meet MIL-STD-461, FCC, VDE - *requires use of external filter* See Figure 1.				N/A
Input Characteristics				
Voltage range - operation over this range specified	14.5		50	V
Efficiency - full load @28V	70	75		%
External shutdown	5		28	V
Output Characteristics				
Output voltage accuracy @28V	26.1	27.5	28.9	V
(For load: Full load +5V	4.90	5.0	5.10	V
to 1/5 Full Load +15V	14.5	15.3	16.1	V
-15V	-14.5	-15.3	-16.1	V
Line regulation - Low/high @28V, ±15V		100	150	mV
+5V		20	30	mV
Overvoltage protection set point 5V output	5.7	6	6.3	V
Differential output noise - DC to 20 MHz @28V, ±15V		100	200	mVPP
+5V		40	80	mVPP
Ripple and noise @28V, ±15V		30	60	mV rms
+5V		10	20	mV rms
Output current to maintain rated accuracy: 28V	0.3		1.5	A
+5V	0.6		3	A
±15V	0.15		.75	A
Sense compensation ($5V_{OUT}$ only)	.1	.2		V
+5V line only				
Isolation Characteristics				
Input output isolation voltage @ 10μA			500	VDC
Dynamic Characteristics				
Output transient response (50 to 100%, 1% steady state of the output)			500	μsec
Line transient response - (Δ VI = ±10V, VO 1% steady state)			500	μsec
Turn-on rise time to (VO 1% steady state) at full load on all outputs, 14.5 - 50V			10	msec
Turn-on delay from power ON			80	msec

Weight: 7.6 oz (215g) typical

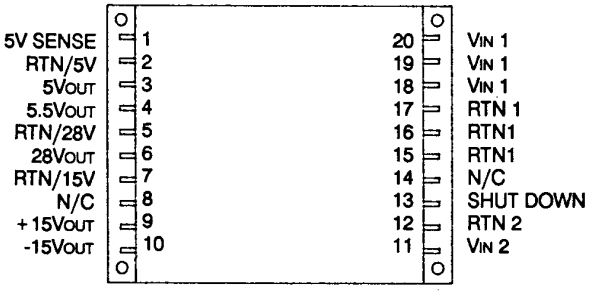
Modifications to these specifications can be accommodated. Consult factory for details.

Figure 2 *Suggested Connection Circuit*

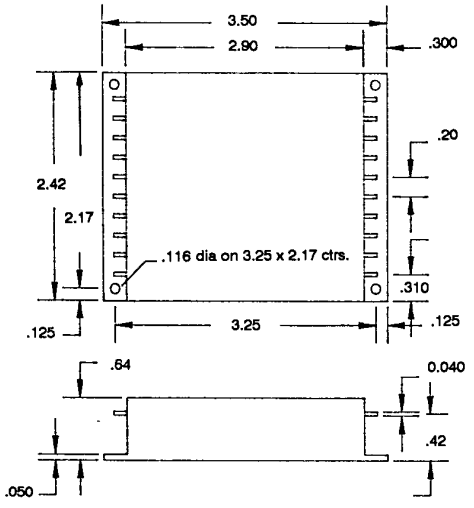


Note: (unless otherwise specified)
1. All resistors = 1/4W, 5%.
2. C13, 14, 23-26, 33-36: CKR06 type, 1l/50V, 10%, P-level or better.
3. C15 = 18µF/50V, 10%, CSR21 type, P-level or better (M39003/09-0182, 0282, 0382).
   C27, 18 = 22µF/35V, 10%, CSR21 type, P-level or better (M39003/09-0155, 0255, 0355).
   C37, 38 = 120µF/10V, 10%, CSR21 type, P-level or better (M39003/09-0117, 0217, 0317).
4. CX1-4 = CKR06 type, TBD.
5. C1, 2 = 33l/75V, 10%, CLR79 type, P-level or better (M39006/22C-0391, 0611, 0831).
6. C3 =20µ/50V, 10%, ceramic, AVX, AOL459.
7. CC1, 2 = Case connection, soldering pads.

Figure 4 *Pin Designation*



MECHANICAL OUTLINE



Pin 1 indicated by black dot on case below pin.

Weight: 215 grams

Figure 5a *Efficiency vs. Load (VIN = 28V)*

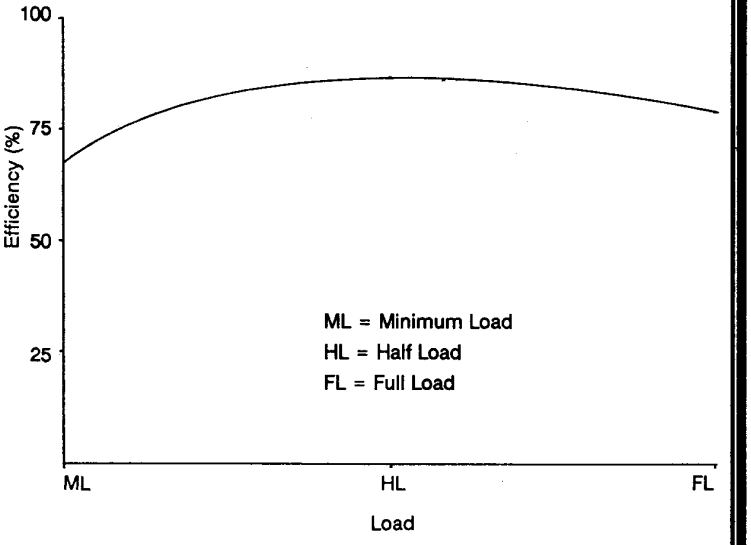


Figure 5b *Efficiency vs. Input Voltage (@Full Load)*

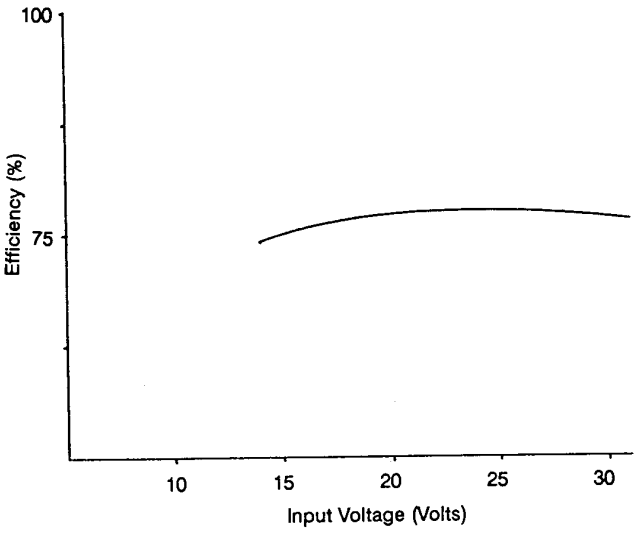


Figure 6 *Power Derating*

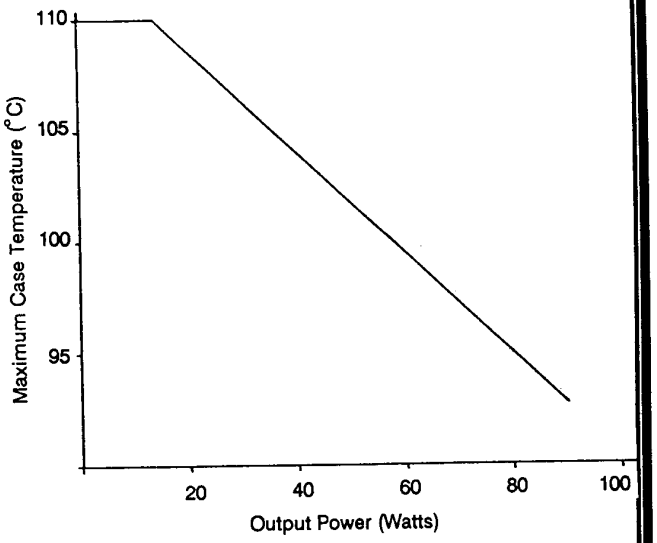
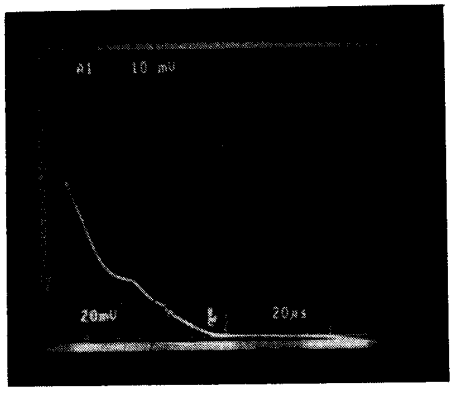
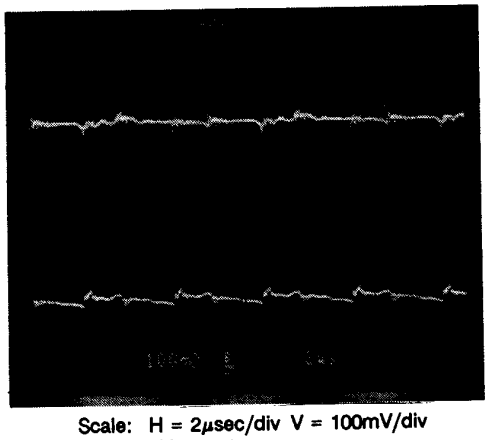


Figure 7 *Inrush Current (with EMI filter)*



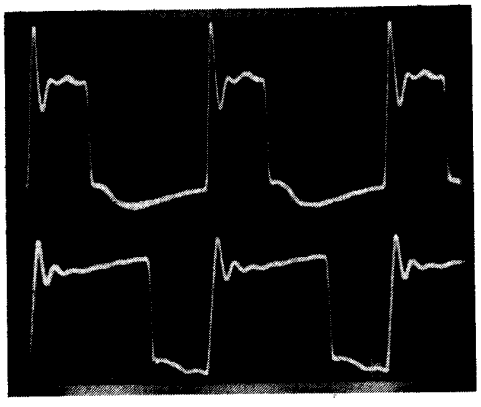
Scale: H = 20μs/div. V = 10A/div

Figure 9 *Output Ripple Waveforms (with worst case loads)*



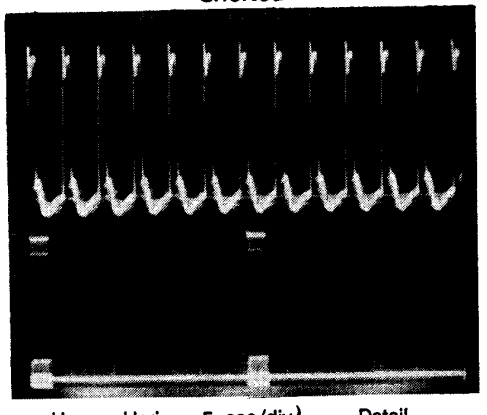
Scale: H = 2μsec/div V = 100mV/div
Upper: 5V output
All outputs @ full load
Lower: +15V output
All outputs @ full load

Figure 10 *Input Current*



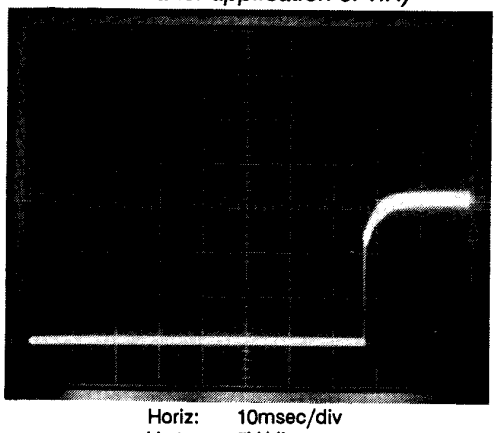
Scale: H = 1μsec/div V = 5A/div
Upper: VIN = 28V
Lower: VIN = 15V

Figure 12 *Input Current with Output Shorted*



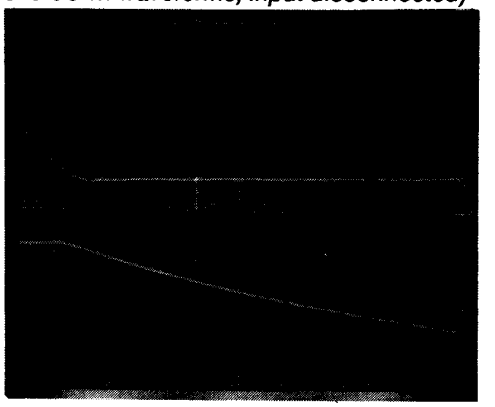
Upper: Horiz = 5μsec/div
Vert = 5A/div
Lower: Horiz = 10msec/div
Vert = 2A/div
Detail during ON pulse

Figure 13 Start Up Waveform
(Start is internally delayed ≈80msec after application of VIN)



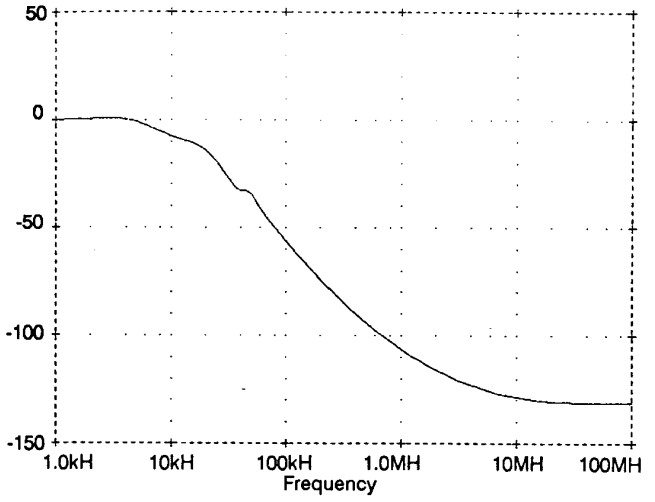
Horiz: 10msec/div
Vert: 5V/div
Startup time +15V output
28V input
Full load on all outputs

Figure 14 Hold Up Time@ Full Load with EMI Filter
(Shutdown waveforms, input disconnected)



Horiz: 100μsec/div
Vert: Upper = 10V/div
Lower = 5V/div
Upper = Input voltage
Lower = +15V output

Figure 15 EMI Filter, Predicted Attenuation



APPLICATION INFORMATION

Evaluation Board

The EB6019 contains all the external components recommended for proper operation and evaluation of the PS6009 DC/DC converter. These are an input EMI filter and necessary output filtering. In addition, there is a shutdown sw for checking shutdown functions, oscilloscope probe sockets allowing realistic measurement of output ripple voltages, and 10mA loads installed on the 28V output to prevent voltage overstress of external 50V output filter capacitors. All features are indicated directly on the printed circuit board.

EMI Filter

The included EMI filter is equivalent to that suggested in Figure 3, but is inadequate to meet category CE03 requirements of MIL-STD-461C. Internal effective resistance of the electrolytic filter capacitor reduces filter Q to minimize interaction with the internal PWM control loop. Fifteen ampere input pulses (250kHz) observed at the unfiltered current loop are, however, reduced to below 2mA at the filtered loop (Figure 8). The ceramic input capacitor is chosen for very low equivalent series resistance (ESR) and equivalent series inductance (ESL) to improve high frequency filter action and to minimize capacitor heating which would otherwise result from the large converter input ripple. Figure 15 indicates calculated attenuation of the EMI filter.

Output Filter Capacitors

Output filtering is a combination of CSR21 type electrolytic and very low ESR and ESL ceramic capacitors selected to maintain low output ripple voltages. Selected capacitor values yield output ripple voltages of 20 and 60 mV(rms) at the switching frequency on the 5V and the ±15V/+28V outputs respectively. The use of lower quality capacitors exhibiting larger ESR or ESL would increase observed output ripple voltages.

Leads connecting the output filter capacitors to the PS6009 terminals are of minimum length to minimize parasitic resistance in the leads which would add to the ESR. Output terminals lead directly from the output filter capacitor for minimum ripple at the load.

Oscilloscope probe sockets are connected directly across the output capacitors to allow accurate measurement of the output ripple voltages. Measurement with conventional probes and ground leads is pessimistically inaccurate because of stray capacitive and inductive pickup on the loop

formed by the probe and ground wire. This effect may be easily demonstrated by connecting the ground lead to the probe tip and observing apparent ripple voltage as the probe is moved near the circuit. Figure 9 shows typical worst case output ripple waveforms for the circuit of Figure 2.

Output filter capacitances are typically determined from allowable output ripple voltage and design inductor ripple current according to the equation

$$C = \Delta I_L / 8 f_s V_o(rms),$$

where the PS6009 design has set f_s = 250kHz and ΔI_L = 0.6A, 0.15A and 0.3A for the 5V, ±15V and 28V outputs respectively.

The maximum allowed capacitor ESR is determined as

$$ESR = V_O(p\text{-}p) / \Delta I_L.$$

Capacitor ESL should be as low as practical as ripple current flowing in the ESL will develop additional output ripple determined as $V_{p\text{-}p} \leq 12 f_s(ESL)$. The factor of 12 depends on the input voltage, but may be as low as 4 for $V_{IN} \approx 20V$.

Protection Features

Four internal systems protect against high output (or input) currents, output short circuits, output undervoltage and output overvoltage. An internal soft start circuit also limits inrush current at start up. There is no input reverse voltage protection with the PS6009. Therefore, a series power diode or fuse and shunt Schottky diode protection is recommended.

Excessive currents are sensed on a pulse-by-pulse basis inherent in the current mode PWM controller, thus terminating each pulse when a predetermined peak current is reached. However, circuit propagation delays could cause excessive internal temperatures under very high current conditions without the additional internal protection.

An internal detection and control circuit forces the converter into a low duty cycle mode in the presence of short circuits on any output, thus protecting the unit from damaging internal heat dissipation (see Figure 12). This protection is effective for load resistances less than ≈0.2Ω, ≈2Ω and ≈4Ω on the 5V, ±15V and 28V outputs respectively. An undervoltage sensing circuit forces the converter into the same low duty cycle mode should the output be forced low or fail to reach normal operating voltage. A sensing circuit triggers an internal SCR to protect against output overvoltage, also activating the low duty cycle mode (see Figure 1).

Because the internal feedback loop derives its control voltage from a winding on the coupled inductor output filter, no or light load conditions cause increased voltages at the 5.4V, ±15V and +28V terminals. An internal SCR crowbars the output, forcing the converter to shut down and restart. Should the no load condition persist, internal control circuits force an approximate 5msec restart attempt every 45msec. During restart, peak voltages (observed by oscilloscope) at the 5.4V, ±15V and the 28V terminals will be ≈6.3V, ≈17V and ≈31V respectively.

With only the 5V output loaded (no minimum load on the ±15V or +28V outputs), the ±15V and the 28V outputs would rise to ≈2.5 and 4.5 times V_{IN}.

Output Regulation & Voltage Sensing

The isolated ±15V and 28V outputs are regulated to within ±5% by the feedback control loop so long as minimum load restrictions are observed. The 5V output is, additionally, series regulated to within ≈±1%; and an external positive sense line is provided. The 5V return line should be of low resistance as there is no negative sense line provided. The sense line length should be limited to about 8 inches, else stray line capacitance may cause control loop instability. The range of voltage correction is limited by the ≈5.5V input voltage to the series regulator and varies with temperature.

The greatest correction is available at low temperature and the least at high temperature. Load current carrying output lines and connections should be of lowest practical resistance depending upon the full load operating currents. Approximately 200mV of correction is available at T_C = 25°C and 3A load; this decreases to ≈100mV at 95°C/full load and increases as load current is decreased.

Minimum Load Currents

As load currents are decreased below specified limits, output inductor current becomes discontinuous and output ripple voltages increase. However, one load current may be decreased below limits if another is increased. The +15V current may drop below limits if the -15V current is increased equally or the ±15V currents may both be decreased if the 5V current is increased five times the 15V decrease (2.5 times if only one 15V current is decreased). Ripple voltages may exceed specification under such conditions. Do not decrease the ±15V or 28V load currents below about 10mA (provided only on the 28V output by the PWM mounted 6kΩ resistors) else the 50V filter capacitors may be overstressed.

Start Up

Internal circuitry delays start up by about 60msec after application of input power. After this delay, the output rise time to with 2% of final voltage is typically 2 to 2.5msec under full load conditions (see Figure 13). Should the output voltage fail to reach 80% of rated output with ≈8msec after the initial delay, the circuit will be forced into a 10% restart attempt duty cycle.

Start up pulse current is internally limited to ≈18A peak at the switching frequency while transient currents of less than 50nsec duration are not limited. To limit input peak voltage due to switching of inductive feed lines, a low ESR input capacitor of 20μF should be placed very near the input terminals. Figure 8 shows a predicted ≈90A peak input current (for a 20μF capacitor, a dynamic source resistance of 300mΩ and an input step of 28V) when no additional inrush current limiting is applied. Very few capacitors are designed to survive such a peak current pulse on a recurring basis. Figure 7 shows that inrush current is limited to ≈40A for the same input conditions when the suggested EMI filter is used. Input currents may be scaled directly for higher or lower input step voltages, whether using the simple input capacitor or the EMI filter. In those applications where start up current peaks must be limited, some additional form of input dv/dt control must be provided.

Hold Up

The PS6009 will continue to supply power for a finite time after removal of the input power. Figure 14 shows that the hold up time is about 20μsec after the input voltage drops to 11V. This time is increased when an input capacitor or EMI filter is attached, the additional time is dependent on the storage capacity of the filter components.

Heat Sinks

The PS6009 rated internal temperature will be exceeded when operating at room temperature and maximum load without a heat sink. The PS6009 should be attached to a heat sink surface if operating at greater than 30% rated load at an ambient temperature exceeding 30°C. In fixing to a heat sink surface, it is important not to stress or distort the case. It is recommended that a flexible thermal blanket, such as Ablestik #12-1-0102, be placed between the PS6009 and the heat sink surface.

1. Preliminary data.
2. Ablestik Laboratories, 833 West 182nd Street, Gardena, CA 92048.

MIL-STD-1772 Qualified

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