MC14018B

Presettable Divide-By-N Counter

The MC14018B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic 1 on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic 1 on the reset input will cause all $\overline{Q}$ outputs to go to a logic 1 state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti−lock gating is included in the MC14018B to assure proper counting sequence.

Features

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4018B
- Pb−Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	− 0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
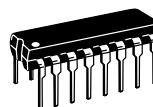
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
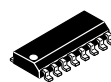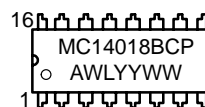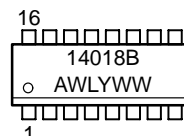
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MARKING DIAGRAMS

PDIP−16
P SUFFIX
CASE 648

16
MC14018BCP
○ AWLYYWW
1

SOIC−16
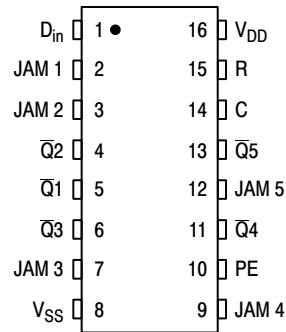D SUFFIX
CASE 751B

16
14018B
○ AWLYWW
1

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14018B

PIN ASSIGNMENT

D_{in}	1 ●		16	V_{DD}
JAM 1	2		15	R
JAM 2	3		14	C
$\overline{Q2}$	4		13	$\overline{Q5}$
$\overline{Q1}$	5		12	JAM 5
$\overline{Q3}$	6		11	$\overline{Q4}$
JAM 3	7		10	PE
V_{SS}	8		9	JAM 4

FUNCTIONAL TRUTH TABLE

Clock	Reset	Preset Enable	Jam Input	$\overline{Q}n$
⌐_	0	0	X	$\overline{Q}n$
_/⎺	0	0	X	$\overline{D}_n$*
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

*D_n is the Data input for that stage. Stage 1
has Data brought out to Pin 1.

ORDERING INFORMATION

Device	Package	Shipping†
MC14018BCP	PDIP–16	500 Units / Rail
MC14018BCPG	PDIP–16 (Pb–Free)	500 Units / Rail
MC14018BD	SOIC–16	48 Units / Rail
MC14018BDG	SOIC–16 (Pb–Free)	48 Units / Rail
MC14018BDR2	SOIC–16	2500 Units / Tape & Reel
MC14018BDR2G	SOIC–16 (Pb–Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging
 Specifications Brochure, BRD8011/D.

MC14018B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0		V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
$V_{in} = 0$ or V_{DD} "1" Level		V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
			10	9.95	—	9.95	10	—	9.95	—	
			15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)		V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
			10	—	3.0	—	4.50	3.0	—	3.0	
			15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)		V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)		I_{OH}	5.0	– 3.0	—	– 2.4	– 4.2	—	– 1.7	—	mAdc
			5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	
			10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
			15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)		I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0 10 15	I_T = (0.3 μA/kHz) f + I_{DD} I_T = (0.7 μA/kHz) f + I_{DD} I_T = (1.0 μA/kHz) f + I_{DD}							μAdc

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ (Note 6)	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.35 ns/pF) C_L + 32 ns t_{TLH}, t_{THL} = (0.6 ns/pF) C_L + 20 ns t_{TLH}, t_{THL} = (0.4 ns/pF) C_L + 20 ns	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to $\overline{Q}$ t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 265 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 102 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 72 ns	t_{PLH}, t_{PHL}	5.0 10 15	— — —	310 120 85	620 240 170	ns
Reset to $\overline{Q}$ t_{PLH} = (0.90 ns/pF) C_L + 325 ns t_{PLH} = (0.36 ns/pF) C_L + 132 ns t_{PLH} = (0.26 ns/pF) C_L + 81 ns		5.0 10 15	— — —	370 150 100	740 300 200	ns
Preset Enable to $\overline{Q}$ t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 325 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 81 ns		5.0 10 15	— — —	370 150 100	740 300 200	ns
Setup Time Data (Pin 1) to Clock Jam Inputs to Preset Enable	t_{su}	5.0 10 15 5.0 10 15	200 100 80 200 100 80	0 0 0 0 0 0	— — — — — —	ns ns
Data (Jam Inputs)–to–Preset Enable Hold Time	t_h	5.0 10 15	540 500 480	270 250 240	— — —	ns
Clock Pulse Width	t_{WH}	5.0 10 15	400 200 160	200 100 80	— — —	ns
Reset or Preset Enable Pulse Width	t_{WH}	5.0 10 15	290 130 110	145 65 55	— — —	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15		No Limit		ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 6.5 8.0	1.25 3.25 4.0	MHz

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
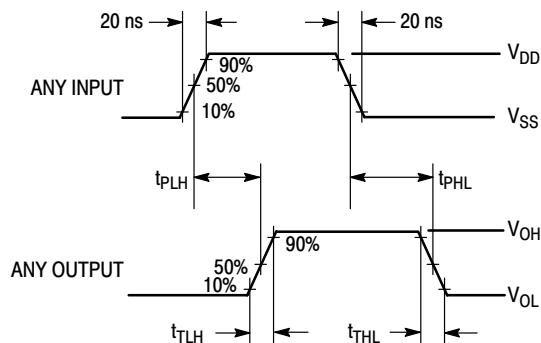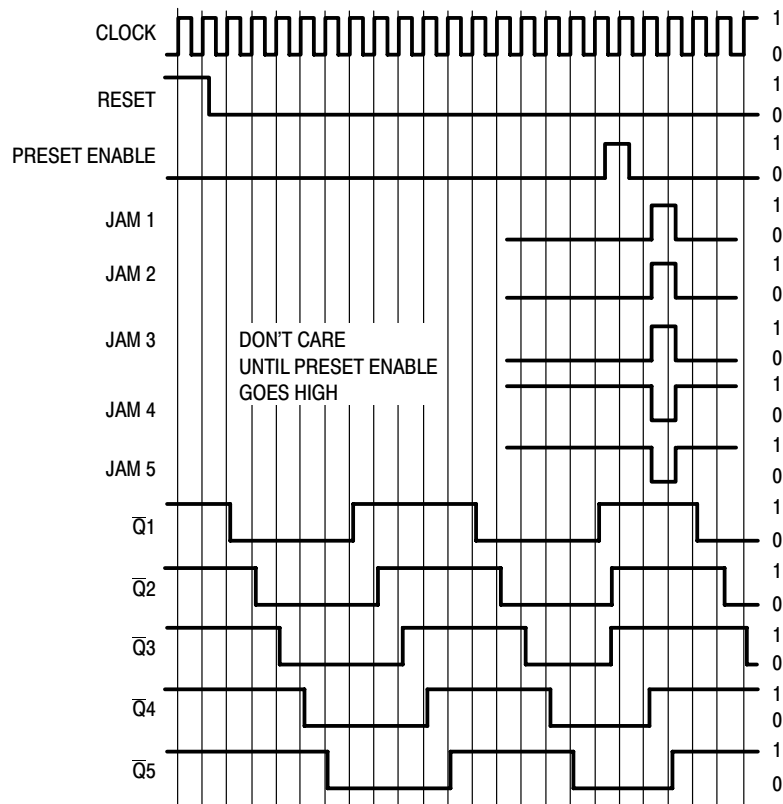
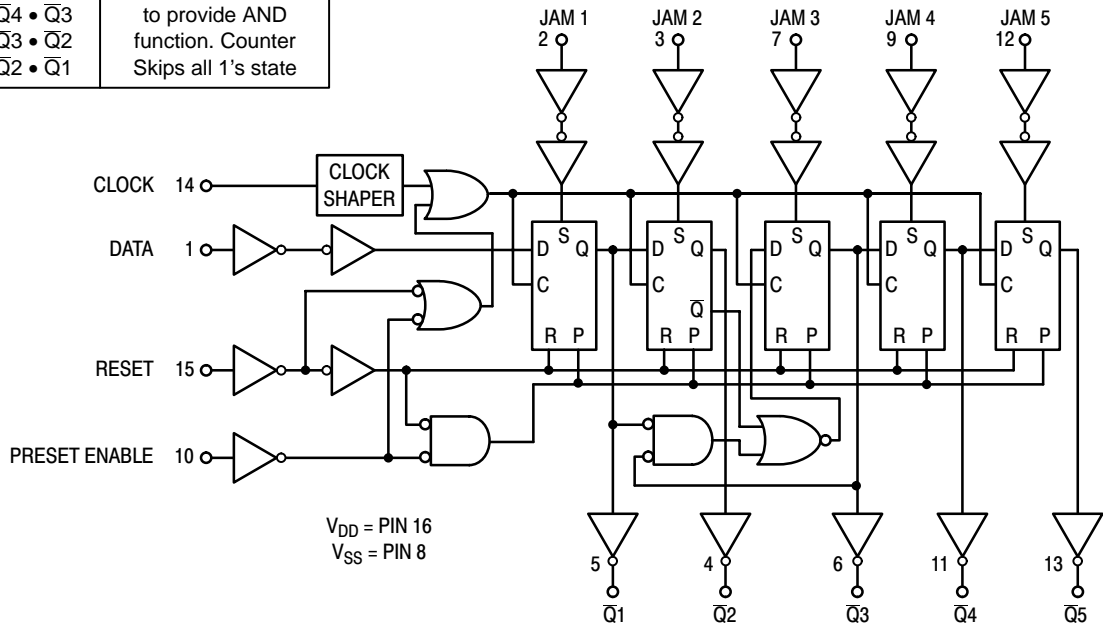

Figure 1. Switching Time Waveforms

MC14018B

TIMING DIAGRAM
($\overline{Q}$5 Connected to Data Input)

CLOCK
RESET
PRESET ENABLE
JAM 1
JAM 2
JAM 3
JAM 4
JAM 5
$\overline{Q}$1
$\overline{Q}$2
$\overline{Q}$3
$\overline{Q}$4
$\overline{Q}$5

DON'T CARE
UNTIL PRESET ENABLE
GOES HIGH

FUNCTION SELECTION

Counter Mode	Connect Data Input (Pin 1) to:	Comments
Divide by 10	$\overline{Q}$5	
Divide by 8	$\overline{Q}$4	No external
Divide by 6	$\overline{Q}$3	components needed.
Divide by 4	$\overline{Q}$2	
Divide by 2	$\overline{Q}$1	
Divide by 9	$\overline{Q}$5 • $\overline{Q}$4	Gate package needed
Divide by 7	$\overline{Q}$4 • $\overline{Q}$3	to provide AND
Divide by 5	$\overline{Q}$3 • $\overline{Q}$2	function. Counter
Divide by 3	$\overline{Q}$2 • $\overline{Q}$1	Skips all 1's state

LOGIC DIAGRAM

JAM 1 2
JAM 2 3
JAM 3 7
JAM 4 9
JAM 5 12

CLOCK 14
CLOCK SHAPER
DATA 1
RESET 15
PRESET ENABLE 10

V_{DD} = PIN 16
V_{SS} = PIN 8

D S Q
C
$\overline{Q}$
R P

5 $\overline{Q}$1
4 $\overline{Q}$2
6 $\overline{Q}$3
11 $\overline{Q}$4
13 $\overline{Q}$5

MC14018B

PACKAGE DIMENSIONS

PDIP−16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648−08
ISSUE T
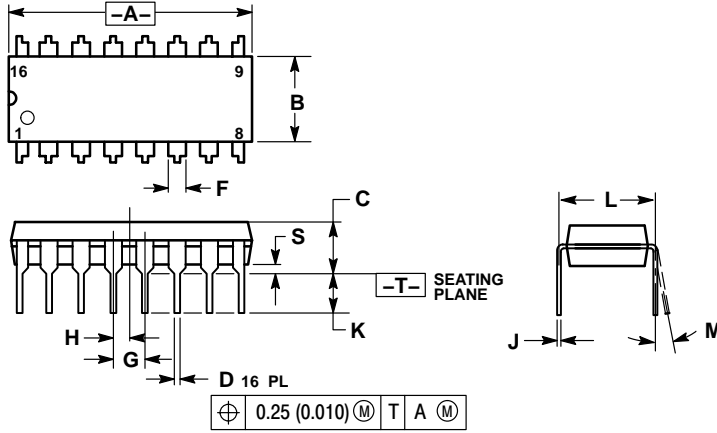
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

MC14018B

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B−05
ISSUE J
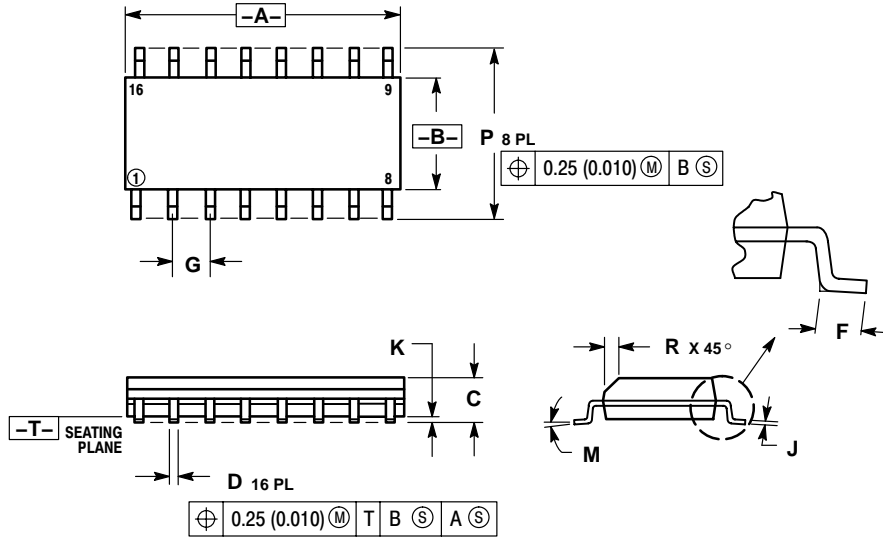
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019