

HM514102B/BL Series

4,194,304-word × 1-bit Dynamic RAM

The Hitachi HM514102B/BL is a CMOS dynamic RAM organized 4,194,304-word × 1-bit. HM514102B/BL has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514102B/BL offers static column mode as a high speed access mode.

Multiplexed address input permits the HM514102B/BL to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Ordering Information

Type No.	Access time	Package
HM514102BS/BLS-7	70 ns	300-mil, 20-pin plastic SOJ (CP-20D)
HM514102BS/BLS-8	80 ns	
HM514102BZ/BLZ-7	70 ns	400-mil, 20-pin plastic ZIP (ZP-20)
HM514102BZ/BLZ-8	80 ns	

Features

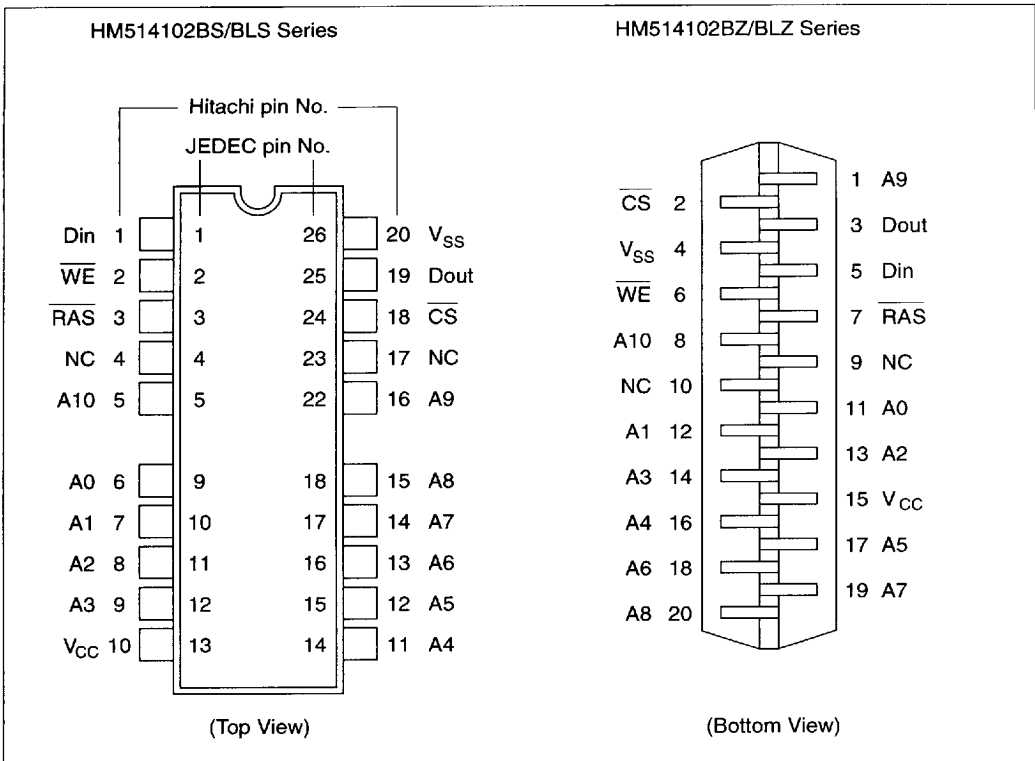
- Single 5 V (±10%)
- High speed
 - Access time
70 ns/80 ns (max)
- Low power dissipation
 - Active mode
550 mW/495 mW (max)
 - Standby mode 11 mW (max)
0.55 mW (L-version)
- Static column mode capability
- 1,024 refresh cycles: 16 ms
1,024 refresh cycles: 128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- Test function
- Battery back up operation (L-version)

■ 4496203 0026261 T04 ■

Hitachi 63

HM514102B/BL Series

Pin Arrangement

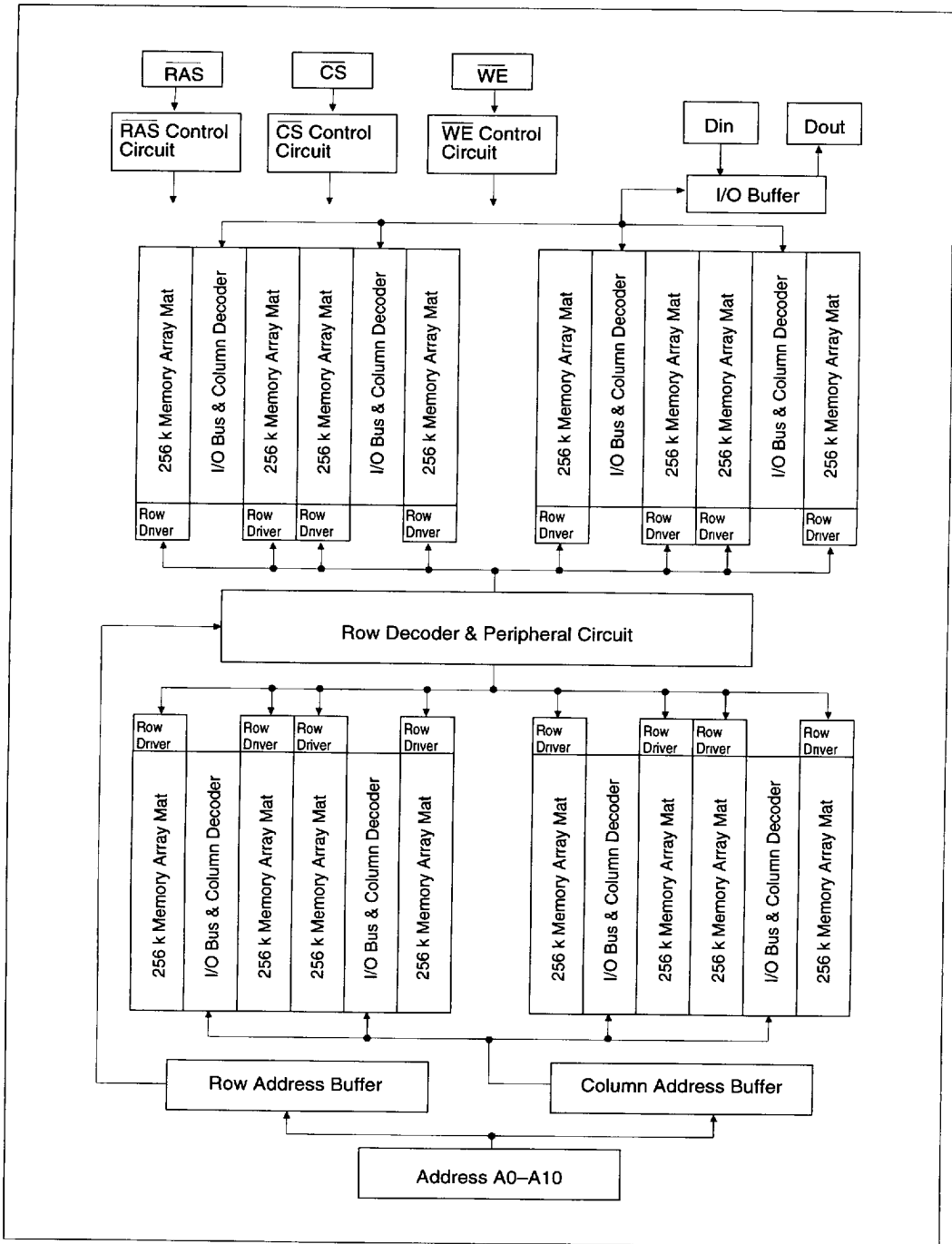


Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
Din	Data-in
Dout	Data-out
RAS	Row address strobe

Pin name	Function
CS	Chip select
WE	Read/write enable
VCC	Power (+5 V)
VSS	Ground
NC	No connection

Block Diagram



■ 4496203 0026263 887 ■

Hitachi 65

HM514102B/BL Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	HM514102 B/BL-7		HM514102 B/BL-8		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I _{CC1}	—	100	—	90	mA	\overline{RAS} , \overline{CS} cycling t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface \overline{RAS} , $\overline{CS} = V_{IH}$ Dout = High-Z	
		—	1	—	1	mA	CMOS interface \overline{RAS} , $\overline{CS} \geq V_{CC} - 0.2 V$ Dout = High-Z	
Standby current (L-version)		—	100	—	100	μA	CMOS interface, \overline{RAS} , $\overline{CS} = V_{IH}$ \overline{WE} , address, Din = V _{IH} or V _{IL} Dout = High-Z	5
\overline{RAS} -only refresh current	I _{CC3}	—	100	—	90	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	—	5	mA	$\overline{RAS} = V_{IH}$, $\overline{CS} = V_{IL}$ Dout = enable	1
\overline{CS} -before- \overline{RAS} refresh current	I _{CC6}	—	100	—	90	mA	t _{RC} = min	
Static column mode current	I _{CC9}	—	100	—	90	mA	t _{SC} = min	1, 3, 4
Battery back up operation current (Standby with CBR refresh) (L-version)	I _{CC10}	—	200	—	200	μA	t _{RC} = 125 μs, t _{RAS} ≤ 1 μs $\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$ Address, Din = V _{IH} or V _{IL} Dout = High-Z	5
Input leakage current	I _{LI}	-10	10	-10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I _{LO}	-10	10	-10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. ICC depends on output load condition when the device is selected. ICC max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CS} = V_{IH}$.
 4. Invalid address is prohibited during static column cycle.
 5. $V_{CC} - 0.2 V \leq V_{IH} \leq 6.5 V$, $0 V \leq V_{IL} \leq 0.2 V$

■ 4496203 0026265 65T ■

HM514102B/BL Series

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address, data-in)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CS} = V_{IH}$ to disable Dout

AC Characteristics ($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *17, *18

Test Conditions

Input rise and fall times: 5 ns

Input timing reference levels: 0.8 V, 2.4 V

Output load: 2 TTL gate + C_L (100 pF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
\overline{RAS} precharge time	t_{RP}	50	—	60	—	ns	
\overline{RAS} pulse width	t_{RAS}	70	10000	80	10000	ns	21
\overline{CS} pulse width	t_{SP}	20	10000	20	10000	ns	22
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	ns	
Column address hold time	t_{AHW}	15	—	15	—	ns	
\overline{RAS} to \overline{CS} delay time	t_{RCD}	20	50	20	60	ns	8
\overline{RAS} to column address delay time	t_{RAD}	15	35	15	40	ns	9
\overline{RAS} hold time	t_{RSH}	20	—	20	—	ns	

HM514102B/BL Series

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)(cont)

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
\overline{CS} hold time	t_{CSH}	70	—	80	—	ns	
\overline{CS} to \overline{RAS} precharge time	t_{SRS}	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Access time from \overline{RAS}	t_{RAC}	—	70	—	80	ns	2, 3, 19
Access time from \overline{CS}	t_{ACS}	—	20	—	20	ns	3, 4, 19
Access time from address	t_{AA}	—	35	—	40	ns	3, 5, 14, 19
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to \overline{CS}	t_{RCH}	0	—	0	—	ns	20
Read command hold time to \overline{RAS}	t_{RRH}	0	—	0	—	ns	20
Column address to \overline{RAS} lead time	t_{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	20	ns	6
\overline{RAS} to column address hold time	t_{AHR}	15	—	15	—	ns	16
Output hold time from address	t_{AOH}	5	—	5	—	ns	
Column address hold time to \overline{RAS} on read	t_{AR}	70	—	80	—	ns	

■ 4496203 0026267 422 ■

Hitachi 69

HM514102B/BL Series

Write Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	—	0	—	ns	10
Write command hold time	t _{WCH}	15	—	15	—	ns	
Write command hold time to $\overline{\text{RAS}}$	t _{WCR}	65	—	70	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	20	—	20	—	ns	
Write command to $\overline{\text{CS}}$ lead time	t _{CWL}	20	—	20	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	11
Data-in hold time	t _{DH}	15	—	15	—	ns	11
Data in hold time to $\overline{\text{RAS}}$	t _{DHR}	65	—	70	—	ns	
Column address hold time to $\overline{\text{RAS}}$ on write	t _{AWR}	65	—	70	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	155	—	175	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	70	—	80	—	ns	10
$\overline{\text{CS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	20	—	20	—	ns	10
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	35	—	40	—	ns	10
Output hold time from $\overline{\text{WE}}$	t _{WOH}	0	—	0	—	ns	

Refresh Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
$\overline{\text{CS}}$ setup time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{\text{CS}}$ hold time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CS}}$ hold time	t_{ZRH}	10	—	10	—	ns	
$\overline{\text{CS}}$ precharge time in normal mode	t_{SIN}	10	—	10	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Static column mode cycle time	t_{SC}	40	—	45	—	ns	
Static column mode $\overline{\text{RAS}}$ pulse width	t_{RASC}	—	100000	—	100000	ns	
$\overline{\text{RAS}}$ to second $\overline{\text{WE}}$ delay time	t_{RSWD}	70	—	80	—	ns	
Static column mode $\overline{\text{CS}}$ precharge time	t_{SI}	10	—	10	—	ns	
Write invalid time	t_{WI}	10	—	10	—	ns	

HM514102B/BL Series

Static Column Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Static column mode cycle time on read-modify-write	t_{SRW}	75	—	85	—	ns	12
Access time from previous \overline{WE}	t_{ALW}	—	70	—	80	ns	3, 13, 19
Previous \overline{WE} to column address delay time	t_{LWAD}	20	35	20	40	ns	15
Column address hold time to previous \overline{WE}	t_{AHLW}	70	—	80	—	ns	
Output enable time from \overline{WE}	t_{OW}	—	25	—	25	ns	19

Test Mode Cycle

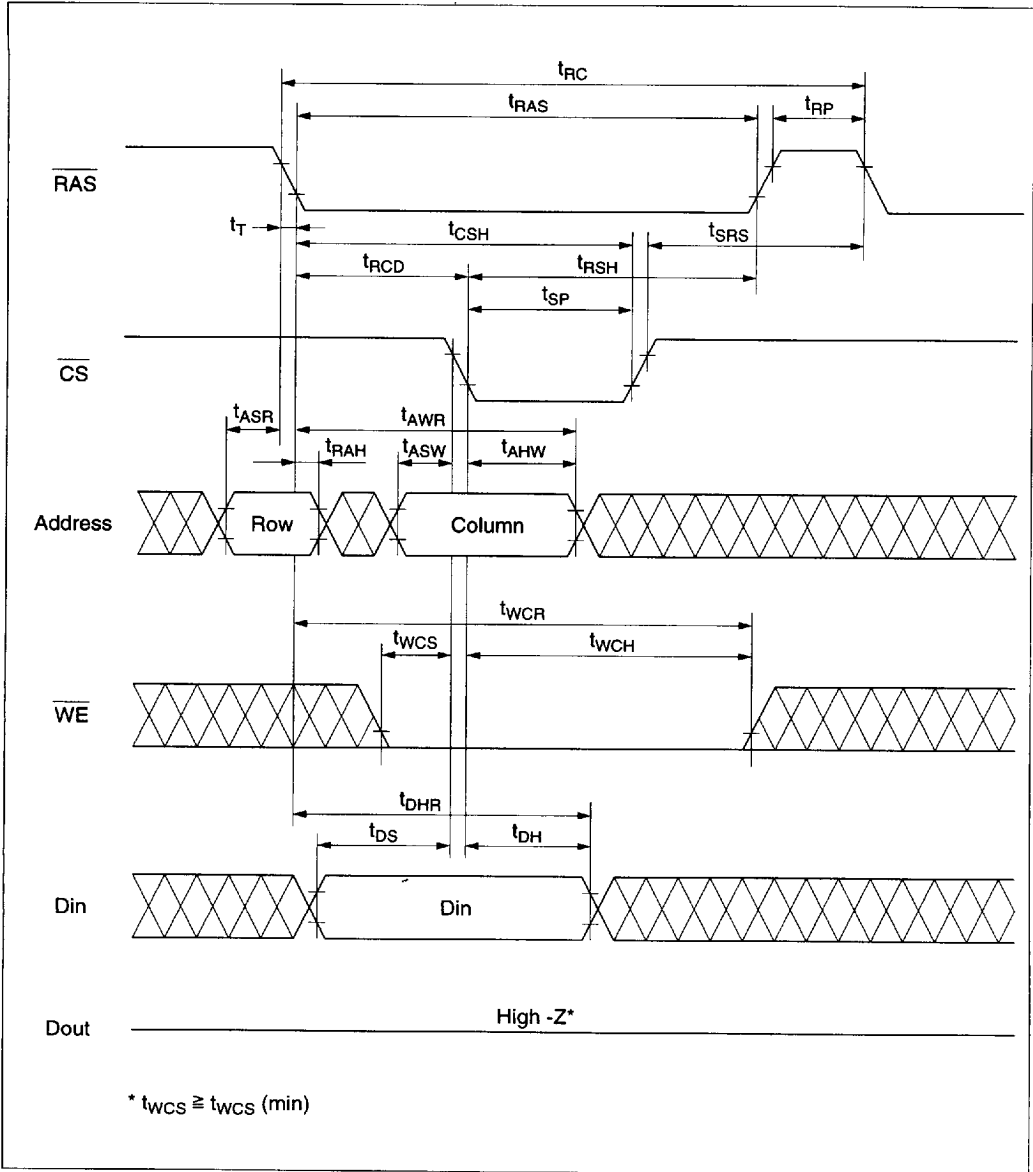
Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
Test mode \overline{WE} setup time	t_{WS}	0	—	0	—	ns	
Test mode \overline{WE} hold time	t_{WH}	10	—	10	—	ns	

Counter Test Cycle

Parameter	Symbol	HM514102B/BL-7		HM514102B/BL-8		Unit	Notes
		Min	Max	Min	Max		
CAS precharge time in counter test cycle	t_{SIT}	40	—	40	—	ns	

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{ACS} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to \overline{CS} leading edge in an early write cycle and to \overline{WE} leading edge in a delayed write or a read-modify-write cycle.
 12. $t_{SRW}(\text{min}) = t_{AWD}(\text{min}) + t_{LWAD}(\text{max}) + t_T$
 13. Assumes that $t_{LWAD} \leq t_{LWAD}(\text{max})$. If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
 14. Assumes that $t_{LWAD} \geq t_{LWAD}(\text{max})$.
 15. Operation with the $t_{LWAD}(\text{max})$ limit insures that $t_{ALW}(\text{max})$ can be met, $t_{LWAD}(\text{max})$ is specified as a reference point only, if t_{LWAD} is greater than the specified $t_{LWAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 16. t_{AHR} defines the time at which the column address hold.
 17. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (\overline{RAS} -only refresh cycle or \overline{CS} -before- \overline{RAS} refresh cycle). If the internal refresh counter is used, a minimum of eight \overline{CS} -before- \overline{RAS} refresh cycles is required.
 18. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – RA10, CA10 and CA0. This test mode operation can be performed by \overline{WE} -and- \overline{CS} -before- \overline{RAS} (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a \overline{RAS} -only refresh cycle or a \overline{CS} -before- \overline{RAS} refresh cycle.
 19. In a test mode read cycle, the value of t_{RAC} , t_{ACS} , t_{AA} , t_{OW} and t_{ALW} are delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
 20. Either t_{RCH} or t_{RRH} must be satisfied.
 21. $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle.
 22. $t_{SP}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write

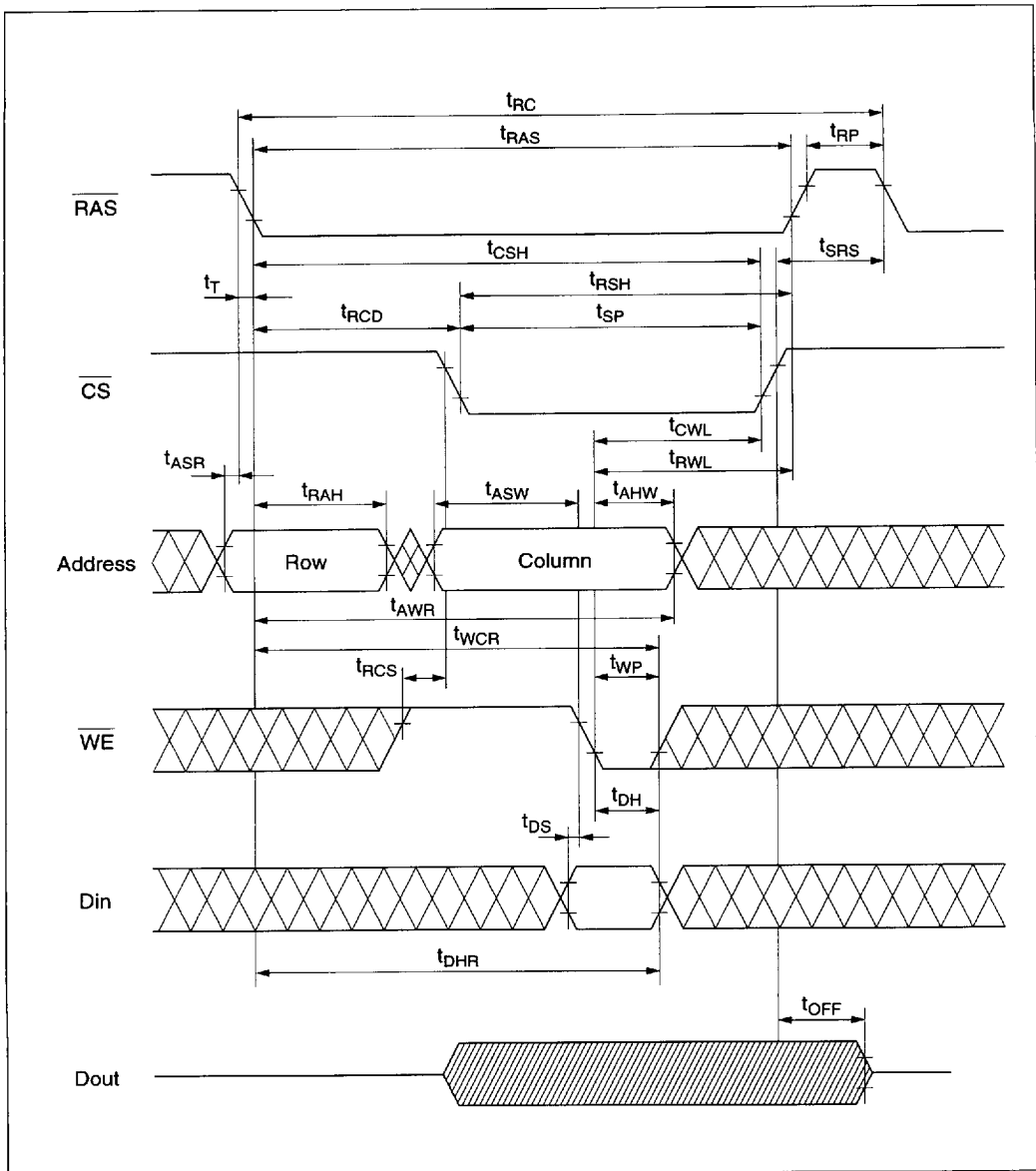
Early Write Cycle



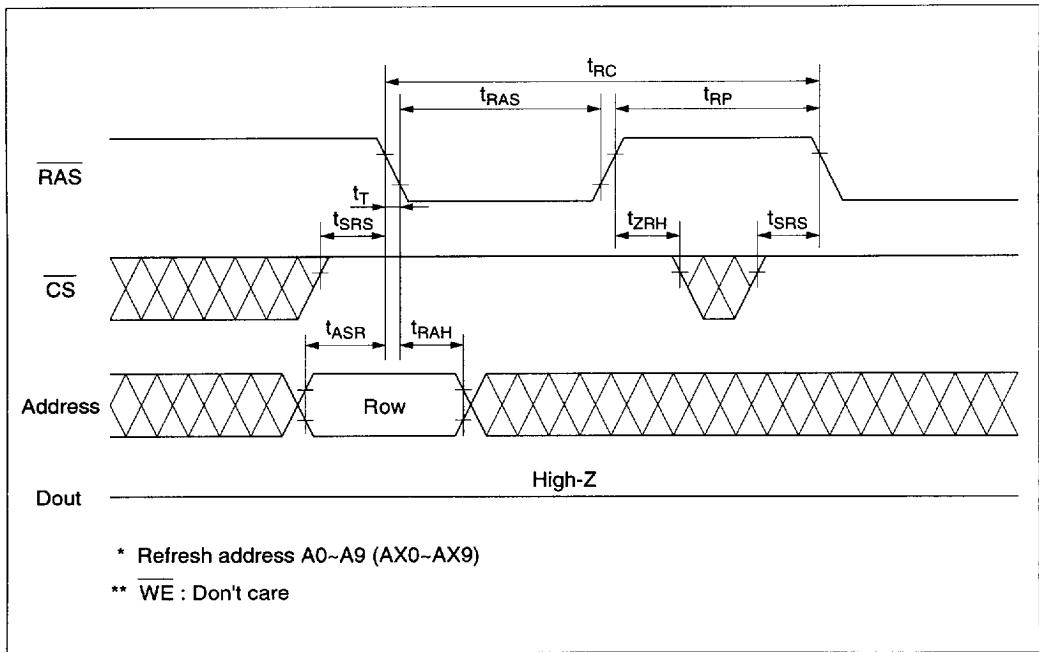
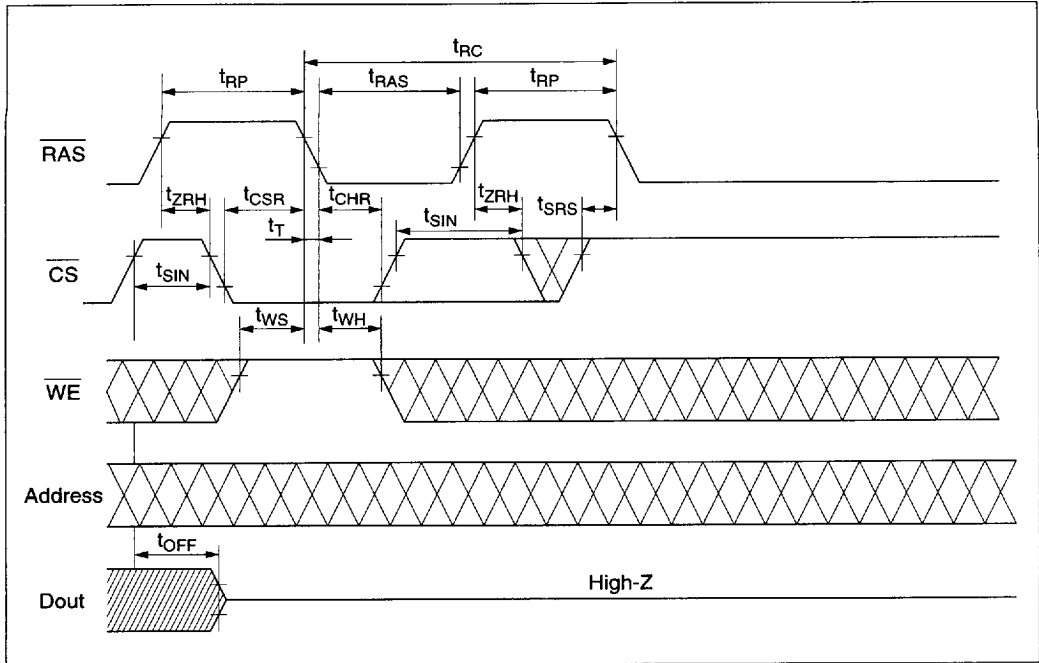
4496203 0026273 726

HM514102B/BL Series

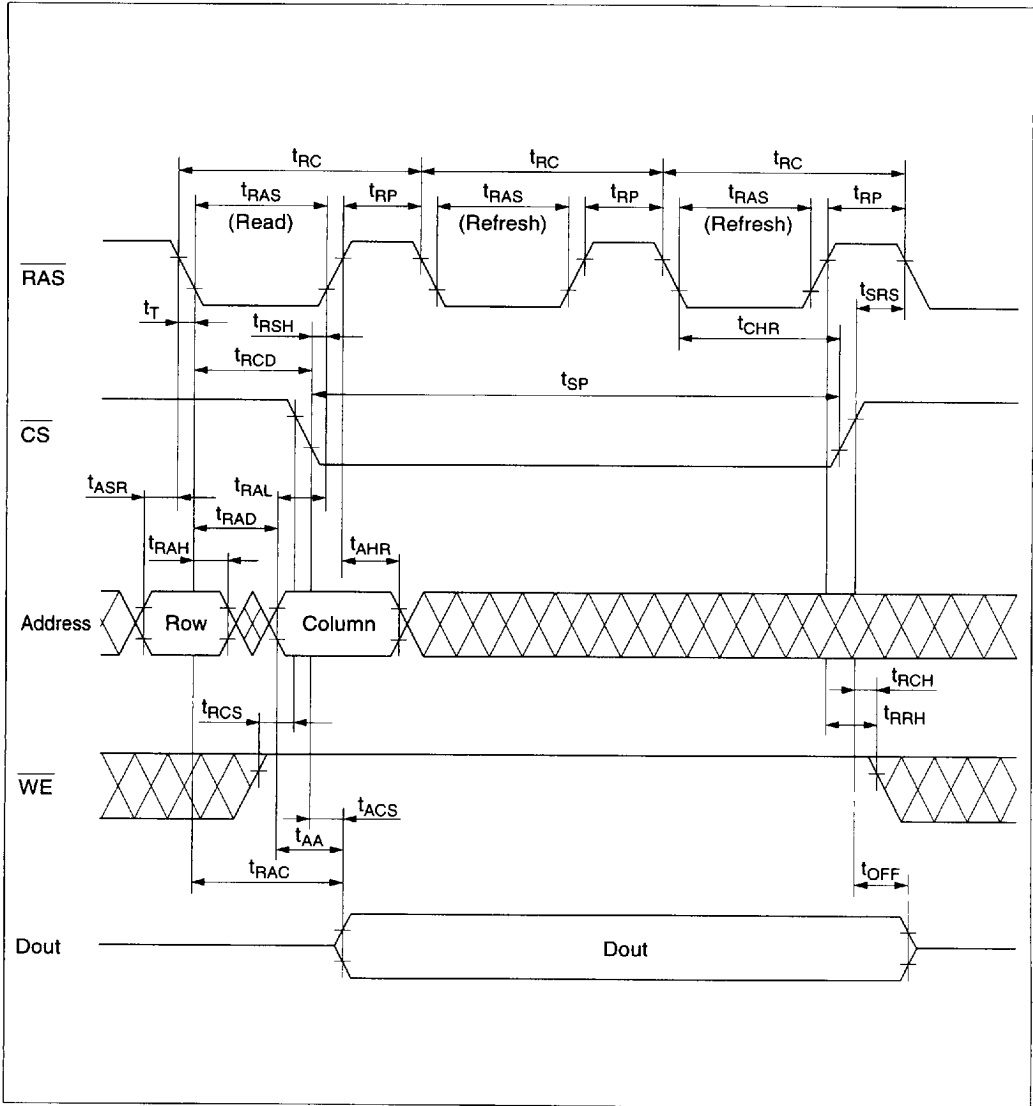
Delayed Write Cycle



HM514102B/BL Series

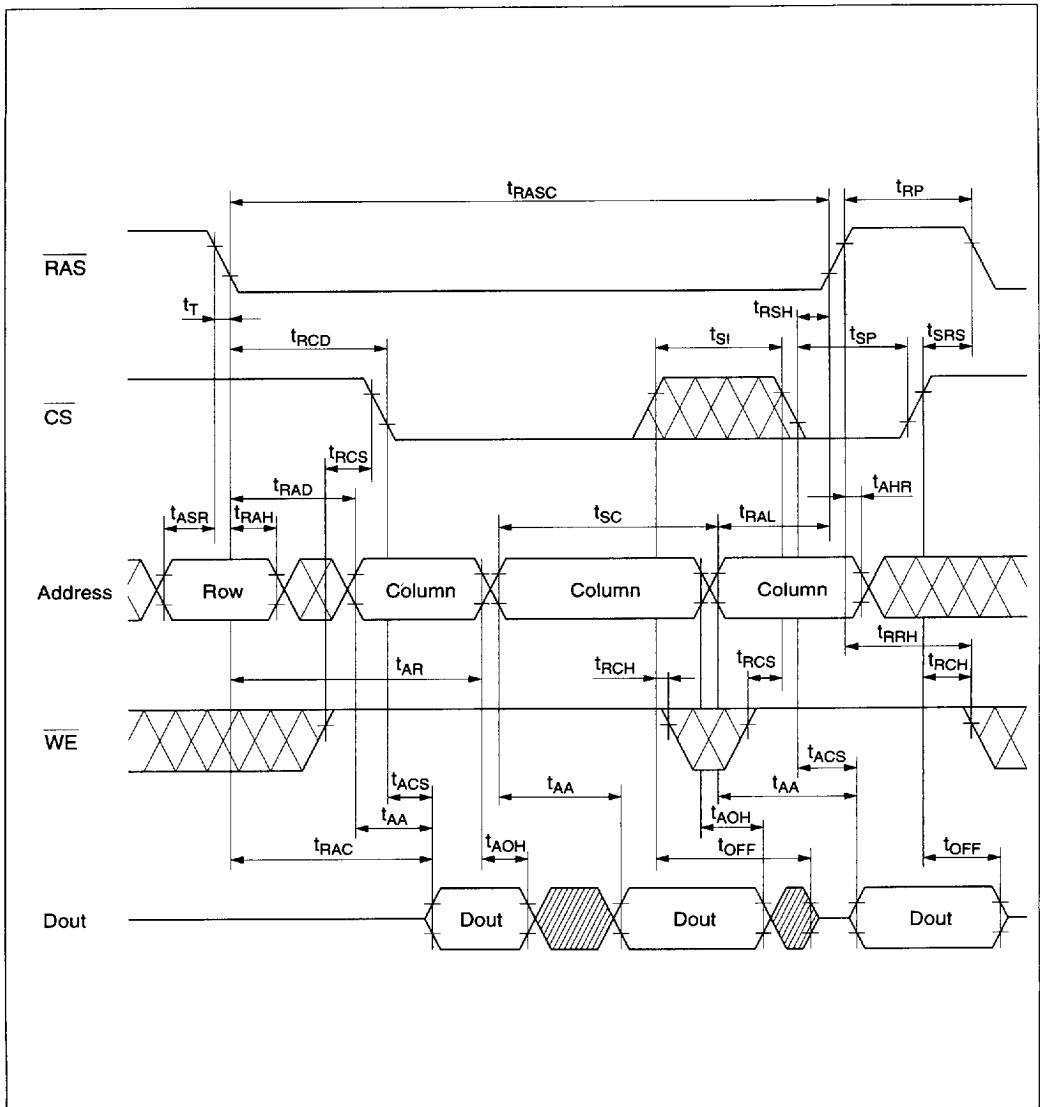


Hidden Refresh Cycle

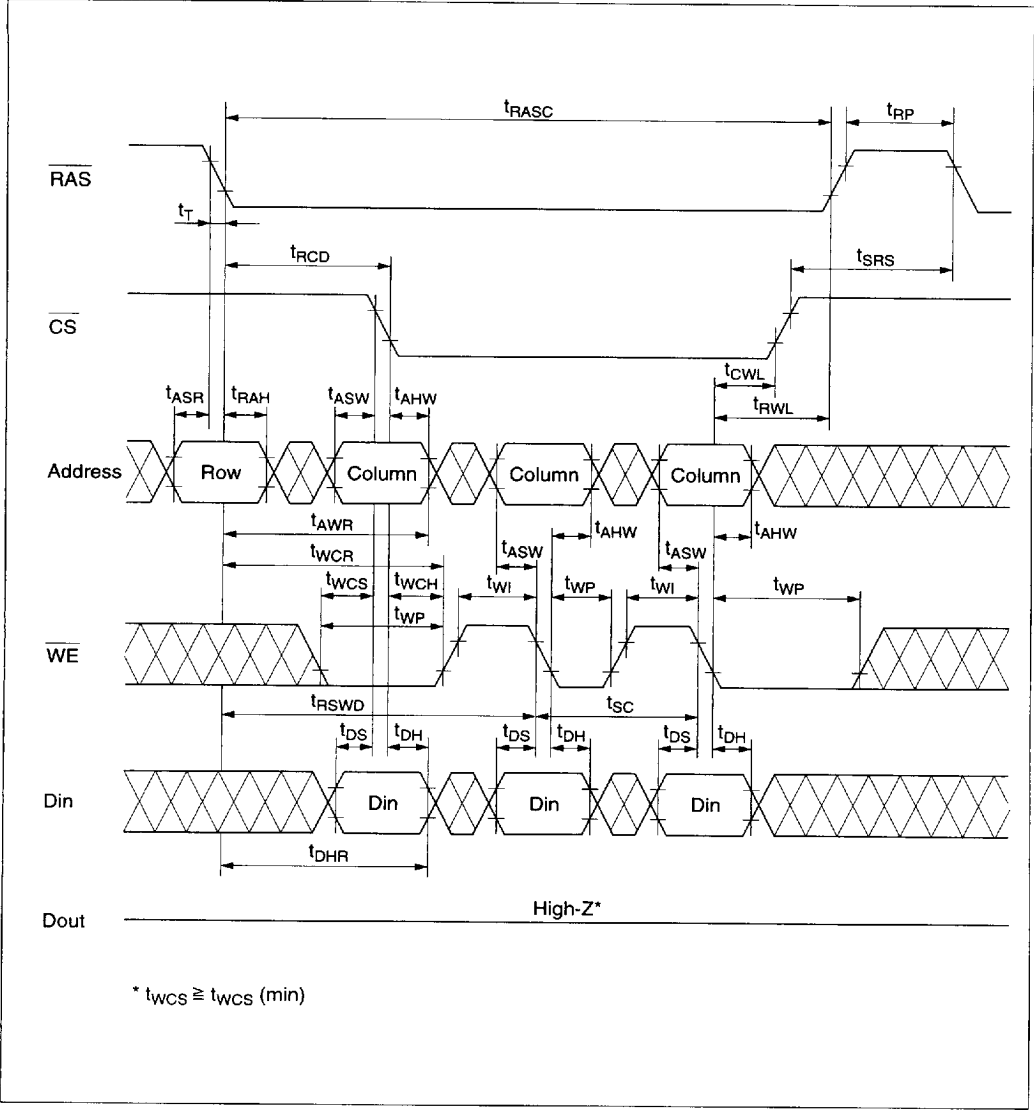


HM514102B/BL Series

Static Column Mode Read Cycle

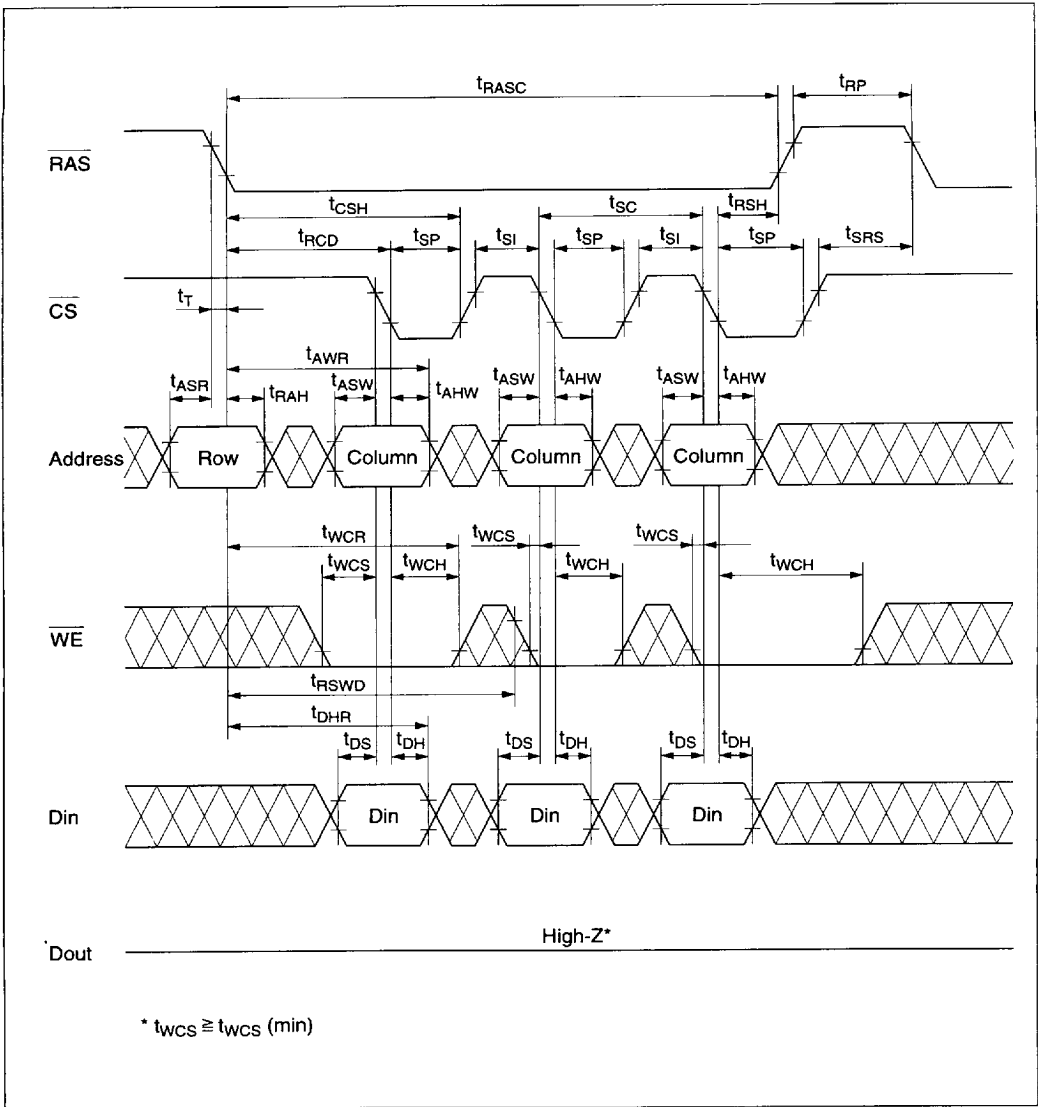


Static Column Mode Write Cycle (1)

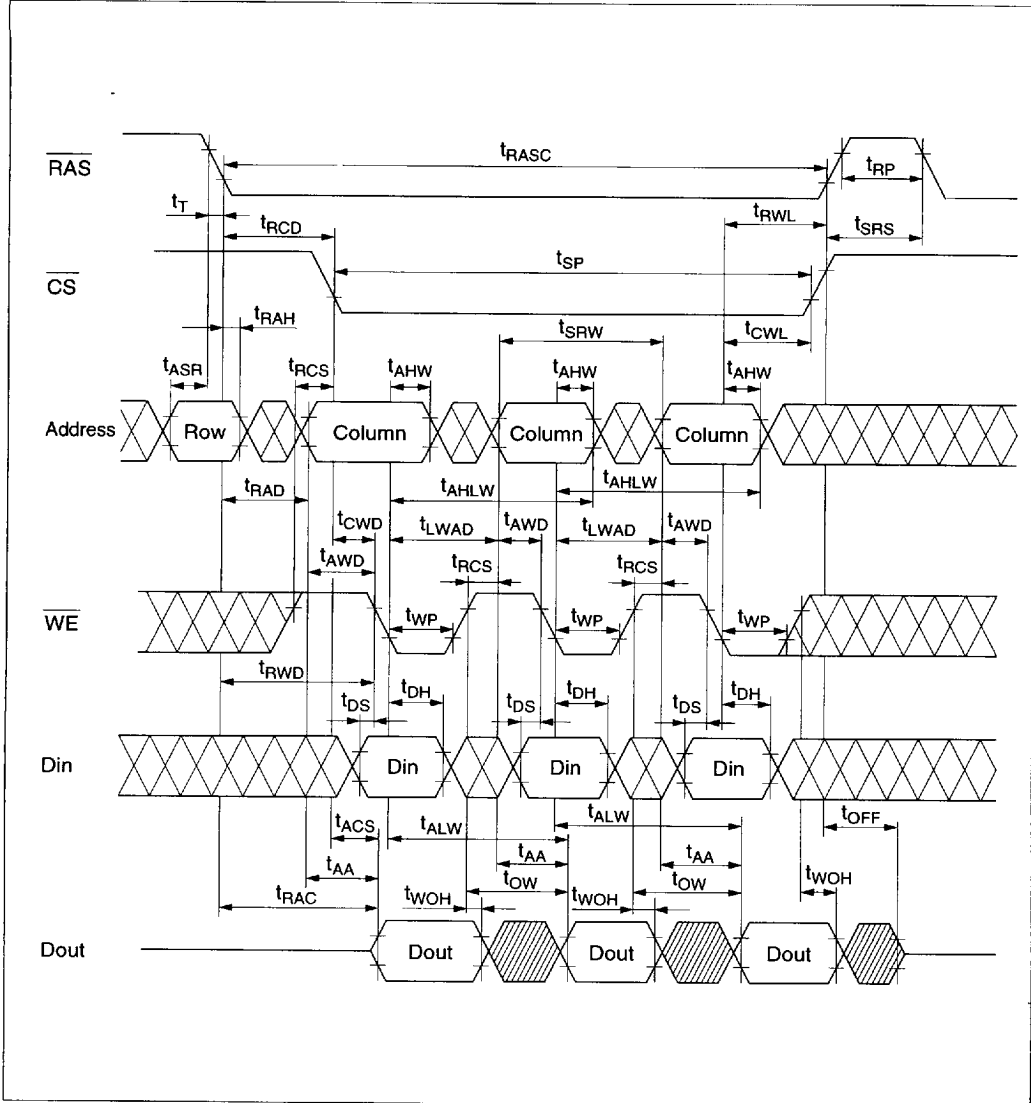


HM514102B/BL Series

Static Column Mode Write Cycle (2)



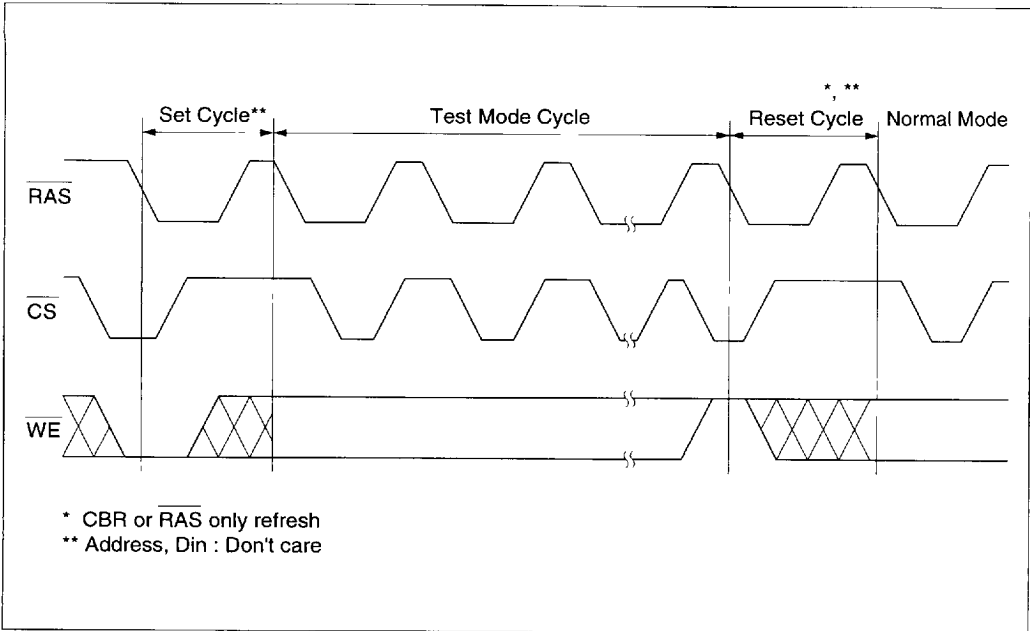
Static Column Mode Read-Modify-Write Cycle



4496203 0026281 8T2

Hitachi 83

Test Mode Cycle



Test Mode Set Cycle

