

EDAC Series 3000 ENCASED DIGITAL TO ANALOG CONVERTERS

D/A converters for virtually any application.

Features

- 20 Different Models
- 12 to 16 Bit Resolution
- Straight Binary, Offset Binary, or 2's Complement Input
- Programmable Output Range Selection
- Bipolar or Unipolar Output
- Precision Internal Voltage Reference
- Pre-Calibrated for Specified Temperature Range
- RFI and EMI Shielded
- Conversion Times to 1 μ Sec for 13 Bits, 3 μ Sec for 16 Bits
- Accuracy to 0.003% of FSR
- Optional Temperature Ranges From -55°C to 90°C
- TTL Compatible Input Holding Register
- Convenient Printed Circuit Board Mounting

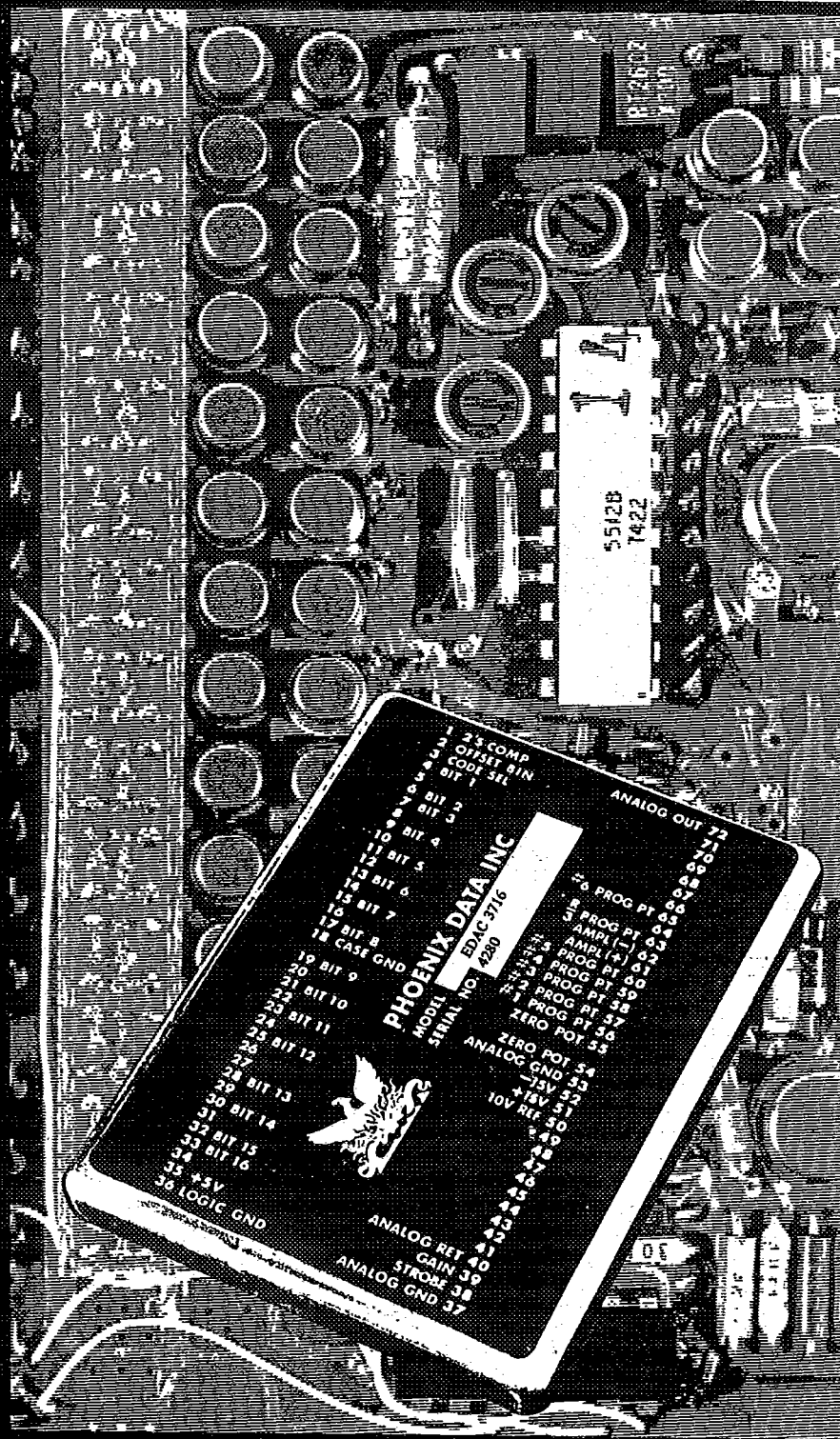
General Description

Phoenix Data precision Digital to Analog Converters have long been an accepted industry standard—providing a wide range of cost and performance configurations to meet the needs of virtually any application. Their ease of application and time-proven reliability have made them a first choice with both commercial and industrial equipment designers everywhere.

The EDAC 3000 series consists of general purpose Digital to Analog Converters employing the latest in precision component and design technology. All D/A Converters use the highly reliable voltage switching technique and are totally self-contained except for external power requirements of ± 15 and 5 volts DC.

Each converter consists of a TTL compatible input holding register, solid-state analog switches, a precision ladder network, temperature compensated internal voltage reference generator, an operational output amplifier, and a low-impedance complementary emitter follower output driver circuit. For those applications not requiring the holding register feature, the strobe input line may be connected to +5 VDC through a 1K ohm resistor, thus allowing the converter to continuously follow input data changes.

All converters are factory calibrated to published specifications over the designated temperature range, and are totally repairable. The dual-in-line pinout configuration (0.100 inch grid centers) allows convenient printed circuit board mounting.



Phoenix Data, Inc.

EDAC Series 3000

ENCASED DIGITAL TO ANALOG CONVERTERS

D/A converters for virtually any application.

Series 3000 Specifications

Model	Input Resolution / (Note 1)	Full Range Slew & Settling Time (Note 2)	Accuracy of FSR (Note 3)	Linearity of FSR	Temperature Coefficient (0°C to 70°C) (Note 4)	Performance
3012	12 Bits	15 μ S	$\pm 0.02\%$	$\pm 0.010\%$	10 ppm/°C	Standard
3112	12 Bits	15 μ S	$\pm 0.01\%$	$\pm 0.006\%$	5 ppm/°C	Precision
3212	12 Bits	1 μ S	$\pm 0.02\%$	$\pm 0.010\%$	10 ppm/°C	High Speed
3312	12 Bits	1 μ S	$\pm 0.01\%$	+0.008%	5 ppm/°C	Precision & High Speed
3413 3414 3415 3416	13 Bits 14 Bits 15 Bits 16 Bits	15 μ S 17 μ S 20 μ S 20 μ S	$\pm 0.015\%$ $\pm 0.0125\%$ $\pm 0.010\%$ $\pm 0.007\%$	$\pm 0.008\%$ $\pm 0.007\%$ $\pm 0.006\%$ $\pm 0.004\%$	10 ppm/°C	Standard
3513 3514 3515 3516	13 Bits 14 Bits 15 Bits 16 Bits	15 μ S 17 μ S 20 μ S 20 μ S	$\pm 0.010\%$ $\pm 0.007\%$ $\pm 0.005\%$ $\pm 0.003\%$	$\pm 0.006\%$ $\pm 0.004\%$ $\pm 0.003\%$ $\pm 0.0015\%$	5 ppm/°C	Precision
3613 3614 3615 3616	13 Bits 14 Bits 15 Bits 16 Bits	1 μ S 1.5 μ S 2 μ S 3 μ S	$\pm 0.015\%$ $\pm 0.0125\%$ $\pm 0.010\%$ $\pm 0.007\%$	$\pm 0.008\%$ $\pm 0.007\%$ $\pm 0.006\%$ $\pm 0.004\%$	10 ppm/°C	High Speed
3713 3714 3715 3716	13 Bits 14 Bits 15 Bits 16 Bits	2.0 μ S 2.5 μ S 3.5 μ S 4.5 μ S	$\pm 0.010\%$ $\pm 0.007\%$ $\pm 0.006\%$ $\pm 0.004\%$	$\pm 0.006\%$ $\pm 0.005\%$ $\pm 0.004\%$ $\pm 0.002\%$	5 ppm/°C	Precision & High Speed

Notes:

1. Lower resolution units available on request.
2. Conversion time includes settling time to rated accuracy for a full-range step (worse case). See Conversion Timing Diagram.
3. Accuracy figures include all error parameters.
4. Standard operating temperature range is 0°C to 70°C. Extended temperature ranges are available. Also, on special order, units available to 2.5 ppm/°C.
5. For Model Number Coding, see Ordering Information.
6. For special configurations or applications, contact your local Phoenix Data, Inc. representative or the factory.
7. The temperature coefficient includes all gain, offset, reference and differential linearity related temperature effects over 0 to 70°C. For extended operating temperature ranges the T.C. degrades by a factor of 2 from +70°C to +90°C and from 0°C to -55°C.

General Specifications

DATA INPUT SIGNALS (WITH INPUT HOLDING REGISTER, TTL COMPATIBLE)

Logic "1" voltage/current (True Input) +2.4 VDC to 5.0 VDC @ 80µA max.
 Logic "0" voltage/current (False Input) 0 VDC to 0.4 VDC @ -1.6 mA max.

Output Impedance Less than 0.02 ohm
 Output Connection Single Ended (shielded)
 Long Term Stability 0.01% FSR @ 25°C for 12 months

ADJUSTMENTS

Models 3000 thru 3300 (Up to 12 Bits)
 Internal Gain and Zero Offset adjustments for the output voltage specified.
 Pinout is provided for external Gain and Zero Offset potentiometers should the converter be used for output ranges other than that specified on order, or for additional adjustment due to temperature, etc.

Models 3400 & 3600 (13 thru 16 Bits)
 External Gain and Zero Offset potentiometers required (no internal adjustments)

Models 3500 & 3700 (13 thru 16 Bits)
 Internal Gain and Zero Offset adjustments (accessible through case). No external potentiometers required, but may be added if desired.

ENCASEMENT SHIELDING

RFI Protected on six (6) sides.
 EMI Protected on five (5) sides.

MECHANICAL

Case material Hot tin-dipped steel
 Repairability Completely repairable

ENVIRONMENTAL

Temperature
 Operating 0°C to 70°C Standard
 Optional -25°C to 85°C, or -55°C to 90°C

NOTE: The conversion error includes all error sources, ±1/2 LSB, and all temperature related errors over the temperature range of 10° to 40° C up to 12 bits and 15° to 35° C for 13 and 14 bit resolution with no adjustments. If an input range other than that specified at time of purchase is selected, the gain and offset may have to be adjusted.

Storage -55°C to 125°C
 Humidity 0 to 99% relative, no condensation

STROBE INPUT SIGNAL

Strobe input "enable" (Logic "1", True) Logic voltage and current levels same as data inputs.
 Strobe input "disable" (Logic "0", False)
 Strobe enable pulse width 50 ns min.

NOTE: Data input is transferred to the DAC output when the Strobe input goes "high" (logic 1), and the output will continue to follow the data input as long as the Strobe input remains high.

DIGITAL INPUT CODES

Straight Binary, Offset Binary, 2's Complement
 (See Input Code Selection for strapping requirements.)

ANALOG OUTPUT SIGNAL (Standard Full-Range, Selectable)

NOTE: 5.12 or 10.24 volts full-range outputs available on special order.

Output Ranges (Models 3000 thru 3300)

Bipolar B10 ±10 VDC @ 10 mA
 B5 ±5 VDC @ 10 mA
 Unipolar U10 0 to +10 VDC @ 10 mA
 N5 0 to -5 VDC @ 10 mA

Output Ranges (Series 3400 thru 3700)

Bipolar B10 ±10 VDC @ 10 mA
 B5 ±5 VDC @ 10 mA
 Unipolar U10 0 to +10 VDC @ 10 mA
 N10 0 to -10 VDC @ 10 mA
 N5 0 to -5 VDC @ 10 mA

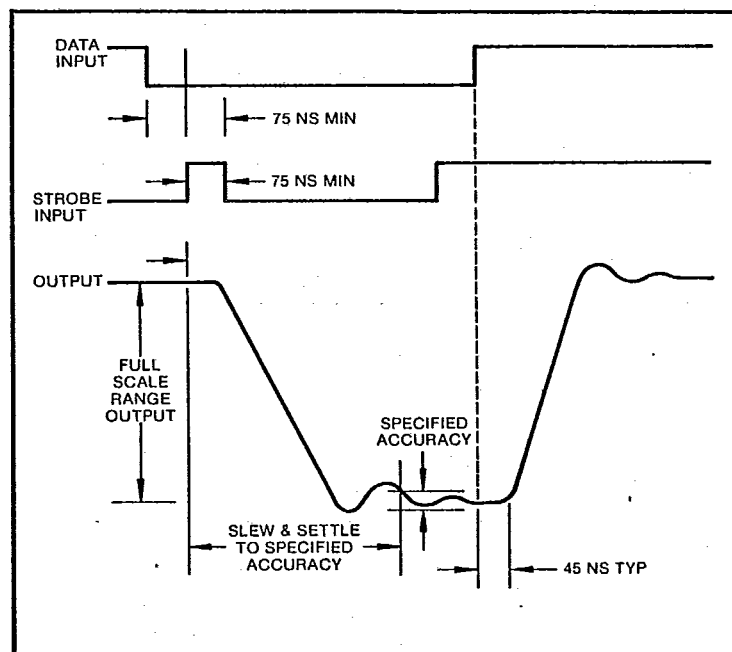
NOTE: See Range Selection Tables for strapping requirements.

POWER REQUIREMENTS

Voltage and current +15 VDC ±5% @ 100 mA
 -15 VDC ±5% @ 50 mA
 + 5 VDC ±5% @ 200 mA
 + 5 VDC ±0.5% @ 200 mA (on precision models)

Voltage Reference Internal (Regulated +10 VDC)
 Package Configuration See Physical Dimensions & Pin Connections

Conversion Timing Diagram



Physical Dimensions & Pin Connections

Models 3400 thru 3700

SHADED PINS DESIGNATE PINS USED

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	2 S COMPLEMENT	16		31		46		61	AMP (+)
2	OFFSET BINARY CODE SEL	17	BIT 8	32	BIT 15	47		62	AMP (-)
3		18	CASE GND	33	BIT 16	48		63	R/3 PROG PT.
4	BIT 1	19	BIT 9	34		49		64	
5		20		35	+5 V ± 5%	50	10 V REF	65	PROG PT. #5
6	BIT 2	21	BIT 10	36	LOG GND	51	-15 V ± 5%	66	
7	BIT 3	22		37	ANA GND	52	-15 V ± 5%	67	
8		23	BIT 11	38	STROBE	53	ANA GND	68	
9	BIT 4	24		39	GAIN ADJ	54	ZERO POT	69	
10		25	BIT 12	40	+15 V RET	55	ZERO POT	70	
11	BIT 5	26		41		56	PROG PT. #1	71	
12		27		42		57	PROG PT. #2	72	ANA OUT (±10 mA)
13	BIT 6	28	BIT 13	43		58	PROG PT. #3		
14		29		44		59	PROG PT. #4		
15	BIT 7	30	BIT 14	45		60	PROG PT. #5		

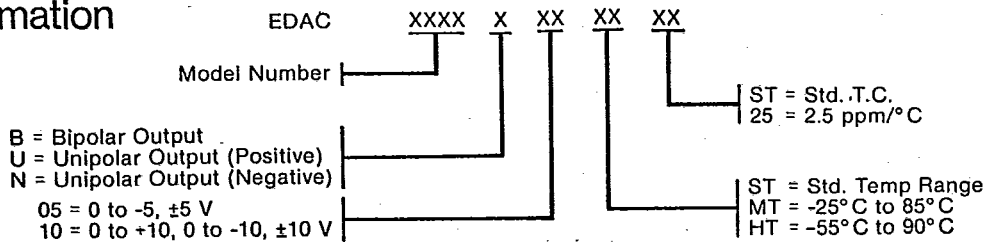
NOTE: TO DISABLE INPUT HOLDING REGISTER, CONNECT STROBE INPUT (PIN 38) TO +5VDC THROUGH 1K OHM RESISTOR. THE OUTPUT WILL CONTINUOUSLY FOLLOW INPUT DATA CHANGES.

Models 3000 thru 3300

SHADING DENOTES PINS USED

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 INPUT	16	BIT 9	31		46		61	
2	BIT 2 INPUT	17	BIT 10	32	-15 V ± 5%	47	ANALOG OUTPUT	62	
3	BIT 3 INPUT	18	BIT 11	33		48	GAIN ADJ	63	
4	BIT 4 INPUT	19	BIT 12	34	+15 V RETURN	49		64	ANALOG RET
5		20		35		50	PROG PT. #4	65	
6		21		36	-5 V RETURN	51	PROG PT. #5	66	
7		22	ENABLE	37		52	PROG PT. #6	67	
8		23		38	PROG PT. AMPL -	53	10 V REF	68	
9	BIT 5	24		39	PROG PT. AMPL +	54		69	
10	BIT 6	25		40	10 V REF	55		70	
11	BIT 7	26		41	PROG PT. #2	56		71	ZERO ADJ
12	BIT 8	27		42		57		72	
13		28	+5 V ± 5%	43		58			
14		29	+15 V ± 5%	44	PROG PT. #3	59			
15		30		45		60			

Ordering Information



Warranty

Phoenix Data, Inc. warrants its products to be free from defects in material and workmanship, under normal use and service, for a period of 90 days from date of original shipment. Warranty obligations shall be limited to replacing or repairing, at our option, any product returned, transportation charges prepaid, and found to be defective within the warranty period.



For additional information, contact your Phoenix Data representative, or:

Phoenix Data, Inc.

3384 WEST OSBORN ROAD PHOENIX, ARIZONA 85017 PHONE 602/278-8528 TWX 910-951-1364

Phoenix Data, Inc. reserves the right, at any time and without notice, to change specifications and configurations presented within this data sheet, and assumes no responsibility for the application or use of circuitry herein described.

REPRESENTATIVE:

Installation

POWER CONNECTIONS

If the DAC is to be remotely located three (3) feet or more from its external power source, each power supply voltage lead should be twisted with its respective ground return. Also, should the DAC be located in a rack or chassis with other equipment, all operating from a common power supply, then careful attention to system grounding and power distribution rules should be considered to prevent ground loops and cross-talk between system components.

DIGITAL INPUT SIGNALS

All digital input data and control signals drive TTL compatible integrated circuits, with each input representing one TTL unit load. All normal precautions associated with TTL input logic should apply.

ANALOG OUTPUT

To minimize noise, it is recommended that a twisted-pair, shielded cable be used to connect the *analog output* and *analog return* of the DAC to its terminating device. The shield should be connected to the analog return line at one end only—preferably at the DAC (source) end.

GROUND CONNECTIONS

The common (ground) return for the ± 15 VDC supplies and the +5 VDC supply are not connected externally. This connection must be made at the DAC pinout or elsewhere in the system. If the connection is not made at the DAC, caution should be taken to limit the voltage difference between the DAC power supply ground return pins to ± 0.25 VDC maximum, including DC offset and peak noise.

Warning Notes

POWER SUPPLY OVERVOLTAGE

Externally supplied power voltages must not exceed specified limits for proper DAC operation. Power supply turn-on/turn-off surging must be suppressed to prevent damage to the DAC circuit. Permanent damage may occur if transients greater than ± 18 VDC or +7 VDC are present on the ± 15 VDC and +5 VDC supply lines respectively.

SHORT CIRCUITS

A short circuit of any input/output connection to any power supply voltage can cause permanent damage to the DAC.

A short circuit of any input/output connection to ground will *not* damage the DAC, except for the reference output.

Gain and Zero Adjustment

ZERO ADJUST

Adjust zero potentiometer for 0.0 VDC output with all-zero code input.

GAIN ADJUST

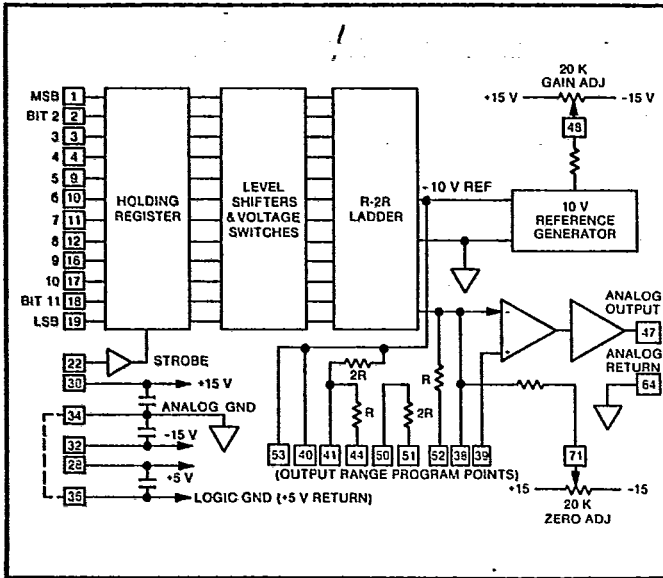
Adjust the gain potentiometer such that the output swing from -F.S. to +F.S. is equal to the specified full-scale range, less *one* LSB. For bipolar units, the positive F.S. magnitude should be equal to $(\frac{2^{(\text{NO. OF BITS})} - 1}{2})$ bit weight or (1/2 full range - one LSB); and, the negative F.S. magnitude should be equal to $(\frac{2^{(\text{NO. OF BITS})}}{2})$ bit weight or (1/2 full range).

F.S. = Full Scale

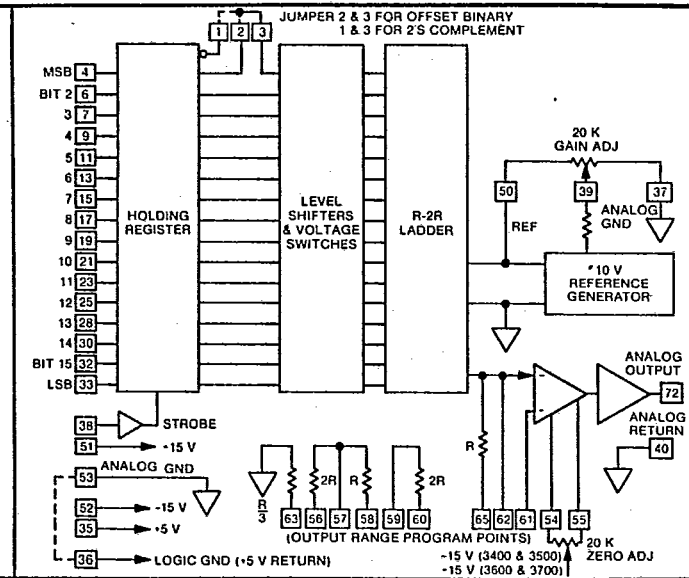
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Application Information

Block Diagram (Models 3000 thru 3300)



Block Diagram (Models 3400 thru 3700)



Programmable Output Range Selection (Pinout jumper connections)

Models 3000 thru 3300

BIPOLAR		UNIPOLAR	
B10(±10VDC)	B5(±5VDC)	U10(0 TO +10VDC)	N5(0 TO -5VDC)
51 to 47	51 to 64	51 to 53	39 to 64
50 to 38	44 to 64	44 to 64	44 to 38
44 to 64	52 to 47	52 to 47	52 to 47
41 to 39	41 to 39	41 to 39	41 to 47
	50 to 39	50 to 39	

Models 3400 thru 3700

BIPOLAR		UNIPOLAR		
B10(±10VDC)	B5(±5VDC)	U10(0 TO +10VDC)	N5(0 TO -5VDC)	N10(0 TO -10VDC)
50 to 56	50 to 56	50 to 56	53 to 56	53 to 56
57 to 61	57 to 61	57 to 61	57 to 72	57 to 62
53 to 58	53 to 58	53 to 58	58 to 62	53 to 58
59 to 72	59 to 61	59 to 61	53 to 59	59 to 61
60 to 62	53 to 60	50 to 60	53 to 60	53 to 60
53 to 63	65 to 72	65 to 72	65 to 72	65 to 72
	53 to 63	53 to 63	61 to 63	53 to 63

Input Code Selection

(Models 3400 thru 3700 only)

BIPOLAR

- Two's Complement: connect pin 1 to pin 3. With this arrangement, the MSB is a logic "1" for all negative value outputs.
- Offset Binary: connect pin 2 to pin 3. With this connection, the MSB is a logic "0" for negative value outputs.

UNIPOLAR

- Straight Binary: connect pin 2 to pin 3

Binary Weights for D/A Converters

(Fraction or full-scale range)

MSB 2 ⁻⁰	.5
2 ⁻¹	.25
2 ⁻²	.125
2 ⁻³	.0625
2 ⁻⁴	.03125
2 ⁻⁵	.015625
2 ⁻⁶	.0078125
2 ⁻⁷	.00390625
2 ⁻⁸	.001953125
2 ⁻⁹	.0009765625
2 ⁻¹⁰	.00048828125
2 ⁻¹¹	.000244140625
2 ⁻¹²	.0001220703125
2 ⁻¹³	.00006103515625
2 ⁻¹⁴	.000030517578125
2 ⁻¹⁵	.0000152587890625
2 ⁻¹⁶	.00000762939453125