

## Features

- Pin- and function-compatible with CY7C1020B
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - $I_{CC} = 80 \text{ mA @ } 10\text{ns}$
- Low complementary metal oxide semiconductor (CMOS) standby power
  - $I_{SB2} = 3 \text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide Molded SOJ and 44-pin thin small outline package (TSOP) II packages

## Functional Description <sup>[1]</sup>

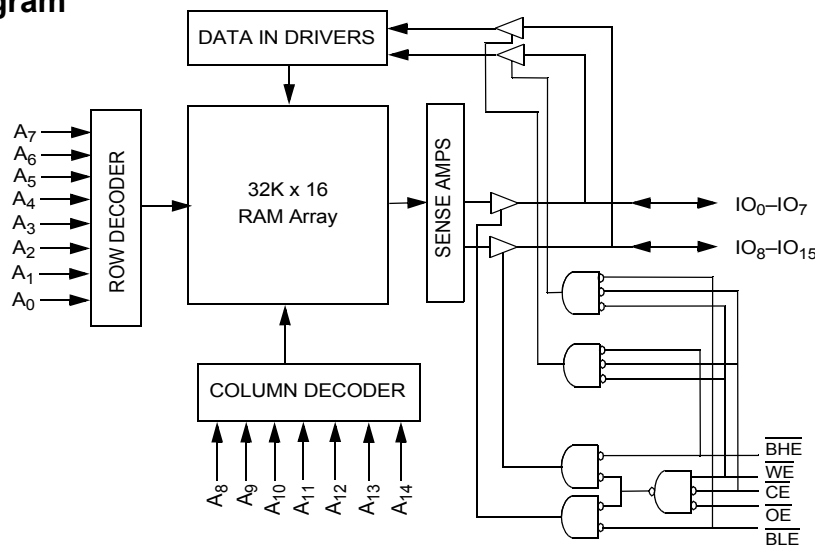
The CY7C1020D is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected. The input and output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high-impedance state when:

- Deselected ( $\overline{CE}$  HIGH)
- Outputs are disabled ( $\overline{OE}$  HIGH)
- $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH)
- When the write operation is active ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW)

Write to the device by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>14</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>14</sub>).

Reading from the device by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 9 for a complete description of read and write modes.

## Logic Block Diagram



### Note

1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

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## Pin Configurations<sup>[2]</sup>

### SOJ/TSOP II Top View

NC	□ 1	44	□ A <sub>5</sub>
A <sub>3</sub>	□ 2	43	□ A <sub>6</sub>
A <sub>2</sub>	□ 3	42	□ A <sub>7</sub>
A <sub>1</sub>	□ 4	41	□ $\overline{OE}$
A <sub>0</sub>	□ 5	40	□ $\overline{BHE}$
$\overline{CE}$	□ 6	39	□ $\overline{BLE}$
IO <sub>0</sub>	□ 7	38	□ IO <sub>15</sub>
IO <sub>1</sub>	□ 8	37	□ IO <sub>14</sub>
IO <sub>2</sub>	□ 9	36	□ IO <sub>13</sub>
IO <sub>3</sub>	□ 10	35	□ IO <sub>12</sub>
V <sub>CC</sub>	□ 11	34	□ V <sub>SS</sub>
V <sub>SS</sub>	□ 12	33	□ V <sub>CC</sub>
IO <sub>4</sub>	□ 13	32	□ IO <sub>11</sub>
IO <sub>5</sub>	□ 14	31	□ IO <sub>10</sub>
IO <sub>6</sub>	□ 15	30	□ IO <sub>9</sub>
IO <sub>7</sub>	□ 16	29	□ IO <sub>8</sub>
$\overline{WE}$	□ 17	28	□ NC
A <sub>4</sub>	□ 18	27	□ A <sub>8</sub>
A <sub>14</sub>	□ 19	26	□ A <sub>9</sub>
A <sub>13</sub>	□ 20	25	□ A <sub>10</sub>
A <sub>12</sub>	□ 21	24	□ A <sub>11</sub>
NC	□ 22	23	□ NC

## Selection Guide

	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA

### Note

- NC pins are not connected on the die.

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage on V<sub>CC</sub> to Relative GND <sup>[3]</sup> ..-0.5 V to +6.0 V  
 DC voltage applied to outputs in High Z State <sup>[3]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V

DC input voltage <sup>[3]</sup> ..... -0.5 V to V<sub>CC</sub> + 0.5 V  
 Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage..... >2001 V (per MIL-STD-883, Method 3015)  
 Latch-up current ..... >200mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	-40 °C to +85 °C	5 V ± 0.5 V	10 ns

## Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-10 (Industrial)		Unit	
			Min	Max		
V <sub>OH</sub>	Output HIGH voltage	I <sub>OH</sub> = -4.0 mA	2.4	-	V	
V <sub>OL</sub>	Output LOW voltage	I <sub>OL</sub> = 8.0 mA	-	0.4	V	
V <sub>IH</sub>	Input HIGH voltage	-	2.2	V <sub>CC</sub> + 0.5V	V	
V <sub>IL</sub>	Input LOW voltage <sup>[3]</sup>	-	-0.5	0.8	V	
I <sub>Ix</sub>	Input load current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA	
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , output disabled	-1	+1	μA	
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>max</sub> = 1/t <sub>RC</sub>	100 MHz	-	80	mA
			83 MHz	-	72	mA
			66 MHz	-	58	mA
			40 MHz	-	37	mA
I <sub>SB1</sub>	Automatic CE power-down current—TTL inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>max</sub>	-	10	mA	
I <sub>SB2</sub>	Automatic CE Power-Down current—CMOS inputs	Max V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	-	3	mA	

### Note

3. V<sub>IL</sub>(min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.

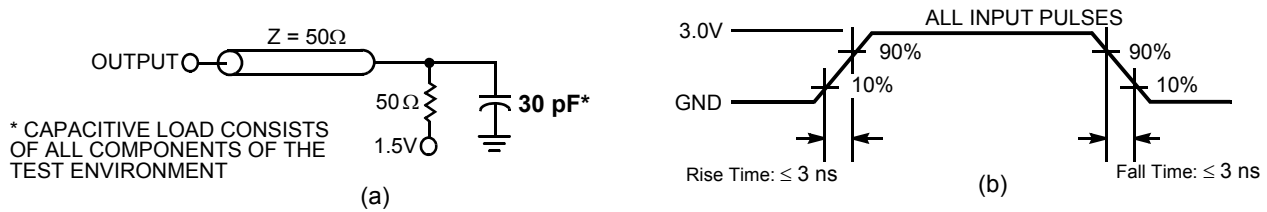
Capacitance [4]

Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

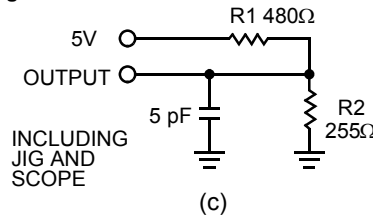
Thermal Resistance [4]

Parameter	Description	Test Conditions	SOJ	TSOP II	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		36.75	21.24	°C/W

AC Test Loads and Waveforms [5]



High-Z characteristics:



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

**Switching Characteristics** (Over the Operating Range) <sup>[6]</sup>

Parameter	Description	-10 (Industrial)		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}^{[7]}$	$V_{\text{CC}}$ (typical) to the first access	100	–	$\mu\text{s}$
$t_{\text{RC}}$	Read cycle time	10	–	ns
$t_{\text{AA}}$	Address to data valid	–	10	ns
$t_{\text{OHA}}$	Data hold from address change	3	–	ns
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to data valid	–	10	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to data valid	–	5	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low Z <sup>[9]</sup>	0	–	ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High Z <sup>[8, 9]</sup>	–	5	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to Low Z <sup>[9]</sup>	3	–	ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to High Z <sup>[8, 9]</sup>	–	5	ns
$t_{\text{PU}}^{[10]}$	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
$t_{\text{PD}}^{[10]}$	$\overline{\text{CE}}$ HIGH to power-down	–	10	ns
$t_{\text{DBE}}$	Byte enable to data valid	–	5	ns
$t_{\text{LZBE}}$	Byte enable to Low Z	0	–	ns
$t_{\text{HZBE}}$	Byte disable to High Z	–	5	ns
<b>Write Cycle</b> <sup>[11, 12]</sup>				
$t_{\text{WC}}$	Write cycle time	10	–	ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to write end	7	–	ns
$t_{\text{AW}}$	Address set-up to write end	7	–	ns
$t_{\text{HA}}$	Address hold from write end	0	–	ns
$t_{\text{SA}}$	Address set-up to write start	0	–	ns
$t_{\text{PWE}}$	$\overline{\text{WE}}$ pulse width	7	–	ns
$t_{\text{SD}}$	Data set-up to write end	6	–	ns
$t_{\text{HD}}$	Data hold from write end	0	–	ns
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to Low Z <sup>[9]</sup>	3	–	ns
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to High Z <sup>[8, 9]</sup>	–	5	ns
$t_{\text{BW}}$	Byte enable to end of write	7	–	ns

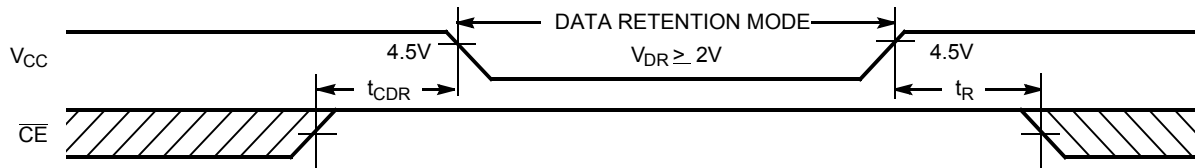
**Notes**

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and 30-pF load capacitance.
7.  $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access can be performed.
8.  $t_{\text{HZOE}}$ ,  $t_{\text{HZBE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (c) of "AC Test Loads and Waveforms [5]" on page 5. Transition is measured when the outputs enter a high impedance state.
9. At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW,  $\overline{\text{WE}}$  LOW and  $\overline{\text{BHE}}/\overline{\text{BLE}}$  LOW.  $\overline{\text{CE}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{BHE}}/\overline{\text{BLE}}$  must be LOW to initiate a write and the transition of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

**Data Retention Characteristics** (Over the Operating Range)

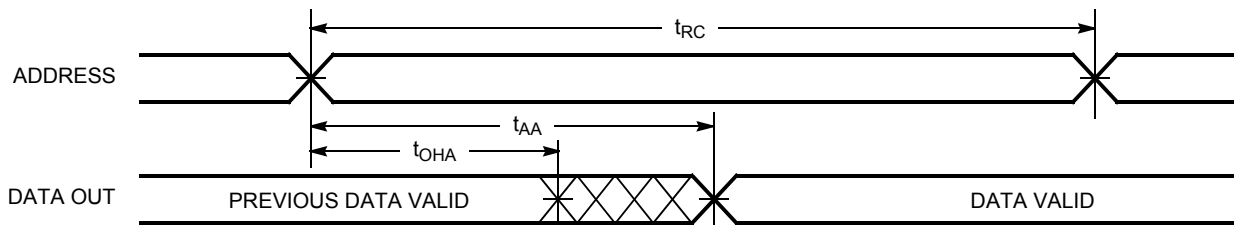
Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention	-	2.0	-	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	-	3	mA
$t_{CDR}^{[13]}$	Chip deselect to data retention time	-	0	-	ns
$t_R^{[14]}$	Operation recovery time	-	$t_{RC}$	-	ns

**Data Retention Waveform**

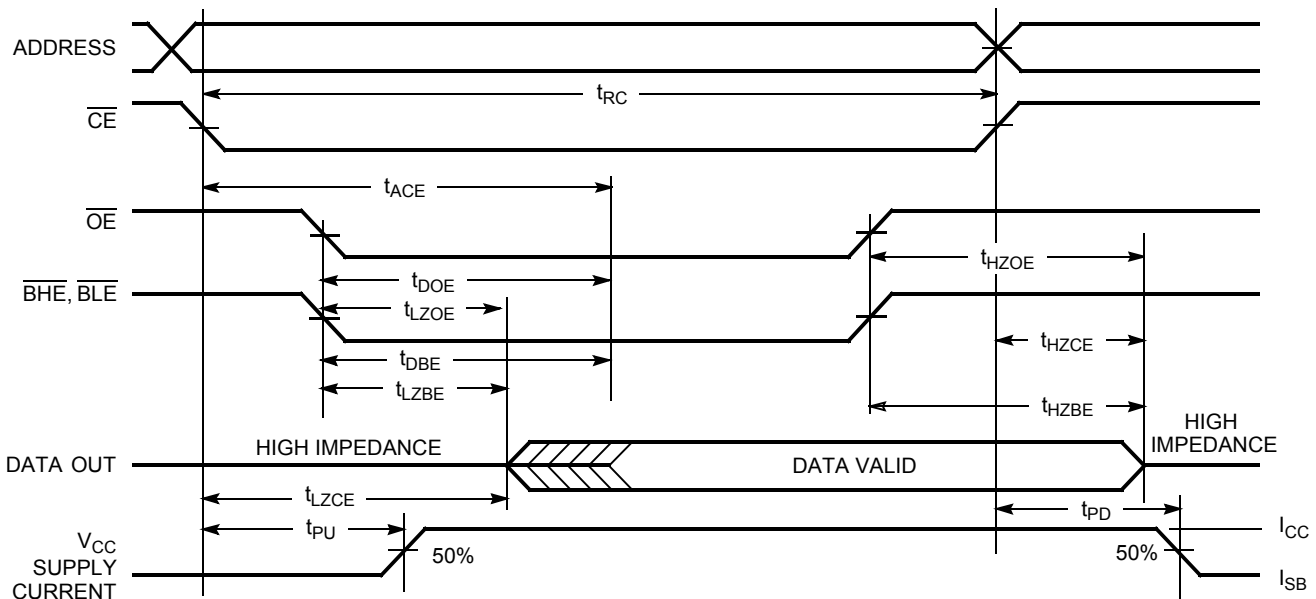


**Switching Waveforms**

**Figure 1. Read Cycle No.1 (Address Transition Controlled)** [15, 16]



**Figure 2. Read Cycle No.2 (OE Controlled)** [16, 17]



**Notes**

- 13. Tested initially and after any design or process changes that may affect these parameters.
- 14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .
- 15. Device is continuously selected. OE, CE, BHE and/or BLE =  $V_{IL}$ .
- 16. WE is HIGH for read cycle.
- 17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms(continued)

Figure 3. Write Cycle No. 1 ( $\overline{CE}$  Controlled) [18, 19]

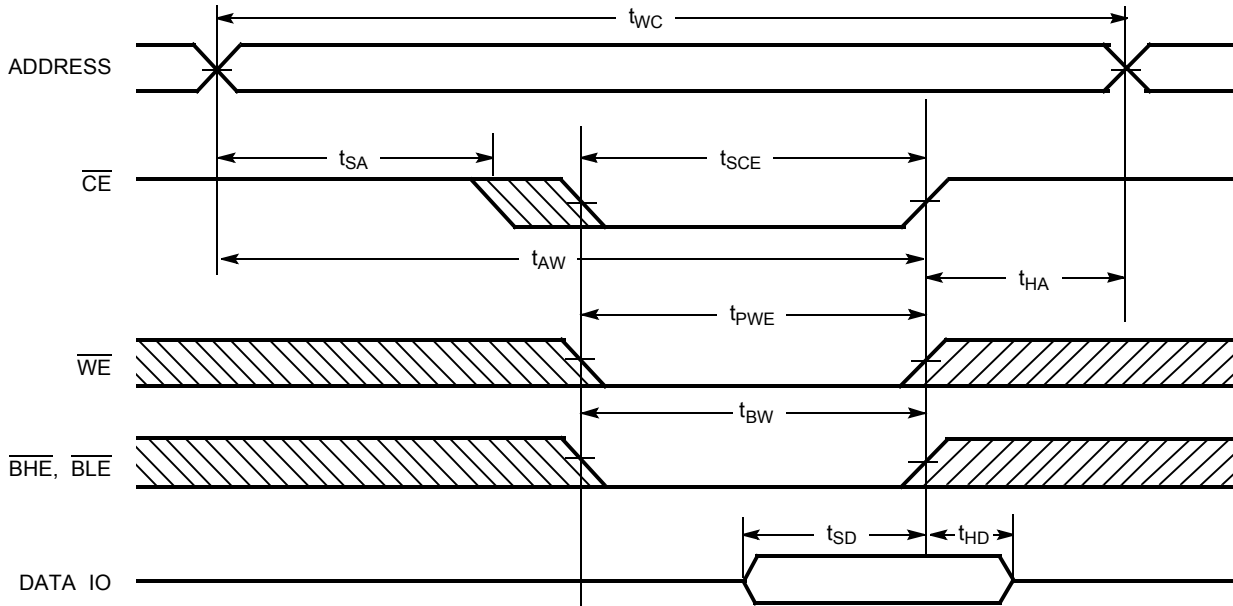
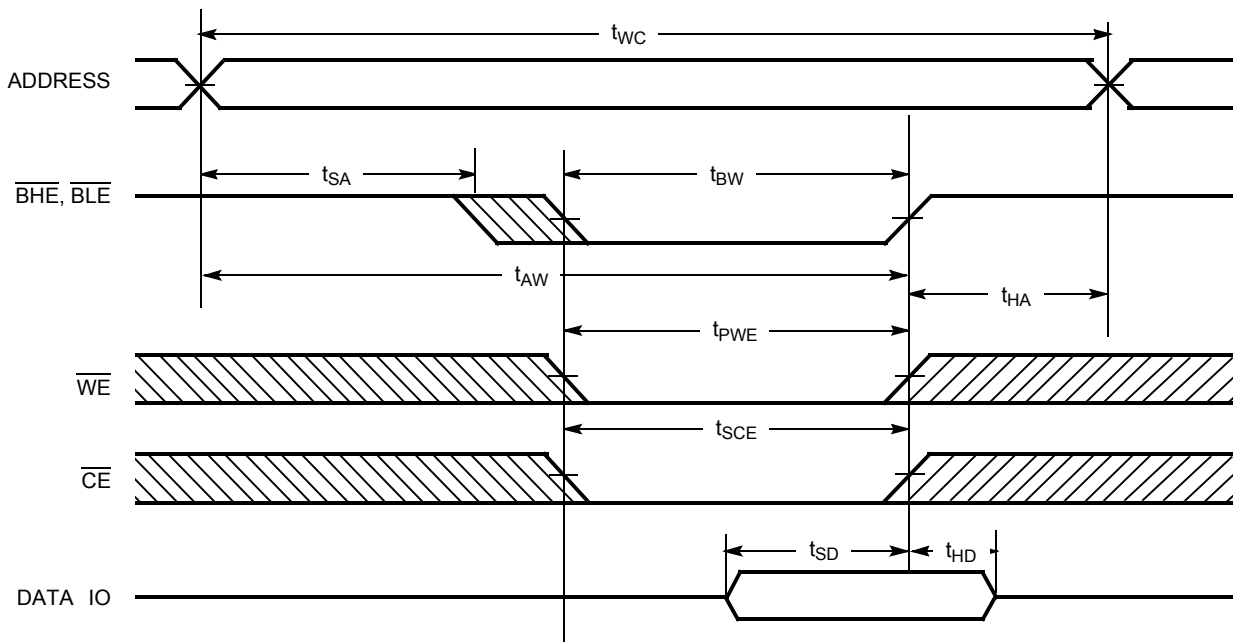


Figure 4. Write Cycle No. 2 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled) [18, 19]



Notes

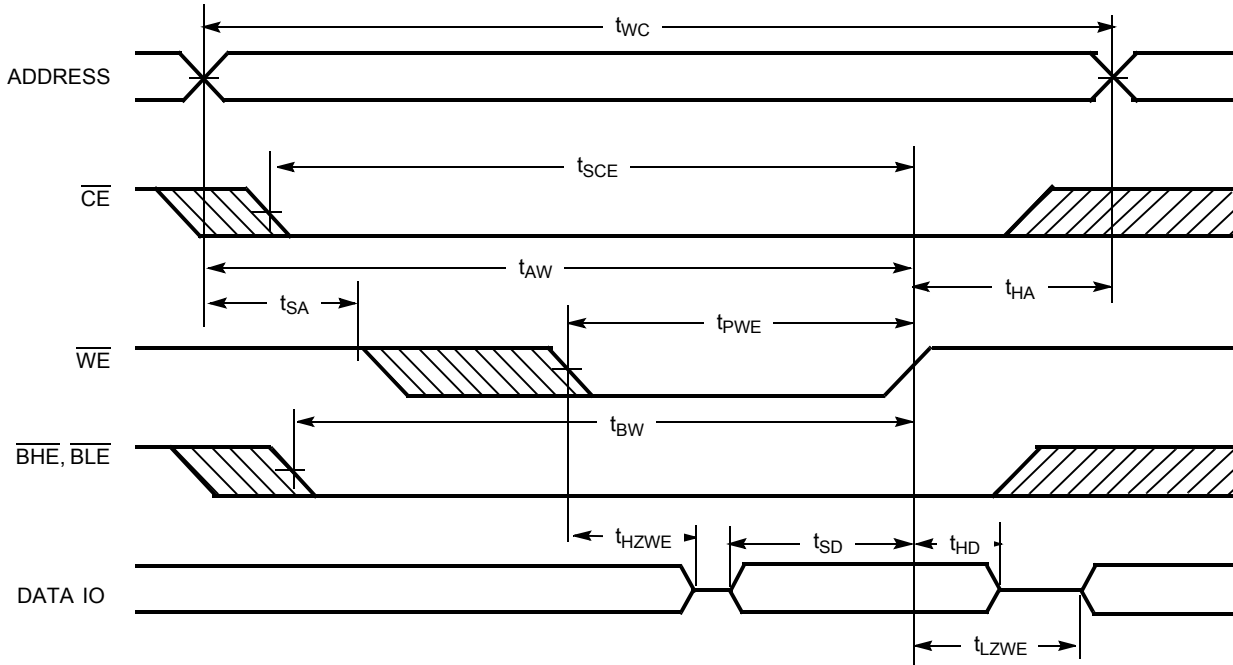
18. Data IO is high impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .

19. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.



Switching Waveforms(continued)

Figure 5. Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [20, 21]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$IO_0-IO_7$	$IO_8-IO_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data out	Data out	Read – All bits	Active ( $I_{CC}$ )
			L	H	Data out	High Z	Read – Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data out	Read – Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data in	Data in	Write – All bits	Active ( $I_{CC}$ )
			L	H	Data in	High Z	Write – Lower bits only	Active ( $I_{CC}$ )
			H	L	High Z	Data in	Write – Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High Z	High Z	selected, outputs disabled	Active ( $I_{CC}$ )

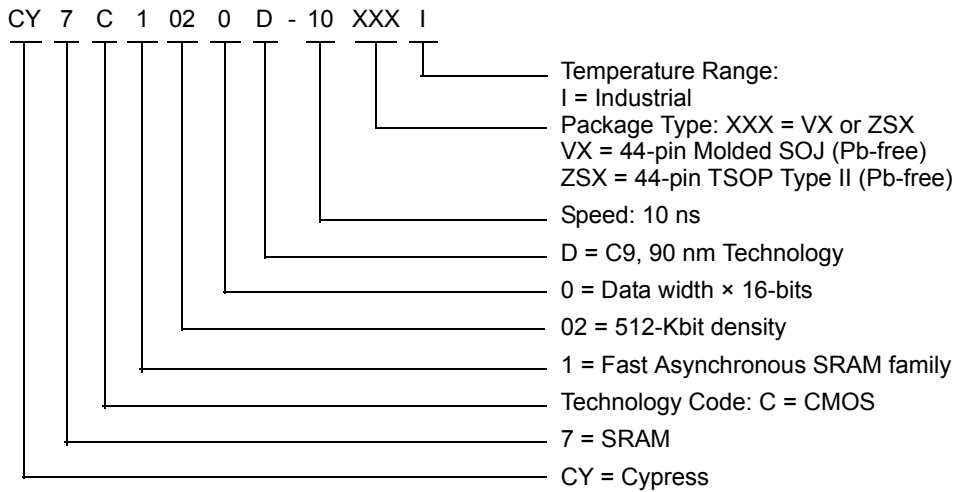
Notes

- 20. The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 21. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1020D-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1020D-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	

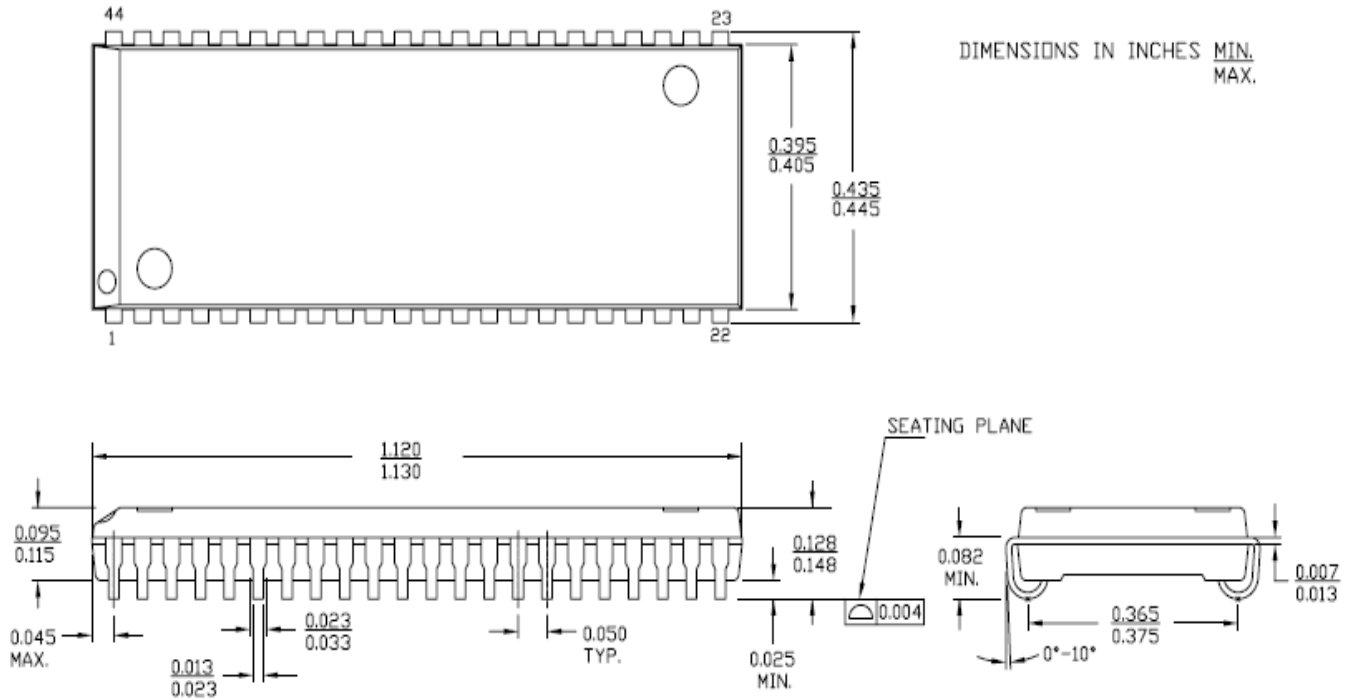
**Ordering Code Definitions**



Please contact your local Cypress sales representative for availability of these parts.

Package Diagrams

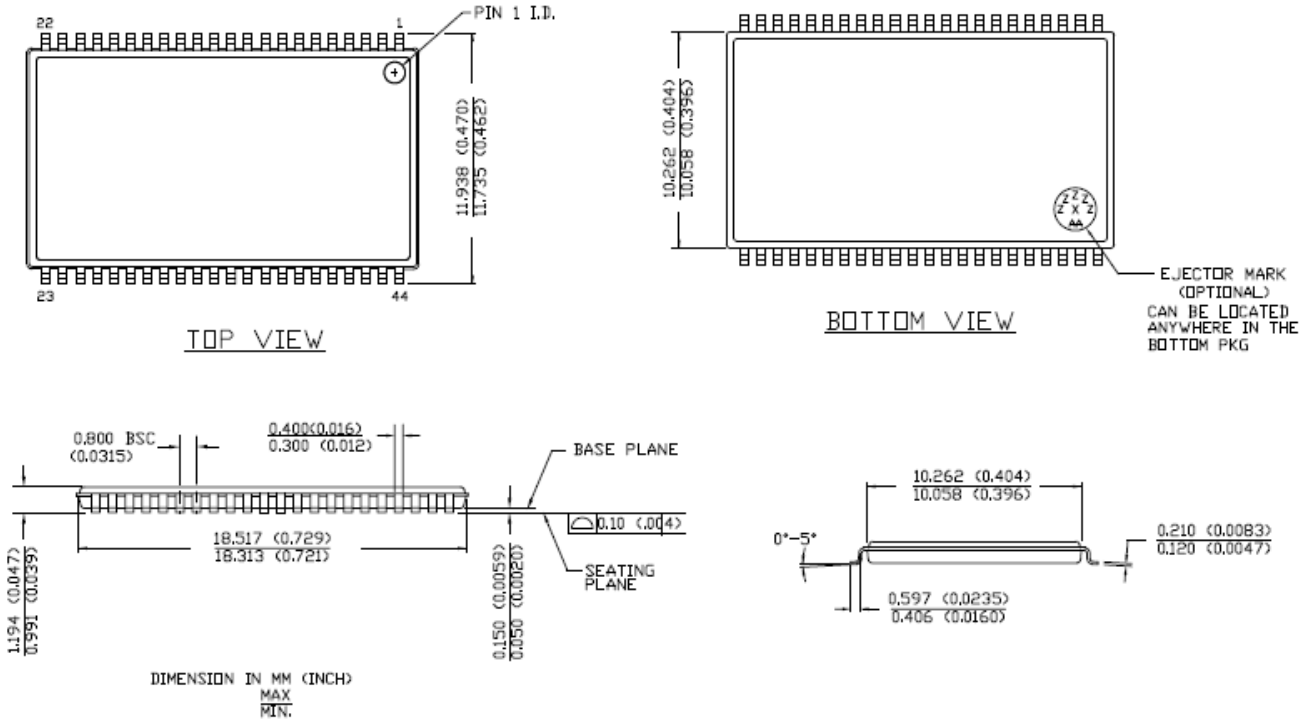
Figure 6. 44-pin (400-Mil) Molded SOJ, 51-85082



51-85082 \*C

Package Diagrams(continued)

Figure 7. 44-Pin Thin Small Outline Package Type II, 51-85087



51-85087 \*C

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## Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
FBGA	very fine ball grid array
I/O	input/output
TSOP	thin small outline package
SRAM	static random access memory
TTL	Transistor transistor logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY7C1020D, 512K (32K x 16) Static RAM Document #: 38-05463				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233695	See ECN	RKF	1) DC parameters modified as per EROS (Spec # 01-0216) 2) Pb-free Offering in the 'Ordering Information'
*B	263769	See ECN	RKF	1) Corrected pin #18 on SOJ/TSOPII Pinout (Page #1) from A <sub>15</sub> to A <sub>4</sub> 2) Changed IO <sub>1</sub> - IO <sub>16</sub> to IO <sub>0</sub> - IO <sub>15</sub> on the Pin-out diagram 3) Added T <sub>power</sub> Spec in Switching Characteristics Table 4) Added Data Retention Characteristics Table and Waveforms 5) Shaded 'Ordering Information'
*C	307594	See ECN	RKF	Reduced Speed bins to -10, -12 and -15 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #3
*E	802877	See ECN	VKN	Changed I <sub>CC</sub> specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3109992	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*G	3219056	04/07/2011	PRAS	Added TOC Added Acronyms and Units of Measure table. Updated Datasheet as per template.

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### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)  
PSoC 1 | PSoC 3 | PSoC 5

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