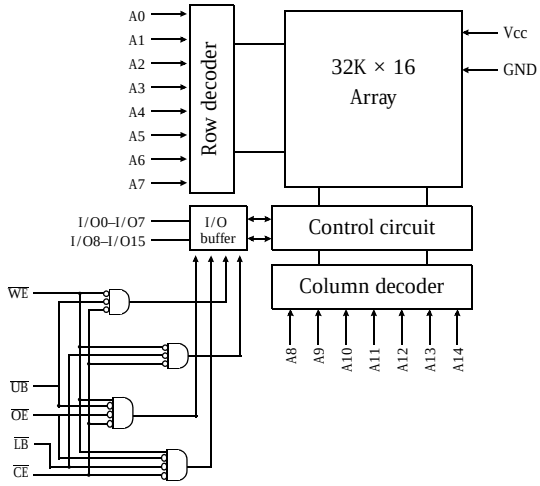
5V/3.3V 32K×16 CMOS SRAM

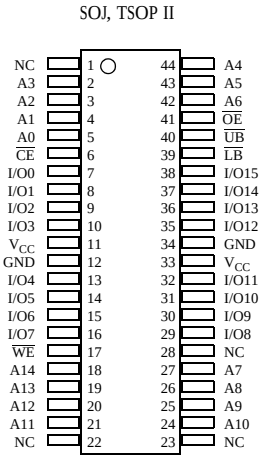
Features

- Organization: 32,768 words × 16 bits
- High speed
  - 10/12/15/20 ns address access time
  - 5/6/8/10 ns output enable access time
- Low power consumption
  - Active: 504 mW max (20 ns cycle)
  - Standby: 18 mW max, CMOS I/O
  - Very low DC component in active power
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- 44-pin JEDEC standard package
  - 400 mil SOJ
  - 400 mil TSOP II
- Upward compatibility
  - 64K×16 (AS7C1026)
  - 256K×16 (AS7C4098)
- Center power and ground pins
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- 3.3V version available (AS7C3513)

Logic block diagram



Pin arrangement



Selection guide

		7C513-10 7C3513-10	7C513-12 7C3513-12	7C513-15 7C3513-15	7C513-20 7C3513-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		5	5	8	10	ns
Maximum operating current	AS7C513	170	160	150	140	mA
	AS7C3513	130	120	110	100	mA
Maximum CMOS standby current		5	5	5	5	mA

Shaded areas indicate advance information.

Functional description

The AS7C513 is a high performance CMOS 524,288-bit Static Random Access Memory (SRAM) organized as 32,768 words × 16 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 5/6/8/10 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is High the device enters standby mode. The AS7C513 is guaranteed not to exceed 28 mW power consumption in CMOS standby mode. This device also offers 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

This device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C513 is packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any pin relative to GND	V_t	–1	+7.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	–55	+150	°C
Temperature under bias	T_{bias}	–10	+85	°C
DC output current	I_{out}	–	50	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15
L L	H X	H X	X H	X H	High Z	High Z	Output disable

Key: X = don't care, L = Low, H = High

Recommended operating conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage	AS7C513	V_{CC}	4.5	5.0	5.5	V
	AS7C3513	V_{CC}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
Input voltage	AS7C513	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C3513	V_{IH}	2.0	–	V_{CC} + 0.5	
		V_{IL}	–0.5†	–	0.8	V
Ambient operating temperature		T_A	0	-	70	°C

† V_{IL} min = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics

				-10		-12		-15		-20		
Parameter	Symbol	Test conditions		Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	$0V \le V_{in} \le V_{CC}$		-5	5	-5	5	-5	5	-5	5	µA
Output leakage current	$\lvert I_{LO} \rvert$	Outputs disabled $0V \le V_{out} \le V_{CC}$		-5	5	-5	5	-5	5	-5	5	µA
Operating power supply current	I_{CC}	$\overline{CE} \le V_{IL}$, V_{CC} = Max outputs open, $f = f_{Max} = 1/t_{RC}$	AS7C513	–	170	–	160	–	150	–	140	mA
			AS7C3513	–	130	–	120	–	110	–	100	
Standby power supply current	I_{SB}	$\overline{CE} \le V_{IL}$, V_{CC} = Max outputs open, $f = f_{Max} = 1/t_{RC}$		–	70	–	60	–	50	–	40	mA
	I_{SB1}	$\overline{CE} \ge V_{CC}$–0.2V, V_{CC} = Max, $V_{in} \le$ GND + 0.2V or $V_{in} \ge V_{CC}$ - 0.2V, f = 0		–	5	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V

Shaded areas indicate advance information.

Capacitance

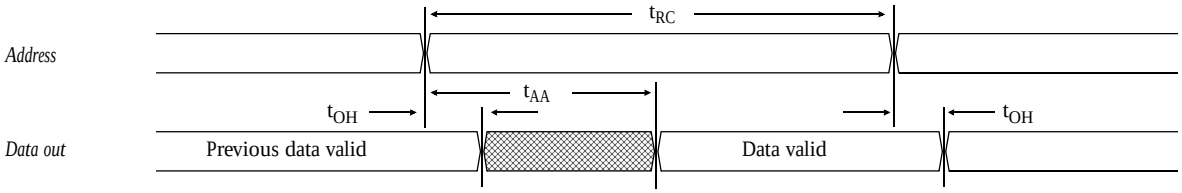
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out}$ = 0V	7	pF

Read cycle [3,9]

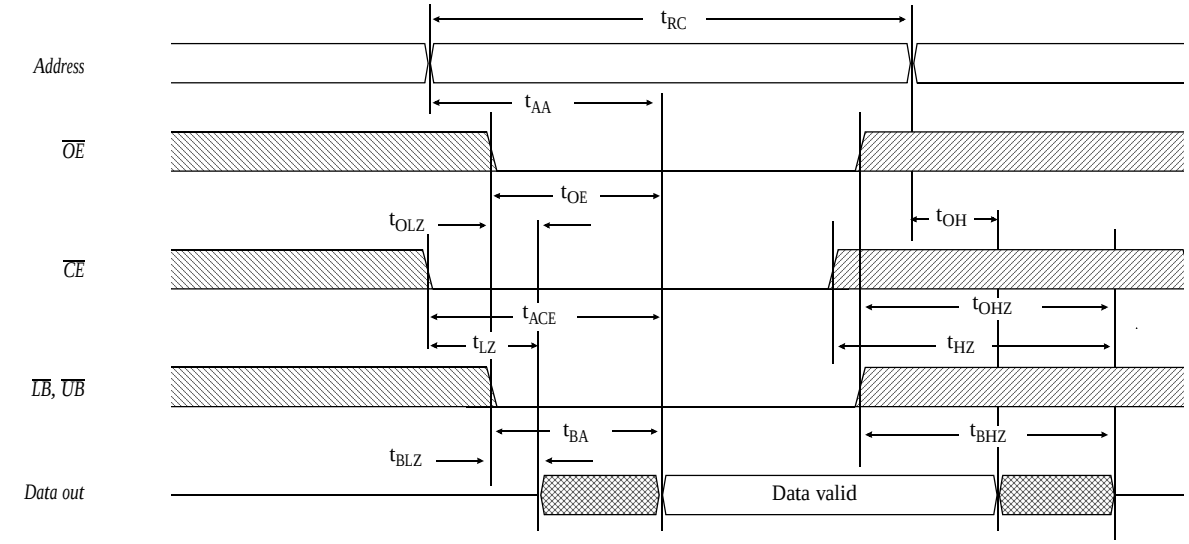
		-10		-12		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	5	–	5	–	8	–	10	ns	
Output hold from address change	t_{OH}	3	–	3	–	4	–	4	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ High to output in high Z	t_{CHZ}	–	5	–	6	–	6	–	8	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
Byte select access time	t_{BA}	–	5	–	6	–	8	–	10	ns	
Byte select Low to Low-Z	t_{BLZ}	0	–	0	–	0	–	0	–	ns	4,5
Byte select High to High-Z	t_{BHZ}	–	5	–	6	–	6	–	8	ns	4,5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	5	–	6	–	6	–	8	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5

Shaded areas indicate advance information.

Read waveform 1 [3,6,7,9]



Read waveform 2 [3,6,8,9]

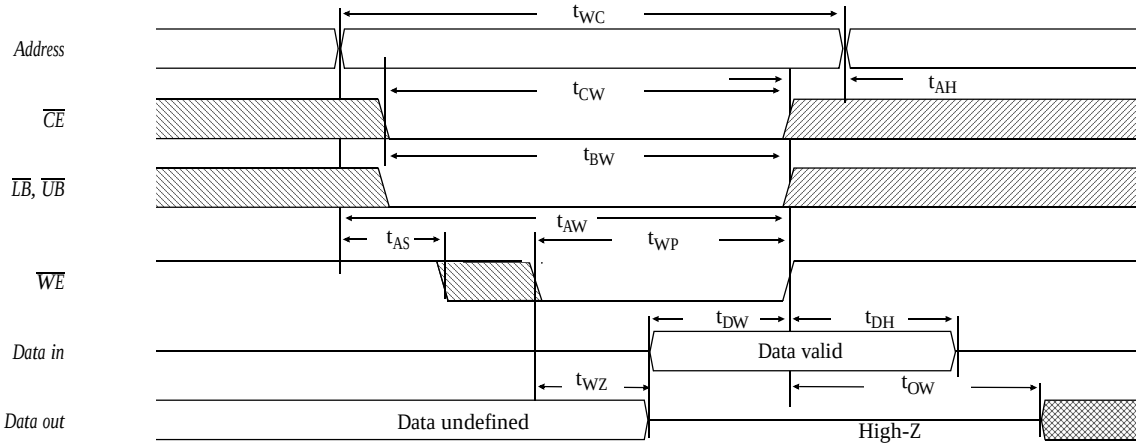


Write cycle [11]

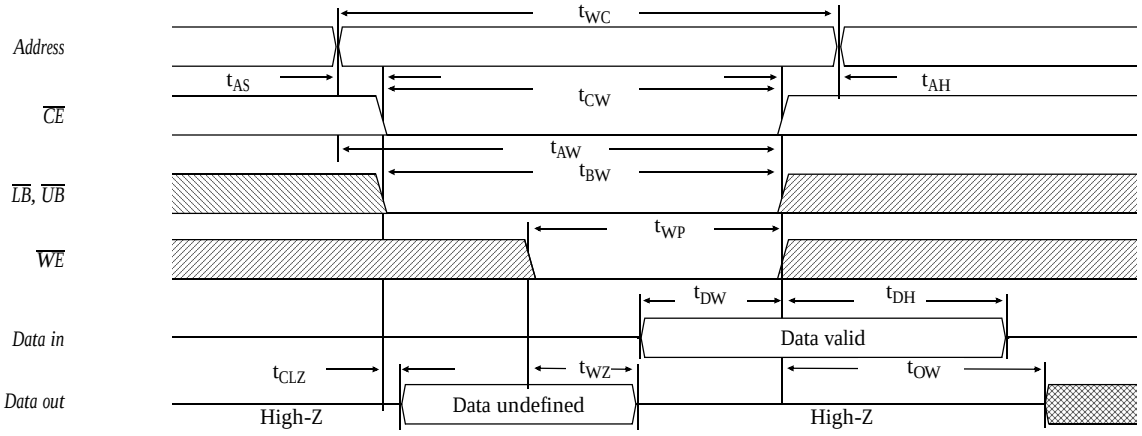
		-10		-12		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	8	–	9	–	10	–	13	–	ns	
Address setup to write end	t_{AW}	7	–	8	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	7	–	8	–	10	–	12	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	5
Write enable to output in High Z	t_{WZ}	–	5	–	6	–	6	–	8	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	ns	4, 5
Byte select Low to end of write	t_{BW}	7	–	9	–	9	–	12	–	ns	

Shaded areas indicate advance information.

Write waveform 1 [10,11]



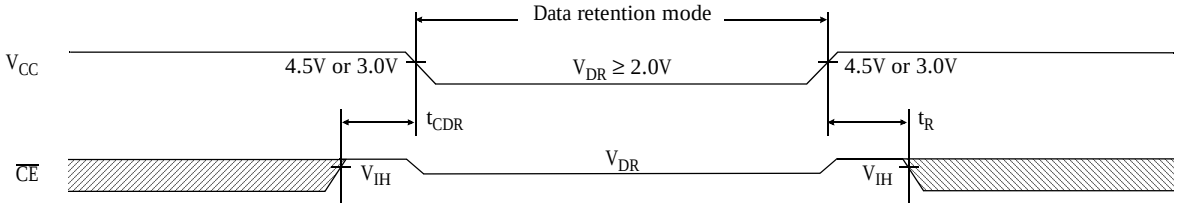
Write waveform 2 [10,11]



Data retention characteristics

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ *or* $V_{in} \leq 0.2V$	2.0	–	V
Data retention current	I_{CCDR}		–	500	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B, except as noted.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

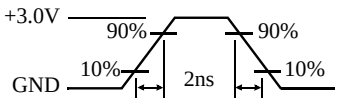


Figure A: Input pulse

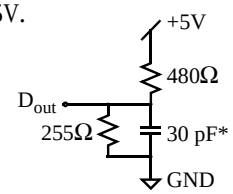


Figure B: Output load

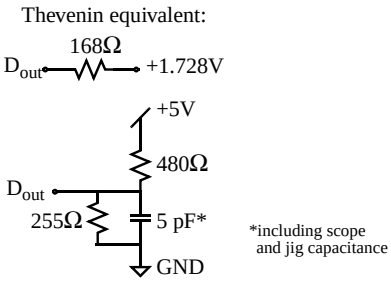


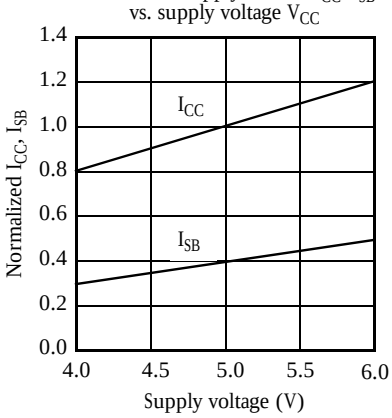
Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}

Notes

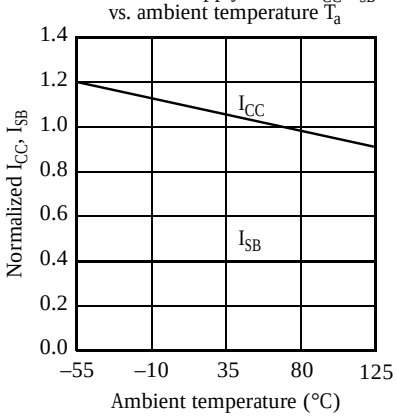
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 These parameters are specified with C_L = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.

Typical DC and AC characteristics

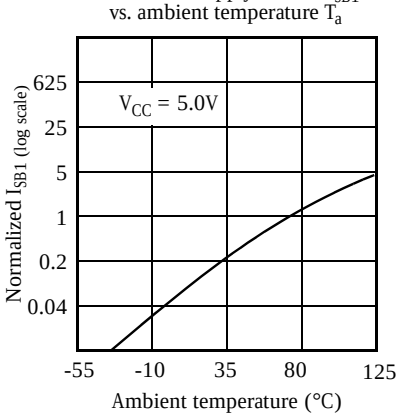
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



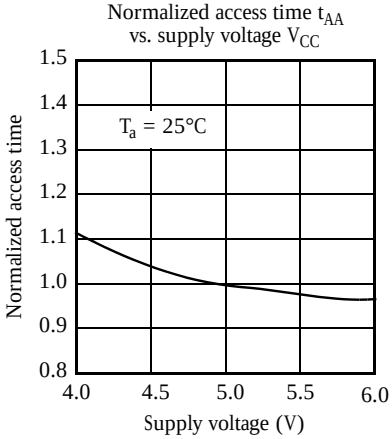
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



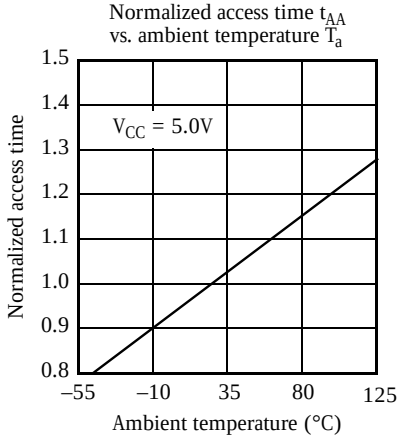
Normalized supply current I_{SB1} vs. ambient temperature T_a



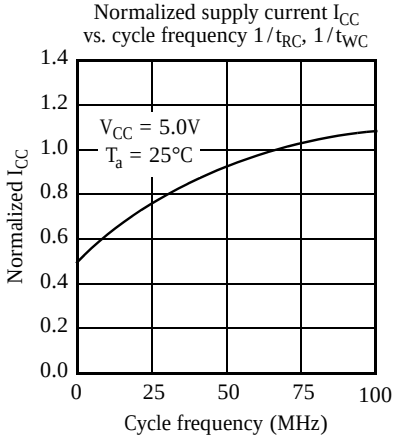
Normalized access time t_{AA} vs. supply voltage V_{CC}



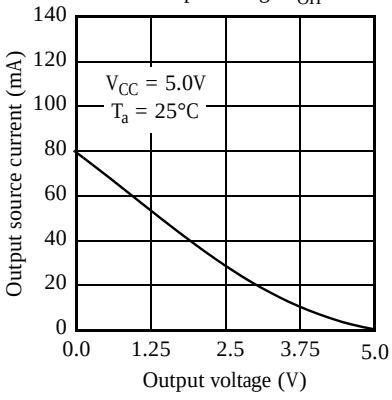
Normalized access time t_{AA} vs. ambient temperature T_a



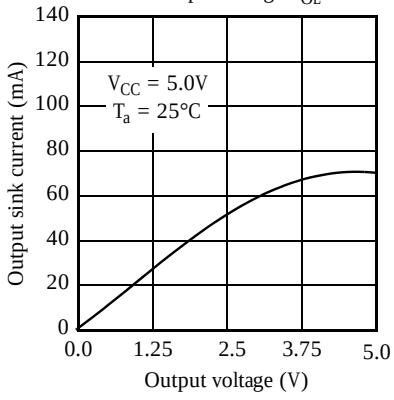
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



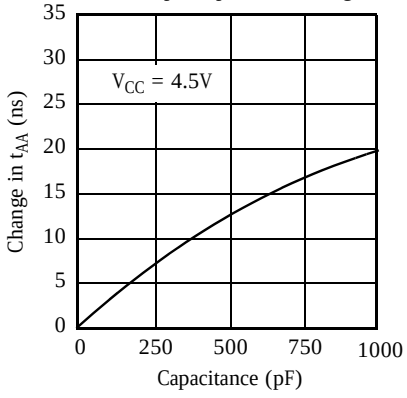
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}

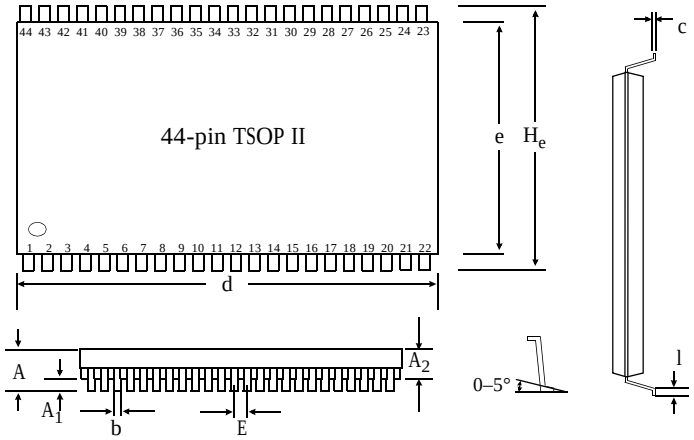


Typical access time change Δt_{AA} vs. output capacitive loading



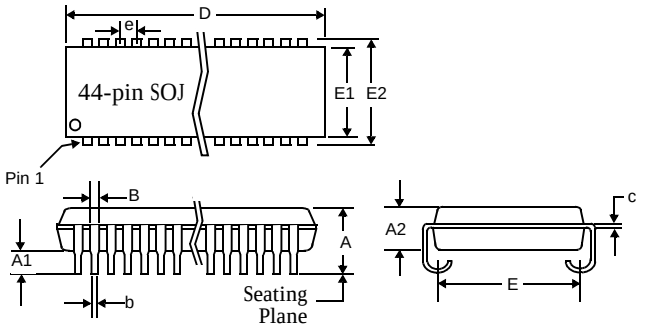
SRAM

Package dimensions



44-pin TSOP II

	Min (mm)	Max (mm)
A		1.2
A_1	0.05	
A_2	0.95	1.05
b	0.25	0.45
c	0.15 (typical)	
d	20.85	21.05
e	10.06	10.26
H_e	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60



44-pin SOJ
400 mil

	Min	Max
A	0.128	0.148
A1	0.025	-
A2	1.105	1.115
B	0.026	0.032
b	0.015	0.020
c	0.007	0.013
D	1.120	1.130
E	0.370 NOM	
E1	0.395	0.405
E2	*0.435*	*0.445*
e	*0.050 NOM*	

AS7C(3)513 ordering codes

Package \ Access time	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 400 mil	AS7C513-10JC AS7C3513-10JC	AS7C513-12JC AS7C3513-12JC	AS7C513-15JC AS7C3513-15JC	AS7C513-20JC AS7C3513-20JC
TSOP II, 18.4×10.2 mm	AS7C513-10TC AS7C3513-10TC	AS7C513-12TC AS7C3513-12TC	AS7C513-15TC AS7C3513-15TC	AS7C513-20TC AS7C3513-20TC

AS7C(3)513 part numbering system

AS7C	X	513	–XX	X	C
SRAM prefix	Voltage: Blank = 5V CMOS 3 = 3.3V CMOS	Device number	Access time	Package: J = SOJ 400 mil T = TSOP II, 18.4×10.2 mm	Commercial temperature range, 0°C to 70 °C