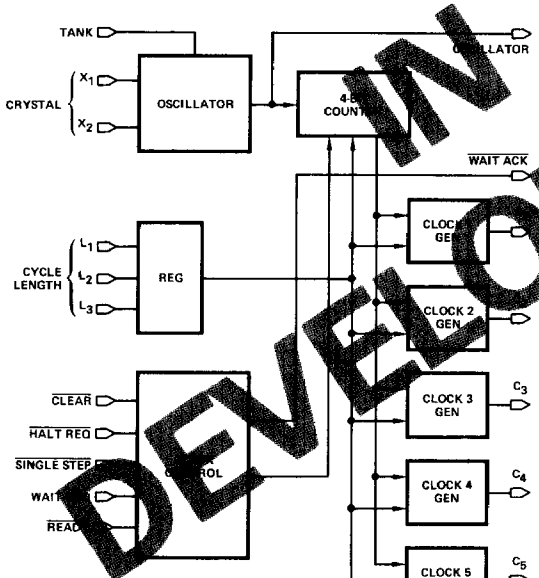
Am25LS2525

System Clock Generator and Driver

DISTINCTIVE CHARACTERISTICS

- Single chip clock generator and driver
- Five different clock output waveforms for Am2900 and other bipolar and MOS systems
- Crystal controlled for stable system operation
- Oscillator to 33MHz – oscillator output for external system timing
- Clock halt, single-step and wait controls
- Variable cycle lengths – 1-of-8 different cycle lengths may be programmed
- 20-Pin package
- 100% product assurance screening to MIL-STD-883 requirements

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

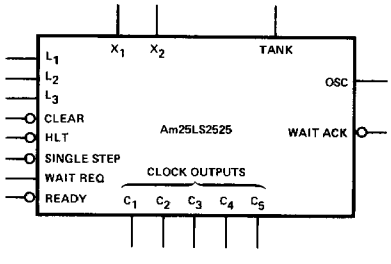
The Am25LS2525 is a single-chip general purpose clock generator/driver. It is controlled by a crystal, selected by the designer, and is microprogrammable to meet a variety of system speed requirements. The Am25LS2525 generates five different clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. Also, variable cycle lengths may be generated under microprogram control. One-of-eight different cycle lengths may be microprogrammed using the Cycle Length inputs L1, L2, and L3.

The Am25LS2525 oscillator runs at frequencies up to 33 MHz. An input pin is provided for a tank circuit which allows the use of overtone mode crystals. A buffered oscillator output is provided for external system timing.

Clock halt, single-step and wait controls are provided for the Am25LS2525. The HALT REQ input halts the clocks; the clocks resume when the HALT REQ input is deactivated. The SINGLE-STEP input, which operates only when the clocks are halted, generates the clocks for a single cycle. The WAIT REQ input stops the clocks and puts the Am25LS2525 in a "wait" state. In this state, the clocks remain stopped until an asynchronous WAIT input signal is received. The WAIT ACK output indicates when the Am25LS2525 is in the "wait" state. The WAIT REQ and READY inputs are pulse sensitive and are overridden by the HALT REQ input.

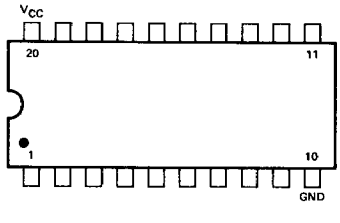
One of eight cycle lengths may be microprogrammed using the L1, L2, and L3 inputs. There are five clock output waveforms for each of the eight possible cycle lengths.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.