

# DATA SHEET

## **74LVT16374A**

**3.3V LVT 16-bit edge-triggered D-type  
flip-flop (3-State)**

Product data sheet  
Supersedes data of 2002 Nov 01

2004 Sep 16

## 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

### FEATURES

- 16-bit edge-triggered flip-flop
- 3-State buffers
- Output capability: +64 mA/−32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

### DESCRIPTION

The 74LVT16374A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is a 16-bit edge-triggered D-type flip-flop featuring non-inverting 3-State outputs. The device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ }^{\circ}\text{C}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nCP to nQx	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	2.9	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{ V}$ or $3.0\text{ V}$	3	pF
$C_{OUT}$	Output pin capacitance	Outputs disabled; $V_O = 0\text{ V}$ or $3.0\text{ V}$	9	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{ V}$	70	$\mu\text{A}$

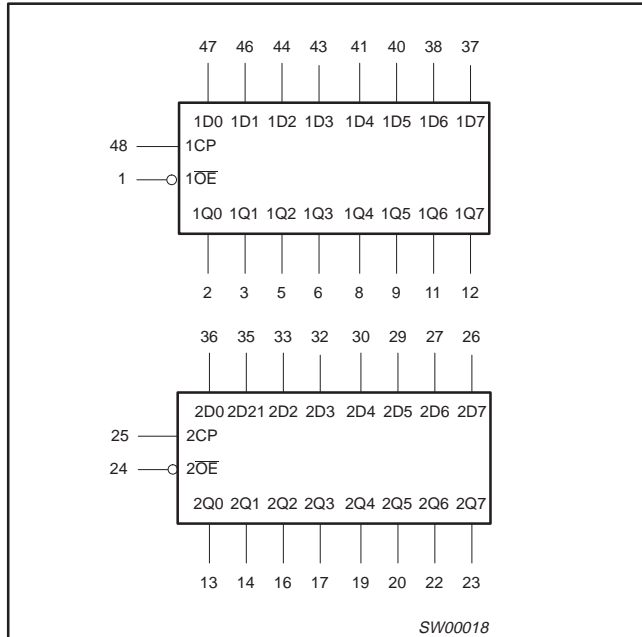
### ORDERING INFORMATION

Type number	Package		Temperature Range ( $^{\circ}\text{C}$ )	Version
	Name	Description		
74LVT16374ADL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	−40 to +85	SOT370-1
74LVT16374ADGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	−40 to +85	SOT362-1
74LVT16374AEV	VFPGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body $4.5 \times 7 \times 0.65\text{ mm}$	−40 to +85	SOT702-1

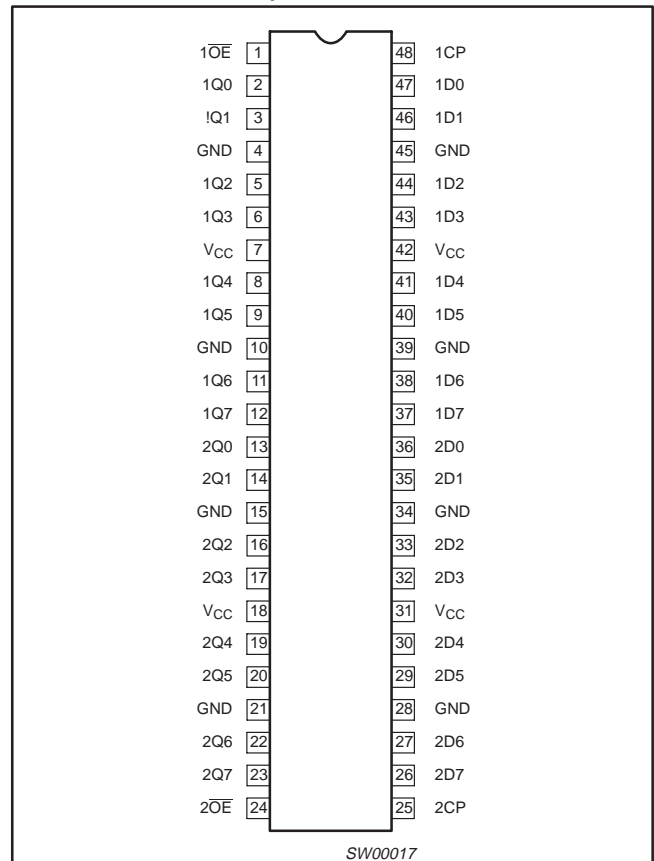
# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

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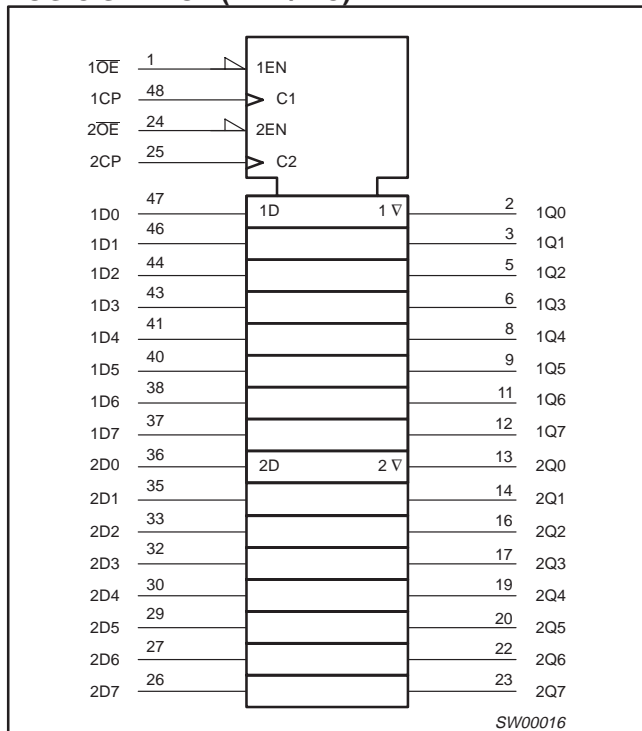
## LOGIC SYMBOL (SSOP AND TSSOP PACKAGES)



## PIN CONFIGURATION (SSOP AND TSSOP PACKAGE OPTIONS)



## LOGIC SYMBOL (IEEE/IEC)



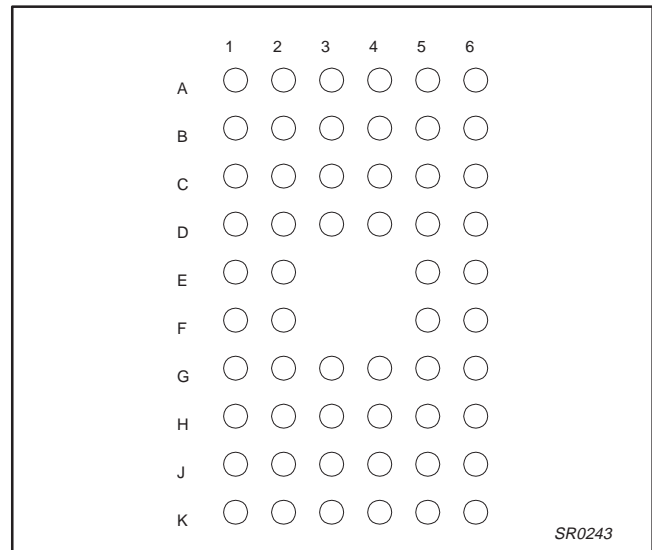
# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

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## PIN DESCRIPTION (SSOP AND TSSOP PACKAGE OPTIONS)

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 to 1D7 2D0 to 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 to 1Q7 2Q0 to 2Q7	Data outputs
1, 24	1 $\overline{OE}$ , 2 $\overline{OE}$	Output enable inputs (active-LOW)
48, 25	1CP, 2CP	Clock pulse inputs (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

## EV PACKAGE TERMINAL PLACEMENT, TOP VIEW



SR0243

## TERMINAL ASSIGNMENTS FOR 74LVT16374A IN VFBGA

	1	2	3	4	5	6
A	1 $\overline{OE}$	NC	NC	NC	NC	1CP
B	1Q1	1Q0	GND	GND	1D0	1D1
C	1Q3	1Q2	V <sub>CC</sub>	V <sub>CC</sub>	1D2	1D3
D	1Q5	1Q4	GND	GND	1D4	1D5
E	1Q7	1Q6			1D6	1D7
F	2Q0	2Q1			2D1	2D0
G	2Q2	2Q3	GND	GND	2D3	2D2
H	2Q4	2Q5	V <sub>CC</sub>	V <sub>CC</sub>	2D5	2D4
J	2Q6	2Q7	GND	GND	2D7	2D6
K	2 $\overline{OE}$	NC	NC	NC	NC	2CP

## FUNCTION TABLE

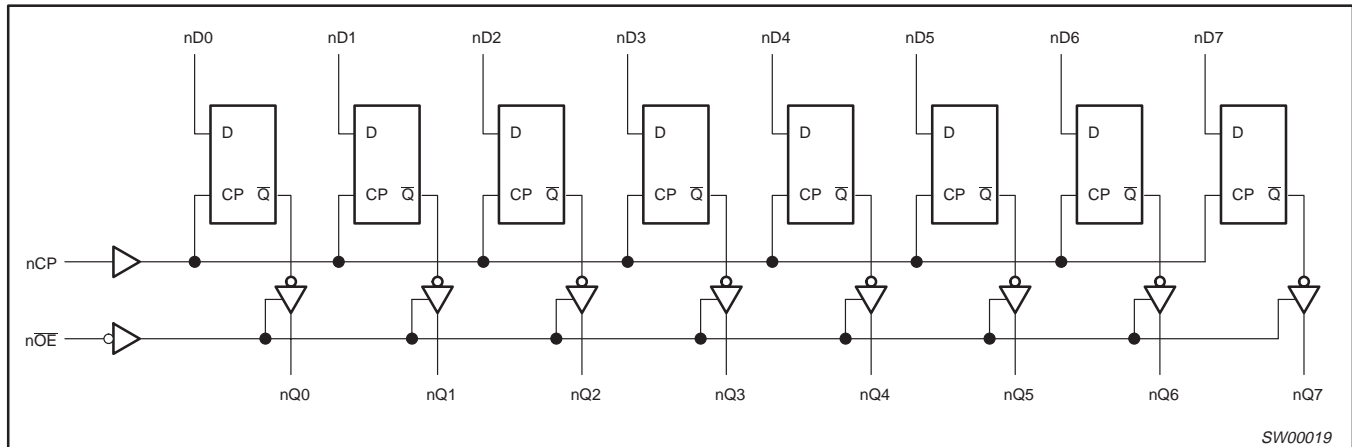
INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
n $\overline{OE}$	nCP	nDx		nQ0 to nQ7	
L L	$\uparrow$ $\uparrow$	l h	L H	L H	Load and read register
L	$\uparrow$	X	NC	NC	Hold
H H	$\uparrow$ $\uparrow$	X nDx	NC nDx	Z Z	Disable outputs

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the HIGH-to-LOW E transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition
- NC = No change
- X = Don't care
- Z = High-impedance "off" state
- $\uparrow$  = LOW-to-HIGH clock transition
- $\uparrow$  = Not a LOW-to-HIGH clock transition

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$ V	-50	mA
$V_I$	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$ V	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	Output in Off or HIGH state	-0.5 to +7.0	V
$I_{OUT}$	DC output current	Output in LOW state	128	mA
		Output in HIGH state	-64	
$T_{stg}$	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	2.7	3.6	V
$V_I$	Input voltage	0	5.5	V
$V_{IH}$	HIGH-level input voltage	2.0		V
$V_{IL}$	Input voltage		0.8	V
$I_{OH}$	HIGH-level output current		-32	mA
$I_{OL}$	LOW-level output current		32	mA
	LOW-level output current; current duty cycle $\leq 50$ %; $f \geq 1$ kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40 °C to +85 °C			
			MIN	TYP <sup>1</sup>	MAX	
$V_{IK}$	Input clamp voltage	$V_{CC} = 2.7 \text{ V}; I_{IK} = -18 \text{ mA}$		-0.85	-1.2	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7 \text{ to } 3.6 \text{ V}; I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$	$V_{CC}$		V
		$V_{CC} = 2.7 \text{ V}; I_{OH} = -8 \text{ mA}$	2.4	2.5		
		$V_{CC} = 3.0 \text{ V}; I_{OH} = -32 \text{ mA}$	2.0	2.3		
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7 \text{ V}; I_{OL} = 100 \mu\text{A}$		0.07	0.2	V
		$V_{CC} = 2.7 \text{ V}; I_{OL} = 24 \text{ mA}$		0.3	0.5	
		$V_{CC} = 3.0 \text{ V}; I_{OL} = 16 \text{ mA}$		0.25	0.4	
		$V_{CC} = 3.0 \text{ V}; I_{OL} = 32 \text{ mA}$		0.3	0.5	
		$V_{CC} = 3.0 \text{ V}; I_{OL} = 64 \text{ mA}$		0.4	0.55	
$V_{RST}$	Power-up output LOW voltage <sup>5</sup>	$V_{CC} = 3.6 \text{ V}; I_O = 1 \text{ mA}; V_I = \text{GND or } V_{CC}$		0.1	0.55	V
$I_I$	Input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or } \text{GND}$ Control pins		0.1	$\pm 1$	$\mu\text{A}$
		$V_{CC} = 0 \text{ V or } 3.6 \text{ V}; V_I = 5.5 \text{ V}$		0.4	10	
		$V_{CC} = 3.6 \text{ V}; V_I = V_{CC}$ Data pins <sup>4</sup>		0.1	1	
		$V_{CC} = 3.6 \text{ V}; V_I = 0 \text{ V}$		-0.4	-5	
$I_{OFF}$	Output off current	$V_{CC} = 0 \text{ V}; V_I \text{ or } V_O = 0 \text{ V to } 4.5 \text{ V}$		0.1	$\pm 100$	$\mu\text{A}$
$I_{HOLD}$	Bus Hold current D inputs <sup>7</sup>	$V_{CC} = 3 \text{ V}; V_I = 0.8 \text{ V}$	75	135		$\mu\text{A}$
		$V_{CC} = 3 \text{ V}; V_I = 2.0 \text{ V}$	-75	-135		
		$V_{CC} = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 3.6 \text{ V}$	$\pm 500$			
$I_{EX}$	Current into an output in the HIGH state when $V_O > V_{CC}$	$V_O = 5.5 \text{ V}; V_{CC} = 3.0 \text{ V}$		50	125	$\mu\text{A}$
$I_{PU/PD}$	Power up/down 3-State output current <sup>3</sup>	$V_{CC} \leq 1.2 \text{ V}; V_O = 0.5 \text{ V to } V_{CC}; V_I = \text{GND or } V_{CC}; \text{OE/OE} = \text{Don't care}$		1	$\pm 100$	$\mu\text{A}$
$I_{OZH}$	3-State output HIGH current	$V_{CC} = 3.6 \text{ V}; V_O = 3.0 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}$		0.5	5	$\mu\text{A}$
$I_{OZL}$	3-State output LOW current	$V_{CC} = 3.6 \text{ V}; V_O = 0.5 \text{ V}; V_I = V_{IH} \text{ or } V_{IL}$		0.5	-5	
$I_{CCH}$	Quiescent supply current	$V_{CC} = 3.6 \text{ V}; \text{Outputs HIGH, } V_I = \text{GND or } V_{CC}, I_O = 0 \text{ mA}$		0.07	0.12	mA
$I_{CCL}$		$V_{CC} = 3.6 \text{ V}; \text{Outputs LOW, } V_I = \text{GND or } V_{CC}, I_O = 0 \text{ mA}$		4	6	
$I_{CCZ}$		$V_{CC} = 3.6 \text{ V}; \text{Outputs Disabled; } V_I = \text{GND or } V_{CC}; I_O = 0 \text{ mA}^6$		0.07	0.12	
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}; \text{One input at } V_{CC} - 0.6 \text{ V}, \text{Other inputs at } V_{CC} \text{ or } \text{GND}$		0.1	0.2	mA

### NOTES:

- All typical values are at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .
- This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.
- This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10msec. From  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  a transition time of 100  $\mu\text{sec}$  is permitted. This parameter is valid for  $T_{amb} = 25 \text{ }^\circ\text{C}$  only.
- Unused pins at  $V_{CC}$  or GND.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- $I_{CCZ}$  is measured with outputs pulled to  $V_{CC}$  or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

## AC CHARACTERISTICS

GND = 0 V;  $t_R = t_F = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40$  °C to  $+85$  °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$		
			MIN	TYP <sup>1</sup>	MAX	MAX	
$f_{max}$	Maximum clock frequency	1	150				MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay nCP to nQx	1	1.5 1.5	2.9 3.0	5.0 5.0	5.6 5.6	ns
$t_{PZH}$ $t_{PZL}$	Output enable time to HIGH and LOW level	3 4	1.5 1.5	3.2 3.0	4.8 4.6	6.0 5.2	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time from HIGH and LOW Level	3 4	1.5 1.5	3.9 3.4	5.4 4.6	6.0 5.0	ns

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C.

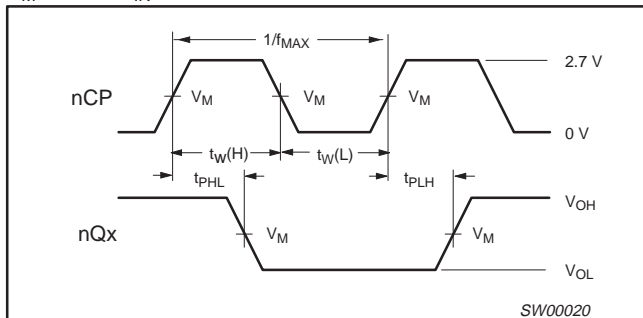
## AC SETUP REQUIREMENTS

GND = 0 V;  $t_R = t_F = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40$  °C to  $+85$  °C.

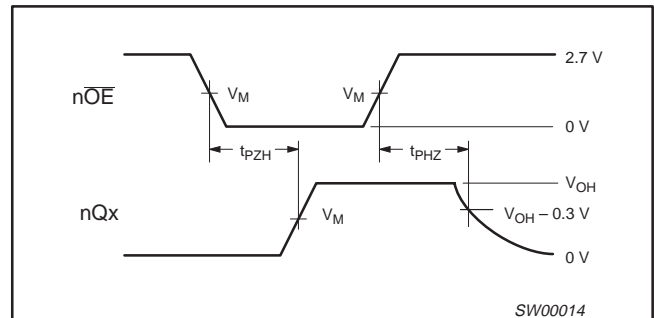
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3 V \pm 0.3 V$		$V_{CC} = 2.7 V$	
			MIN	TYP	MIN	
$t_{S(H)}$ $t_{S(L)}$	Setup time nDx to nCP	2	2.0 2.0	0.7 0.7	2.0 2.0	ns
$t_{H(H)}$ $t_{H(L)}$	Hold time nDx to nCP	2	0.8 0.8	0 0	0.1 0.1	ns
$t_{W(H)}$ $t_{W(L)}$	nCP pulse width HIGH or LOW	1	1.5 3.0	0.6 1.6	1.5 3.0	ns

## AC WAVEFORMS

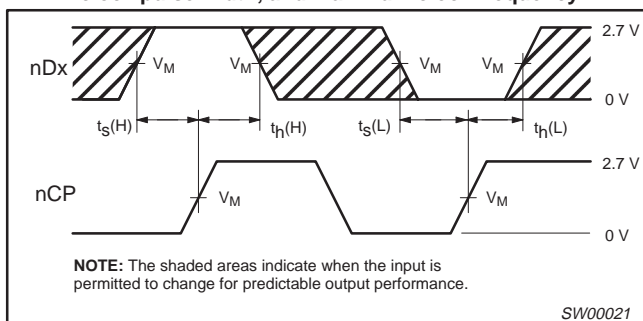
$V_M = 1.5$  V,  $V_{IN} =$  GND to 3.0 V



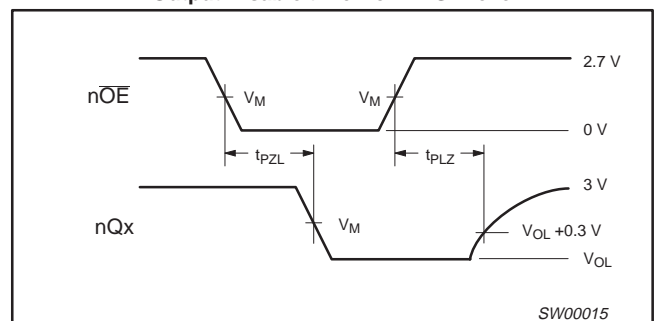
Waveform 1. Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



Waveform 3. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level



Waveform 2. Data setup and hold times

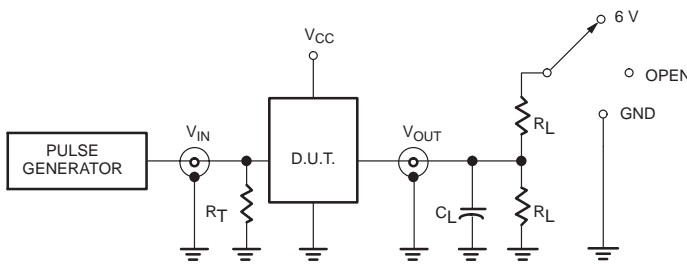


Waveform 4. 3-State Output Enable time to LOW level and Output Disable time from LOW level

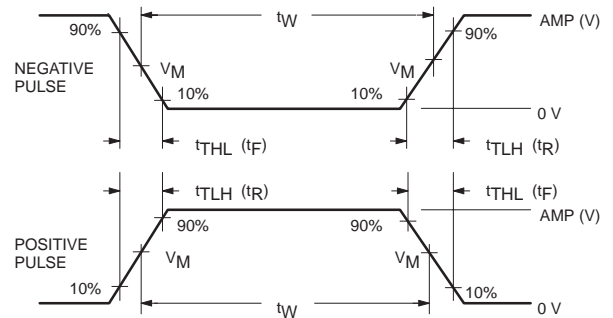
# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

## TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



$V_M = 1.5\text{ V}$   
Input Pulse Definition

### SWITCH POSITION

TEST	SWITCH
$t_{PHZ}/t_{PZH}$	GND
$t_{PLZ}/t_{PZL}$	6 V
$t_{PLH}/t_{PHL}$	open

### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74LVT16	2.7 V	$\leq 10\text{ MHz}$	500 ns	$\leq 2.5\text{ ns}$	$\leq 2.5\text{ ns}$

SW00003

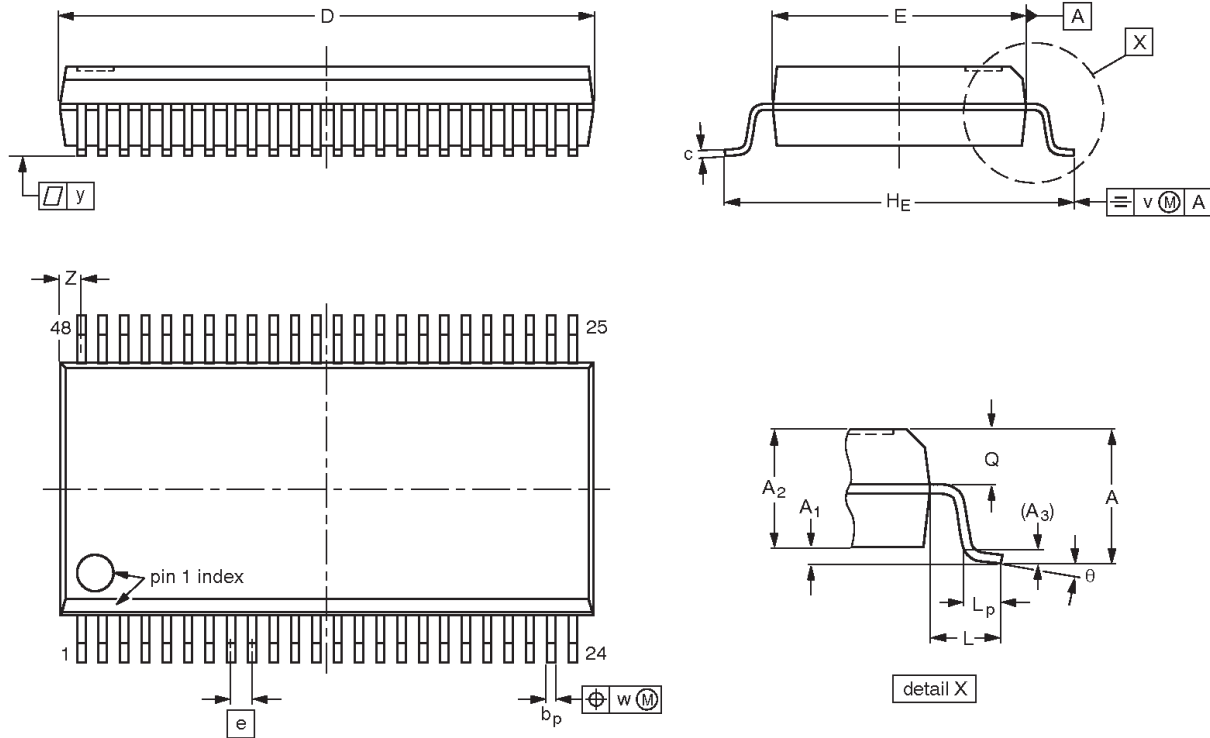


# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

**SSOP48:** plastic shrink small outline package; 48 leads; body width 7.5 mm

**SOT370-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

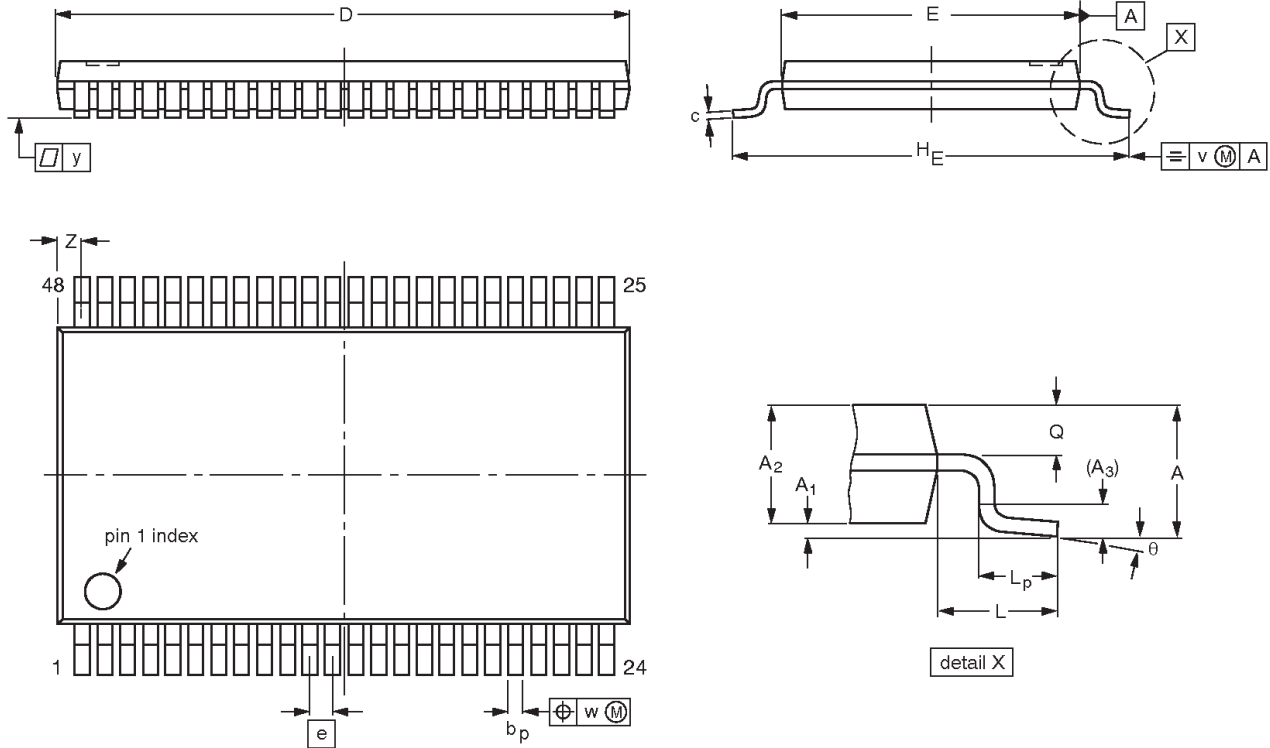
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

**TSSOP48:** plastic thin shrink small outline package; 48 leads; body width 6.1 mm

**SOT362-1**



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

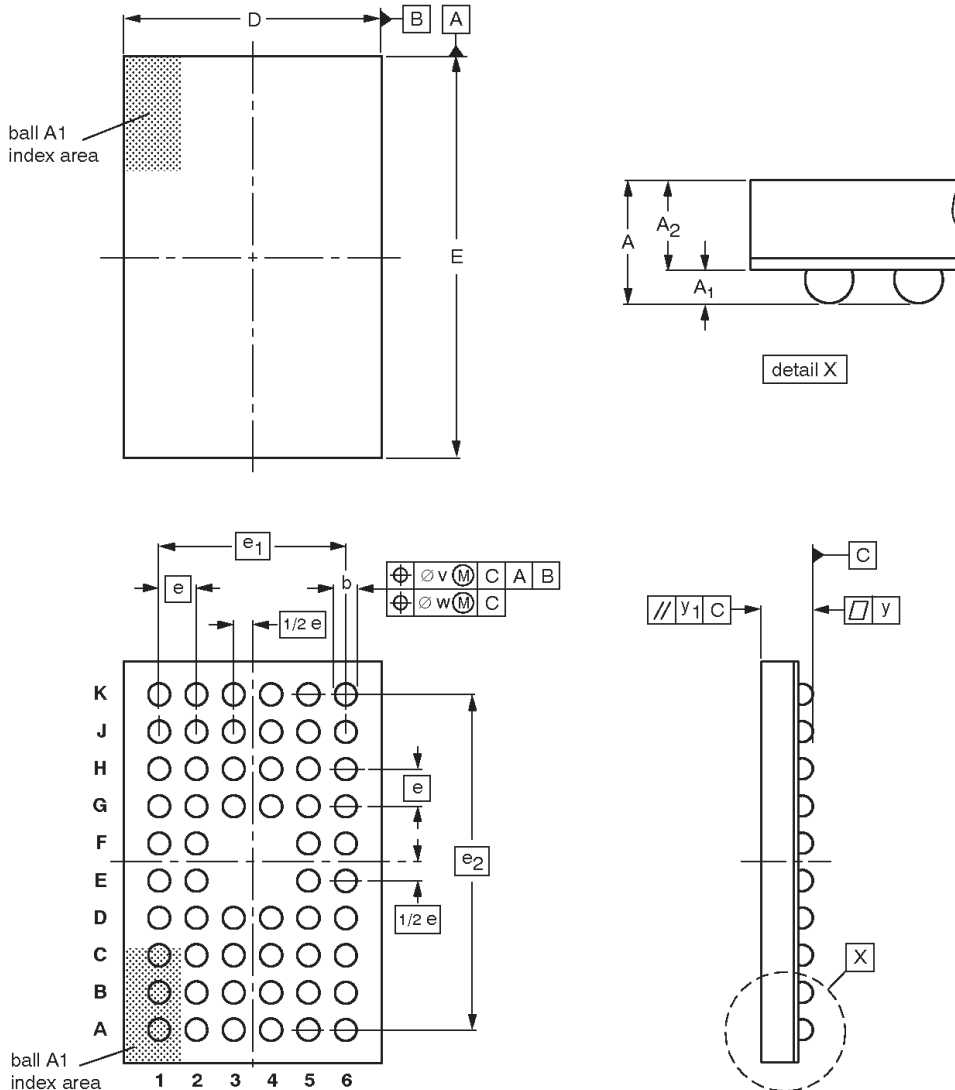
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-99-12-27 03-02-19

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

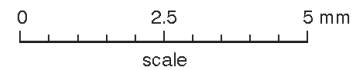
**VFPGA56:** plastic very thin fine-pitch ball grid array package; 56 balls;  
body 4.5 x 7 x 0.65 mm

**SOT702-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y	y <sub>1</sub>
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				02-08-08 03-07-01

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

## REVISION HISTORY

Rev	Date	Description
_5	20040916	Product data sheet (9397 750 14077). Supersedes data of 2002 Nov 01 (9397 750 10649). Modifications: <ul style="list-style-type: none"> <li>● AC Setup Requirements table on page 7: <ul style="list-style-type: none"> <li>– <math>V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}</math> change <math>t_s(H)</math> and <math>t_s(L)</math> setup time nDx to nCP Min. from 2.5 ns to 2.0 ns change <math>t_h(H)</math> and <math>t_h(L)</math> hold time nDx to nCP Min. from 0.5 ns to 0.8 ns</li> <li>– <math>V_{CC} = 2.7\text{ V}</math> change <math>t_s(H)</math> and <math>t_s(L)</math> setup time nDx to nCP Min. from 2.5 ns to 2.0 ns change <math>t_h(H)</math> and <math>t_h(L)</math> hold time nDx to nCP Min. from 0 ns to 0.1 ns</li> </ul> </li> </ul>
_4	20021101	<b>Product data (9397 750 10649); supersedes Product specification 74LVT16374A_3 of 1999 Oct 18 (9397 750 06514)</b> Engineering Change Notice 853–1781 29140 (date: 20021101)

# 3.3V 16-bit edge-triggered D-type flip-flop (3-State)

74LVT16374A

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Date of release: 09-04

For sales offices addresses send e-mail to:  
[sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com)

Document number:

9397 750 14077

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