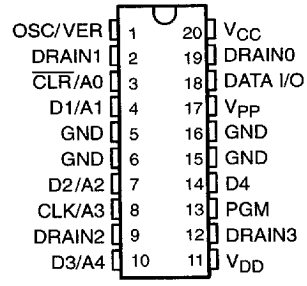
- **Programmable-PWM Current Threshold**
- **Programmable-PWM Frequency Controlled by Internal or External Oscillator**
- **Integrated Output Recirculation Clamp Diodes**
- **Low $r_{DS(on)}$ . . . 1 Ω Typ**
- **Four Power MOSFET Outputs**
- **Integrated Snubbing Clamp Voltage at 40 V**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



description

The power logic quad D-type latch pulse-width-modulation (PWM) driver controls open-drain DMOS transistor outputs and is designed for applications that require relatively high power. The device contains a built-in snubbing clamp and recirculation clamp on the outputs for inductive transient protection and inductive energy recirculation respectively. Power driver applications include solenoids and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent user-programmable PWM circuit that works in conjunction with the recirculation clamping diode in order to control the average current in inductive-load applications. The PWM circuit provides a programmable current-limit threshold that disables the output until the next rising edge of the independent PWM programmable clock. Each clock is generated from a user-programmable internal or external clock reference that in turn is programmed independently for each output through a frequency divide-by circuit.

TERMINAL NOMENCLATURE	
OSC/VER	Oscillator/Verify
DRAIN0 – DRAIN3	Drain Output 0 to 3
CLR/A0	Clear/Address 0
D1/A1	Data 1/Address 1
GND	Ground
D2/A2	Data 2/Address 2
D3/A4	Data 3/Address 4
D4	Data 4
V_{CC}	Logic Supply Voltage
DATA I/O	Program Data Input/Output
V_{PP}	Programming Supply Voltage
PGM	Program Enable
V_{DD}	Output Supply Voltage
CLK/A3	Clock/Address 3

FUNCTION TABLE
(each channel)

INPUTS			OUTPUT DRAIN
CLR	CLK	D	
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

User-programmable functions are controlled through 32 EEPROM bits. These bits are programmed by placing the TPIC6E175 into program mode by taking PGM high. The address to be programmed is then set up on dual functionality terminals A0–A4 (see Tables 1 and 2). The data bit to be programmed is set up on DATA I/O, and V_{PP} is then ramped from V_{CC} to V_{PPH} and back to V_{CC} to program the bit. The programming data can then be verified by taking VER high while monitoring DATA I/O, which gives the value of the data at the address selected on A0–A4. For each user-programmable parameter, Table 3 shows the binary programming values and the option selected by each programming value.

The TPIC6E175 contains four positive-edge-triggered D-type flip-flops with direct clear input. Each flip-flop features an open-drain power DMOS-transistor output.

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description (continued)

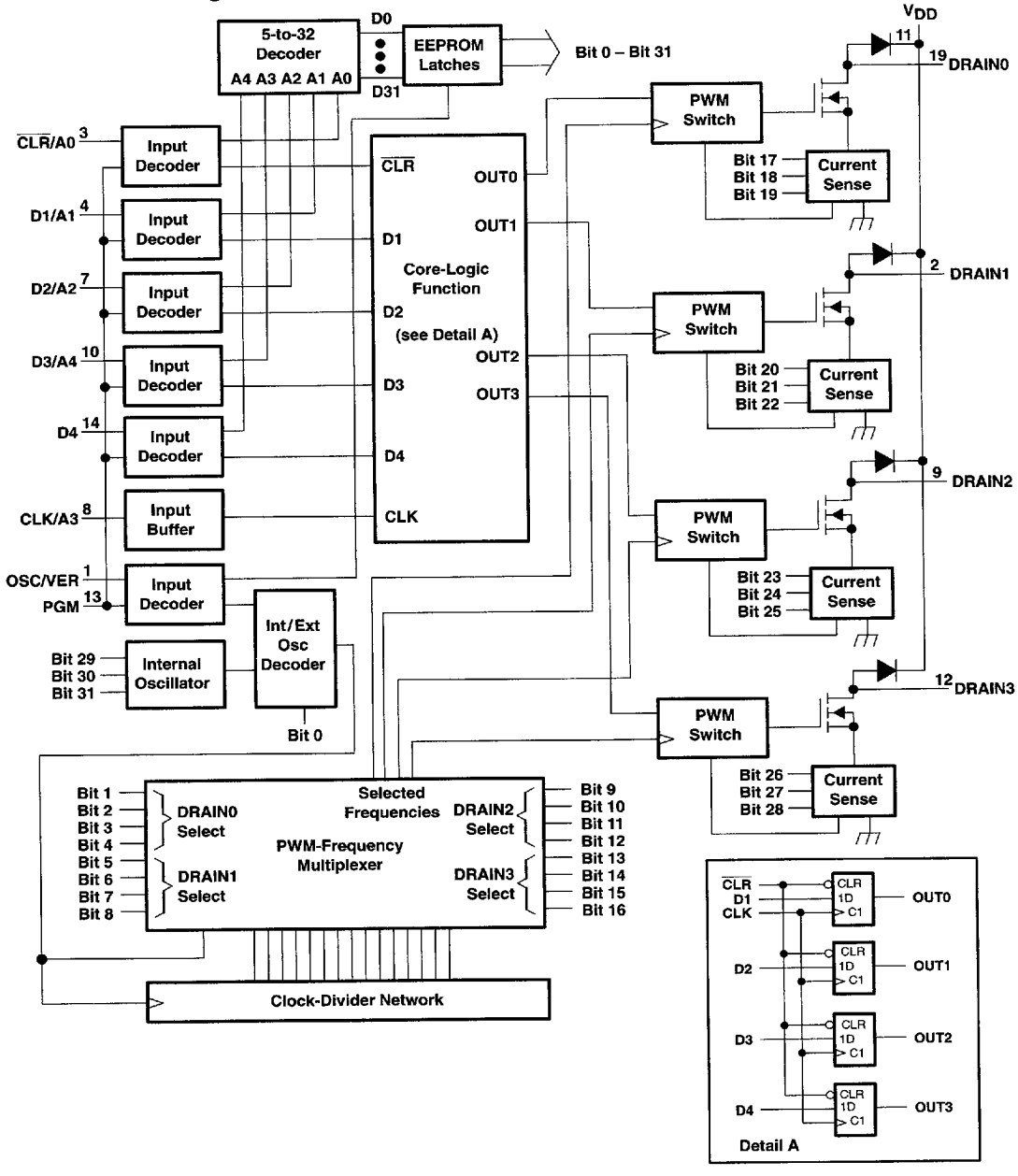
When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements, is transferred to the DRAIN outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all four DMOS-transistor outputs off. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

For proper operation, V_{DD} must be connected to a voltage source equal to or greater than the maximum drain voltage in the application.

The TPIC6E175 is offered in a 20-pin thermally-enhanced dual-in-line (NE) package and is characterized for operation over the operating case temperature range of –40°C to 125°C.

PRODUCT PREVIEW

functional block diagram



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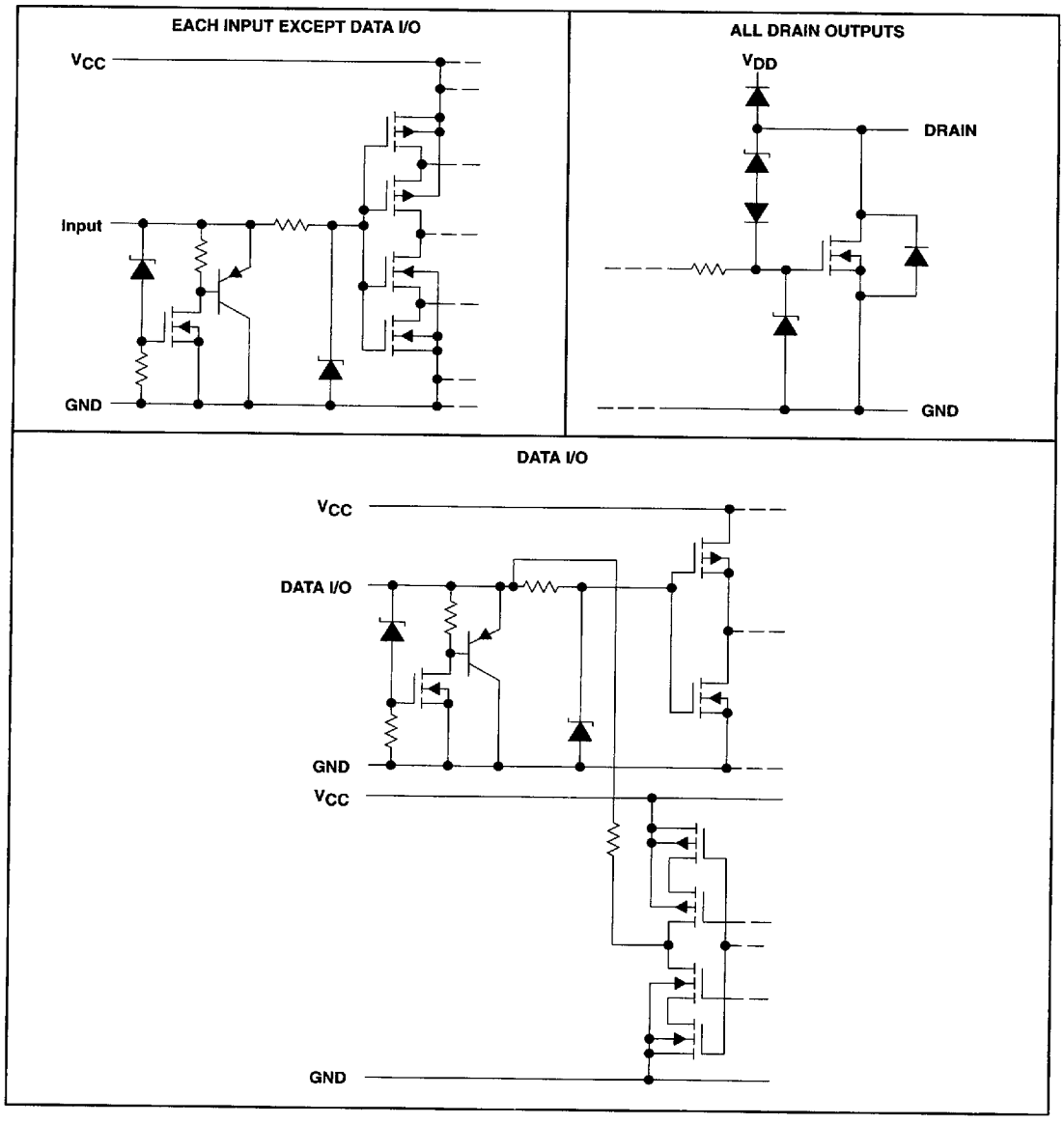
equivalent inputs and outputs



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DATA I/O	18	I/O	Programming data input/output
DRAIN0 DRAIN1 DRAIN2 DRAIN3	19 2 9 12	O	Drain outputs 0–3
D2/A2	7	I	Data 2 or Address 2
GND	5, 6, 15, 16	—	Ground
OSC/VER	1	I	Oscillator or Programming verify
PGM	13	I	Program enable
D3/A4	10	I	Data 3 or Address 4
$\overline{CLR}$/A0	3	I	Clear or Address 0
CLK/A3	8	O	Clock or Address 3
D1/A1	4	I	Data 1 or Address 1
D4	14	I	Data 4
V_{CC}	20	—	Logic supply voltage
V_{DD}	11	—	Output supply voltage
V_{PP}	17	—	Programming supply voltage

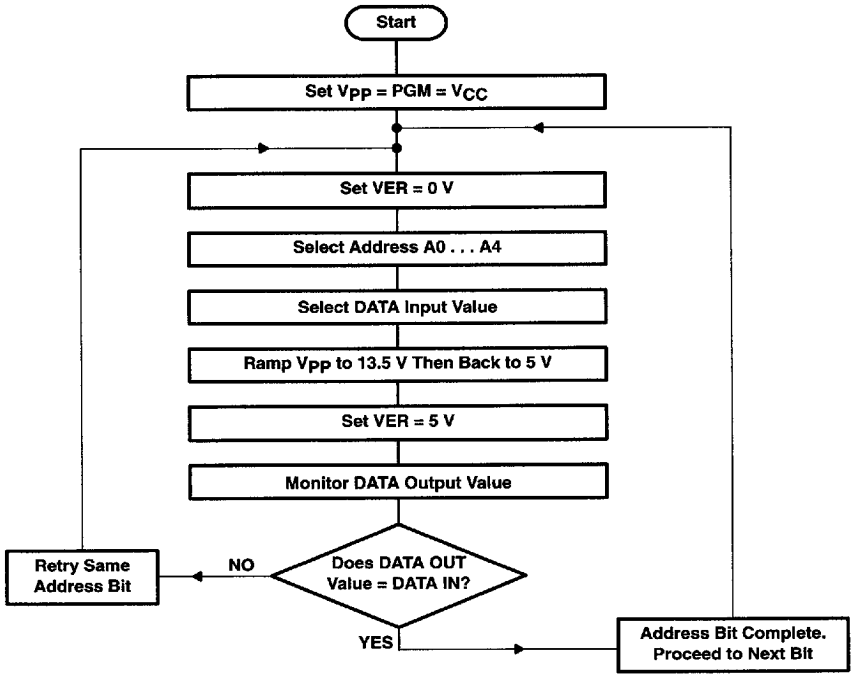

Figure 1. Recommended EEPROM Programming Sequence

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Table 1. Function Selection for Dual-Functionality Terminals

TERMINAL NUMBER	NORMAL MODE (PGM = L)	PROGRAM MODE (PGM = H)
1	OSC	VER
3	$\overline{CLR}$	A0
4	D1	A1
7	D2	A2
8	CLK	A3
10	D3	A4

H = high level, L = low level

Table 2. EEPROM Bit Description

BIT NO.	BIT ADDRESS	USER-PROGRAMMABLE PARAMETER	DESCRIPTION†
0	00000	Internal/External Oscillator	Selects internal or external oscillator to be used for PWM clock
1 (LSB)	00001	DRAIN0 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
2	00010		
3	00011		
4 (MSB)	00100		
5 (LSB)	00101	DRAIN1 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
6	00110		
7	00111		
8 (MSB)	01000		
9 (LSB)	01001	DRAIN2 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
10	01010		
11	01011		
12 (MSB)	01100		
13 (LSB)	01101	DRAIN3 Frequency Multiplexer	Selects PWM frequency based on internal/external clock frequency and the number of divide-by-2s chosen
14	01110		
15	01111		
16 (MSB)	10000		
17 (LSB)	10001	DRAIN0 Current Sense Adjust	Selects the peak current for the PWM-chop mode
18	10010		
19 (MSB)	10011		
20 (LSB)	10100	DRAIN1 Current Sense Adjust	Selects the peak current for the PWM-chop mode
21	10101		
22 (MSB)	10110		
23 (LSB)	10111	DRAIN2 Current Sense Adjust	Selects the peak current for the PWM-chop mode
24	11000		
25 (MSB)	11001		
26 (LSB)	11010	DRAIN3 Current Sense Adjust	Selects the peak current for the PWM-chop mode
27	11011		
28 (MSB)	11100		
29 (LSB)	11101	Oscillator Frequency Adjust	Selects the frequency of the internal oscillator
30	11110		
31 (MSB)	11111		

† See Table 3

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Table 3. EEPROM Programming Values

PROGRAMMABLE PARAMETER	OPTION SELECTED	BINARY VALUE MSB< . . . > LSB
Internal/External Oscillator	Internal Oscillator	0
	External Oscillator	1
Frequency Multiplexer for All Drain Outputs	Oscillator ÷ 1	0000
	Oscillator ÷ 2	0001
	Oscillator ÷ 4	0010
	Oscillator ÷ 8	0011
	Oscillator ÷ 16	0100
	Oscillator ÷ 32	0101
	Oscillator ÷ 64	0110
	Oscillator ÷ 128	0111
	Oscillator ÷ 256	1000
	Oscillator ÷ 512	1001
	Oscillator ÷ 1024	1010
	Oscillator ÷ 2048	1011
	Oscillator ÷ 4096	1100
	Oscillator ÷ 8192	1101
	Oscillator ÷ 16384	1110
	Oscillator ÷ 32768	1111
Current Sense Adjust for All Drain Outputs	300 mA†	000
	400 mA†	001
	500 mA†	010
	600 mA†	011
	700 mA†	100
	800 mA†	101
	900 mA†	110
	1000 mA†	111
Oscillator Frequency Adjust	Internal Oscillator, Frequency = 1.2 MHz	000
	Internal Oscillator, Frequency = 1.1 MHz	001
	Internal Oscillator, Frequency = 0.9 MHz	010
	Internal Oscillator, Frequency = 0.8 MHz	011
	Internal Oscillator, Frequency = 0.6 MHz	100
	Internal Oscillator, Frequency = 0.5 MHz	101
	Internal Oscillator, Frequency = 0.3 MHz	110
	Internal Oscillator, Frequency = 0.1 MHz	111

† Current target ±20%

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absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) ..... 7 V
Logic input voltage range, V_I ..... −0.3 V to 7 V
Output supply voltage, V_{DD} (see Note 1) ..... 40 V
Programming supply voltage during programming, V_{PP} (see Notes 1 and 2) ..... 16 V
Programming supply voltage, verify/normal operation, V_{PP} ..... 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 3) ..... 40 V
Continuous source-to-drain diode current ..... 1 A
Pulsed source-to-drain diode current (see Note 3) ..... 1 A
PWM output current, each output, all outputs on, $I_{O(PWM)}$, T_A = 25°C, d = 10% (see Note 4 and Figure 10) ..... 900 mA
PWM output current, each output, all outputs on, $I_{O(PWM)}$, T_A = 25°C, d = 50% (see Note 4 and Figure 9) ..... 800 mA
Peak drain current, single output, $I_{D(PWM)}$, T_A = 25°C (see Notes 3 and 4) ..... 1 A
Avalanche current, $I_{(av)}$ (see Note 5 and Figure 7) ..... 1 A
Single-pulse avalanche energy, E_A (see Note 5 and Figure 7) ..... 100 mJ
Continuous total power dissipation ..... See Dissipation Rating Table
Operating case temperature range, T_C ..... −40°C to 125°C
Operating virtual junction temperature range, T_J ..... −40°C to 150°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. For programming waveform, see Figure 2.
3. Each power DMOS source is internally connected to GND. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
4. Output current depends upon program current-sense adjust and load conditions.
5. V_{supply} = 24 V, starting junction temperature, (T_{JS}) = 25°C, L = 87 mH, I_{AS} = 1 A.

DISSIPATION RATING TABLE

PACKAGE	$T_C \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
NE	2775 mW	20 mW/°C	775 mW
NE on FR-4 PCB	4163 mW	33.3 mW/°C	833 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
Output supply voltage, V_{DD}		40	V
Programming supply voltage during programming, V_{PP}	12	15	V
Programming supply voltage during verify or normal operation, V_{PP}	V_{CC}−0.7	V_{CC}	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA			40			V
V_{SD}	Source-drain diode forward voltage	I_F = 1 A				1	1.5	V
$V_{OH(DATA\ I/O)}$	High-level data output voltage	I_{OH} = −100 µA,	V_{CC} = 4.5 V		4.25	4.48		V
$V_{OL(DATA\ I/O)}$	Low-level data output voltage	I_{OL} = 100 µA,	V_{CC} = 4.5 V			200	250	mV
V_f	Forward clamp voltage	I_f = 1 A				1.35	2	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0,	All inputs low			1.6	5	mA
$I_{CC(freq)}$	Logic supply current at frequency	SRCK = 5 MHz,	I_O = 0			5.5		mA
I_{DS}	Off-state drain current	V_{DD} = 40 V,	V_{DS} = 35 V			0.2	1	µA
		V_{DD} = 40 V,	V_{DS} = 30 V,	T_C = 125°C		1	5	
$r_{DS(on)}$	Static drain-to-source on-state resistance	I_D = 200 mA,	V_{CC} = 4.5 V			1	1.5	Ω
		I_D = 200 mA,	V_{CC} = 4.5 V,	T_C = 125°C		1.6	2.4	
		I_D = 750 mA,	V_{CC} = 4.5 V			1.1	1.75	

timing requirements over recommended ranges of supply voltage and operating case temperature

		MIN	MAX	UNIT
t_{su}	Setup time, D high before CLK↑ (see Figure 5)	20		ns
t_{su1}	Setup time, VER to PGM (see Figure 2)	2		µs
t_{su2}	Setup time, address and DATA I/O to V_{PP} (see Figure 2)	2		µs
t_{su3}	Setup time, PGM to DATA I/O (see Figure 2)	2		µs
t_{su4}	Setup time, PGM to address (see Figure 2)	2		µs
t_h	Hold time, D high before CLK↑ (see Figure 5)	20		ns
t_{h1}	PGM hold time, DATA I/O (see Figure 2)	2		µs
t_{h2}	Hold time, DATA I/O after V_{PP} (see Figure 2)	2		µs
t_w	Pulse duration (see Figure 5)	40		ns
t_{w1}	Pulse duration, V_{PP} program (see Figure 2)	5		ms
t_{pd}	Propagation delay, VER to DATA I/O (see Figure 2)	2		µs
t_r	Rise time, V_{PP} during programming (see Figure 2)	2	3	ms
t_f	Fall time, V_{PP} during programming (see Figure 2)	2	3	ms

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switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, See Figure 5	I_D = 250 mA,		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK				150		ns
t_{r1}	Rise time, drain output (see Figure 5)				750		ns
t_{f1}	Fall time, drain output (see Figure 5)				425		ns
t_{rr}	Reverse-recovery time (see Figure 6)	I_F = 250 mA,	di/dt = 40 A/µs		300		ns
t_{rra}	Reverse-recovery current rise time (see Figure 6)				100		ns

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All four outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All four outputs with equal power		50	°C/W

PARAMETER MEASUREMENT INFORMATION

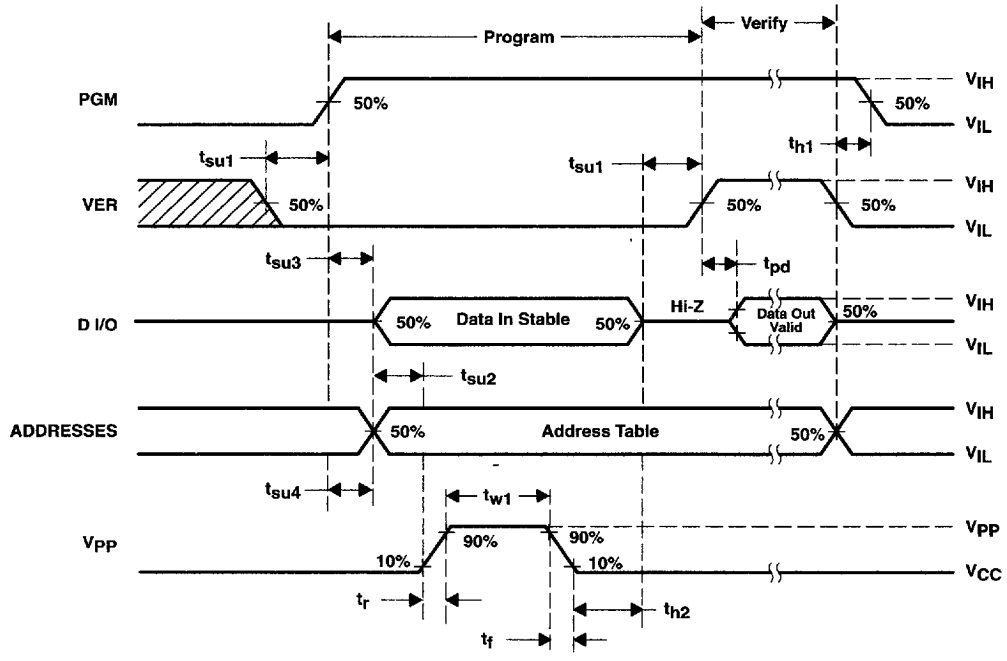

Figure 2. Programming Waveforms

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PARAMETER MEASUREMENT INFORMATION

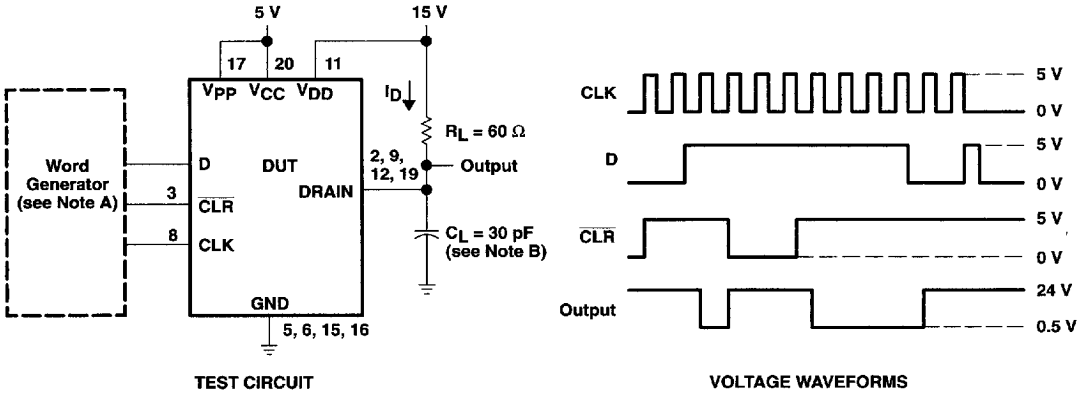

Figure 3. Resistive Load Operation

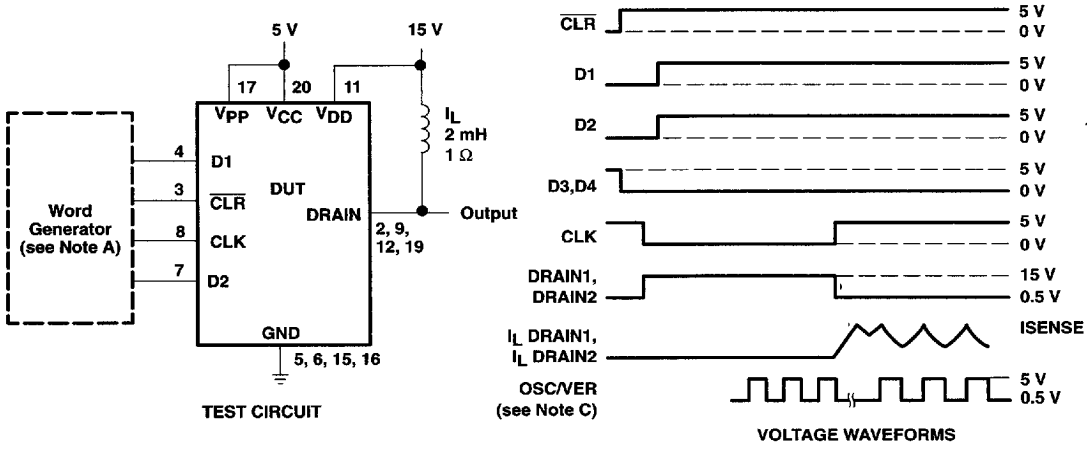

Figure 4. Inductor Load Operation

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. DRAIN0 and DRAIN3 remain at 0A I_L.

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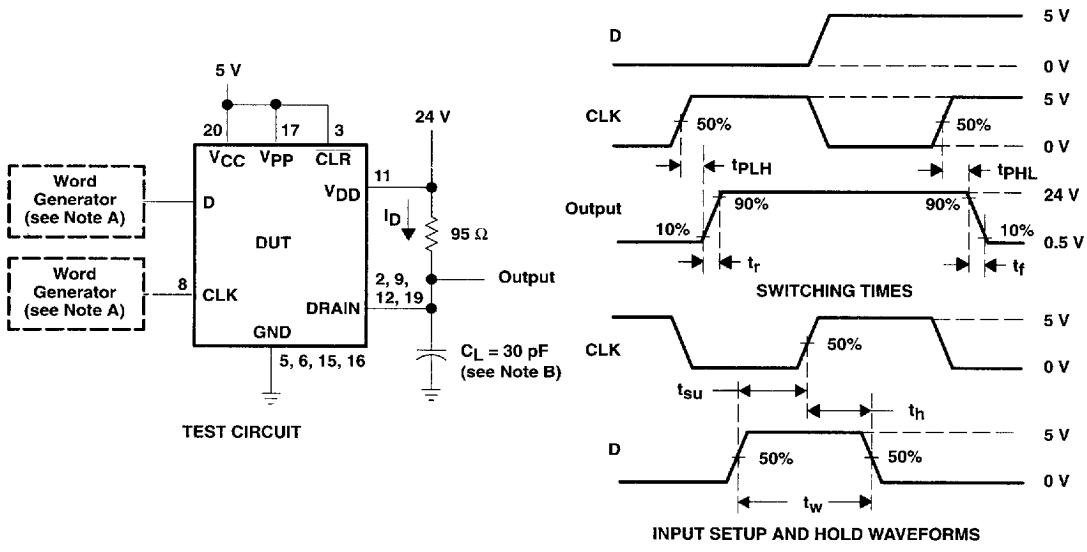
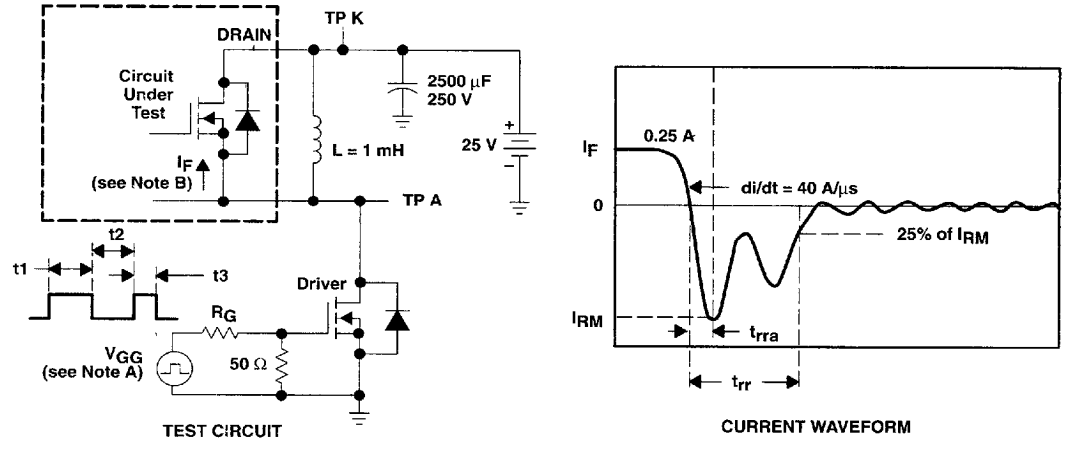
PARAMETER MEASUREMENT



NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance

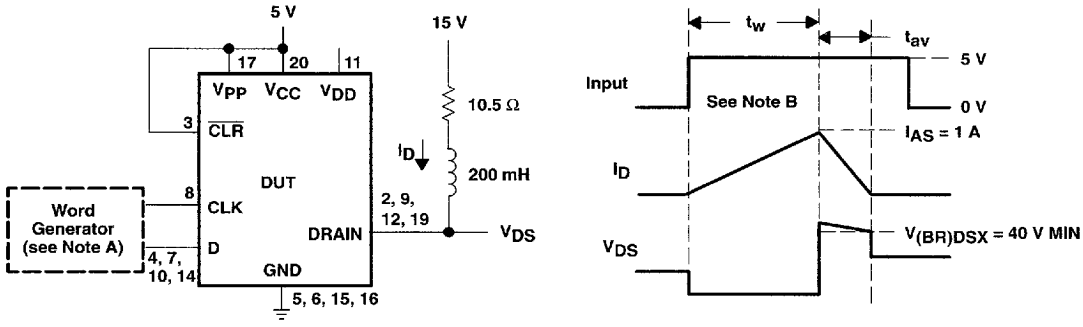
Figure 5. Test Circuit and Voltage Waveforms, Switching Times



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 40 A/µs. A V_{GG} double-pulse train sets I_F = 0.25 A, where t1 = 15 µs, t2 = 8.5 µs, and t3 = 3.5 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 6. Reverse-Recovery-Current Test Circuit and Waveform of Source Drive Device

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE-ENERGY TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$

B. Input pulse duration (t_w) is controlled by the value of peak current $I_{AS} = 1$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 100$ mJ,

where t_{av} = avalanche time

Figure 7. Single-Pulse Avalanche-Energy Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

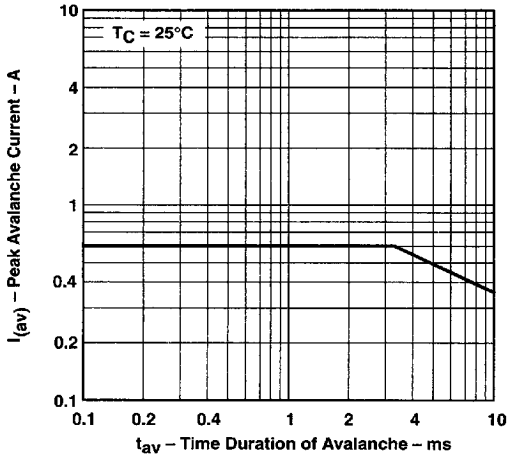


Figure 8

MAXIMUM PWM
CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

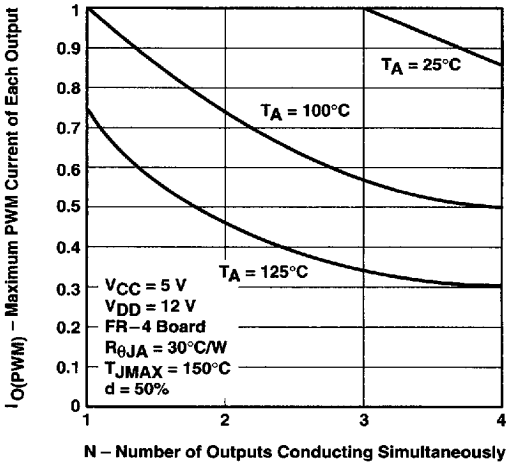


Figure 9

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

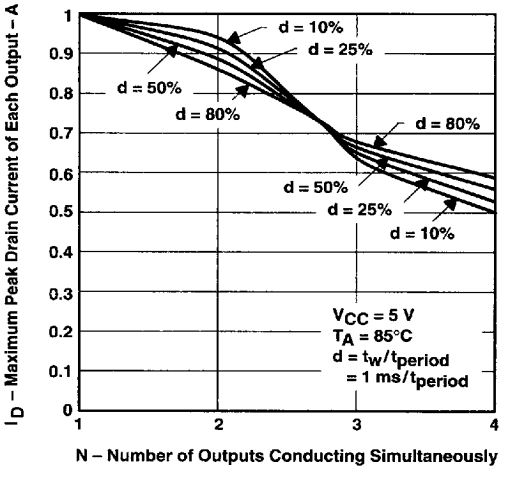
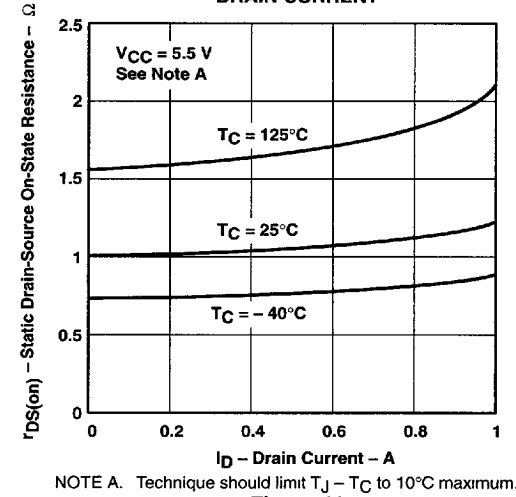


Figure 10

STATIC DRAIN-SOURCE
ON-STATE RESISTANCE
vs
DRAIN CURRENT



NOTE A. Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

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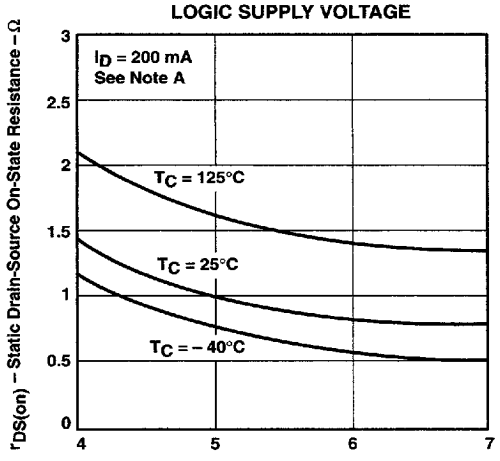
TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 12

SWITCHING TIME vs FREE-AIR TEMPERATURE

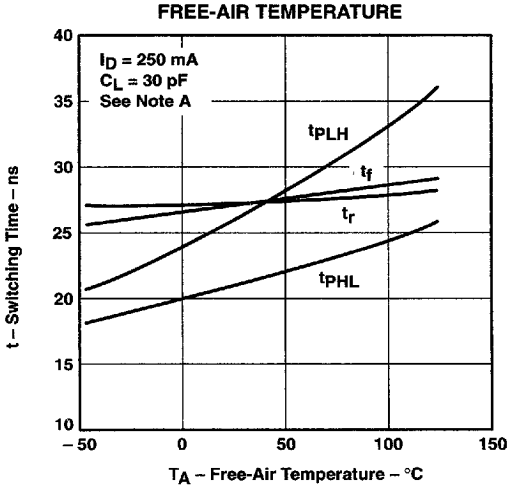


Figure 13

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