DESCRIPTION

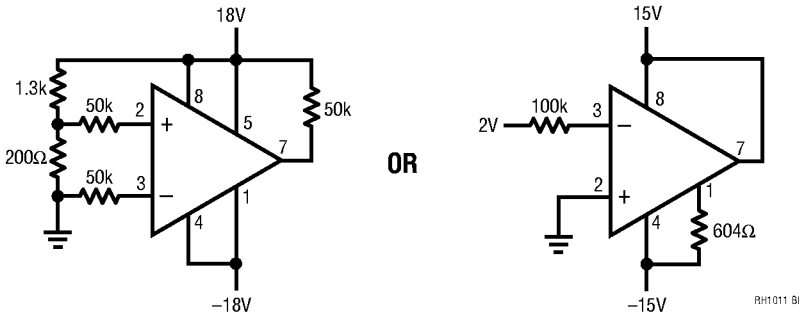
The RH1011 is a general purpose comparator with significantly better input characteristics than the LM111. Although pin compatible with the LM111, it offers four times lower bias current, six times lower offset voltage and five times higher voltage gain.

The wafer lots are processed to Linear Technology's in-house Class S flow to yield circuits usable in stringent military applications.

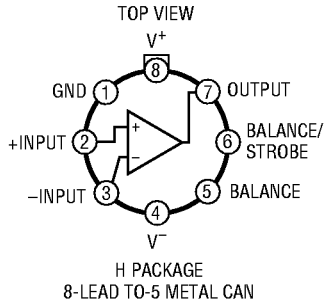
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 8 to Pin 4) 36V
Output to Negative Supply (Pin 7 to Pin 4) 35V
Ground to Negative Supply (Pin 1 to Pin 4) 30V
Differential Input Voltage ..... ±35V
Voltage at STROBE Pin (Pin 6 to Pin 8) 5V
Input Voltage (Note 1) ..... Equal to Supplies
Output Short-Circuit Duration ..... 10 sec
Operating Temperature Range
(Note 2) ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

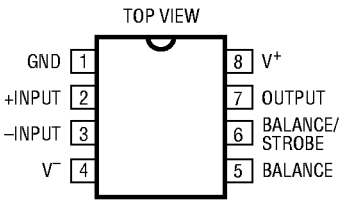
BURN-IN CIRCUIT



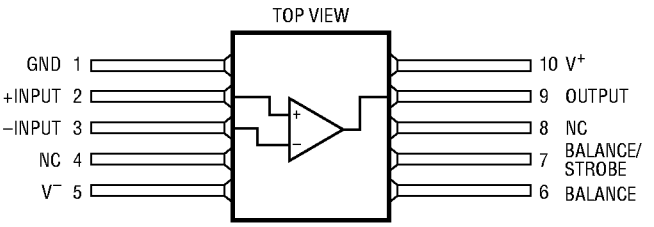
PACKAGE INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN



J8 PACKAGE
8-LEAD CERDIP



W PACKAGE
10-LEAD CERPAC

TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 10)

SYMBOL	PARAMETER	CONDITIONS	NOTES	T_A = 25°C MIN	TYP	MAX	SUB-GROUP	−55°C T_A 125°C MIN	TYP	MAX	SUB-GROUP	UNITS
V_{OS}	Input Offset Voltage		3			1.5	1			3.0	2,3	mV
		R_S 50k	4			2.0	1			3.0	2,3	mV
I_{OS}	Input Offset Curret		4			4	1			6	2,3	nA
I_B	Input Bias Current		3			50	1			80	2,3	nA
			4			65	1			80	2,3	nA
$\frac{V_{OS}}{T}$	Input Offset Voltage Drift	T_{MIN} T T_{MAX}	5,9							25		µV/°C
A_{VOL}	Large Signal Voltage Gain	R = 1k to 15V, −10V V_{OUT} 14.5V		200			4					V/mV
		R = 500 to 5V, 0.5V V_{OUT} 4.5V		50			4					V/mV
CMRR	Common Mode Rejection Ratio			90			1					dB
	Input Voltage Range	V_S = ±15V	8,9	−14.5		13		−14.5		13		V
		V_S = Single 5V	8,9	0.5		3.0		0.5		3.0		V
t_d	Response Time		6,9			250						ns
V_{OL}	Output Saturation Voltage	V_{IN} = 5mV, I_{SINK} = 8mA				0.4	1			0.5	2,3	V
		V1 = 0V, I_{SINK} = 50mA				1.5	1			1.5	2,3	V
	Output Leakage Current	V_{IN} = 5mV, V1 = −15V, V_{OUT} = 20V				10	1			500	2,3	nA
	Positive Supply Current					4.0	1					mA
	Negative Supply Current					2.5	1					mA
	Strobe Current	Minimum to Ensure Output Transisor is Turned Off	7,9	500								µA
	Input Capacitance				6							pF

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 10)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	MAX	20Krad(Si) MIN	MAX	50Krad(Si) MIN	MAX	100Krad(Si) MIN	MAX	200Krad(Si) MIN	MAX	UNITS
V_{OS}	Input Offset Voltage				1.5		1.5		1.5		1.5		2	mV
I_{OS}	Input Offset Current				4		4		4		20		50	nA
I_B	Input Bias Current				50		100		150		200		300	nA
A_{VOL}	Large-Signal Voltage Gain	R = 1k to 15V −10V V_{OUT} 14.5V		200		200		150		100		50		V/mV
CMRR	Common Mode Rejection Ratio			90		90		90		90		86		dB
	Input Voltage Range	V_S = ±15V	8,9	−14.5	13	−14.5	13	−14.5	13	−14.5	13	−14.5	13	V
		V_S = Single 5V		0.5	3.0	0.5	3.0	0.5	3.0	0.5	3.0	0.5	3.0	V
V_{OL}	Output Saturation Voltage	V_{IN} = 5mV, I_{SINK} = 8mA			0.4		0.4		0.4		0.4		0.4	V
		V_{IN} = 0V, I_{SINK} = 50mA			1.5		1.5		1.5		1.5		1.5	V
	Output Leakage Current	V_{IN} = 5mV, V1 = −15V V_{OUT} = 20V			10		10		100		100		100	nA

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 10)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si) MIN	10Krad(Si) MAX	20Krad(Si) MIN	20Krad(Si) MAX	50Krad(Si) MIN	50Krad(Si) MAX	100Krad(Si) MIN	100Krad(Si) MAX	200Krad(Si) MIN	200Krad(Si) MAX	UNITS
	Positive Supply Current				4.0		4.0		4.0		4.0		4.0	mA
	Negative Supply Current				2.5		2.5		2.5		2.5		2.5	mA
	Strobe Current	Minimum to Ensure Output Transistor is Truned Off	7,9	500		500		500		500		500		µA
	Input Capacitance				6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)		6 (Typ)	pF

Note 1: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection discussion in the LT®1011 data sheet.

Note 2: T_{JMAX} = 150°C.

Note 3: Output is sinking 1.5mA with V_{OUT} = 0V.

Note 4: These specifications apply for all supply voltages from a single 5V to ±15V, the entire input voltage range and for both high and low output states. The high state is I_{SINK} 100µA, V_{OUT} ($V^+ - 1V$) and the low state is I_{SINK} 0.8V. Therefore, this specication defines a worst-case error band that includes effects due to common mode signals, voltage gain and output load.

Note 5: Drift is calculated by dividing the offset difference measured at minimum and maximum temperatures by the temperature difference.

Note 6: Response time is measured with a 100mV step and 5V overdrive. The output load is a 500 resistor tied to 5V. Time measurement is taken when the output crosses 1.4V.

Note 7: Do not short the STROBE pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500µA will strobe the RH1011 if speed is not important. External leakage on the STROBE pin in excess of 0.2µA when the strobe is "off" can cause offset voltage shifts.

Note 8: See graph, Input Offset Voltage vs Common Mode Voltage on the LT1011 data sheet.

Note 9: Guaranteed by design, characterization or correlation to other tested parameters.

Note 10: V_S = ±15V, V_{CM} = 0V, R_S = 0 , T $_A$ = 25°C, V1 = –15V, output at Pin 7, unless otherwise noted.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4
Group A Test Requirements (Method 5005)	1,2,3,4
Group C and D End Point Electrical Parameters (Method 5005)	1

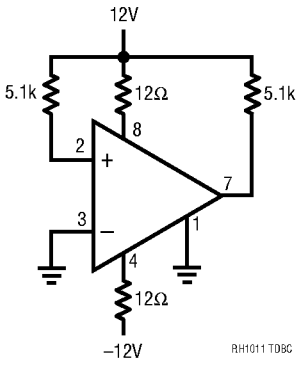
* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

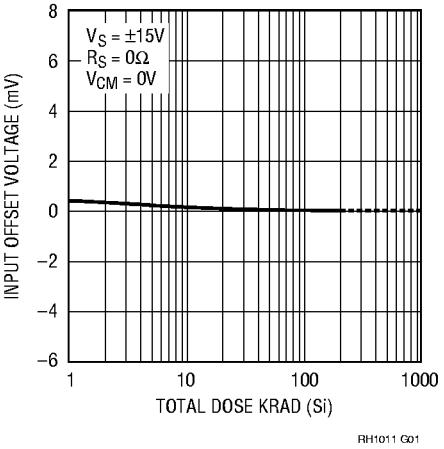
Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT

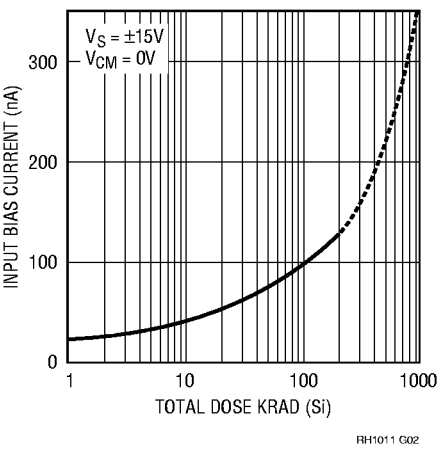


TYPICAL PERFORMANCE CHARACTERISTICS

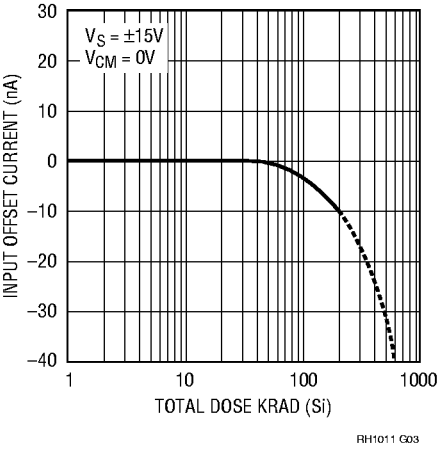
Input Offset Voltage



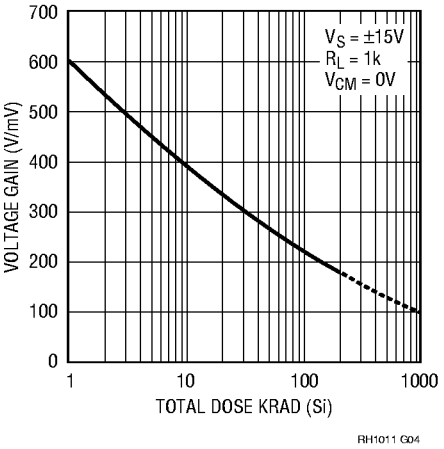
Input Bias Current



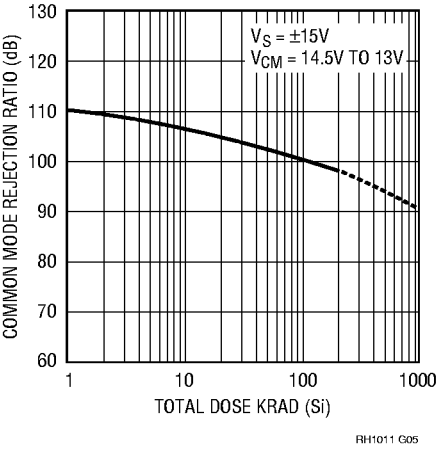
Input Offset Current



Voltage Gain



Common Mode Rejection Ratio



I.D. No. 66-10-0159 Rev. A 0896

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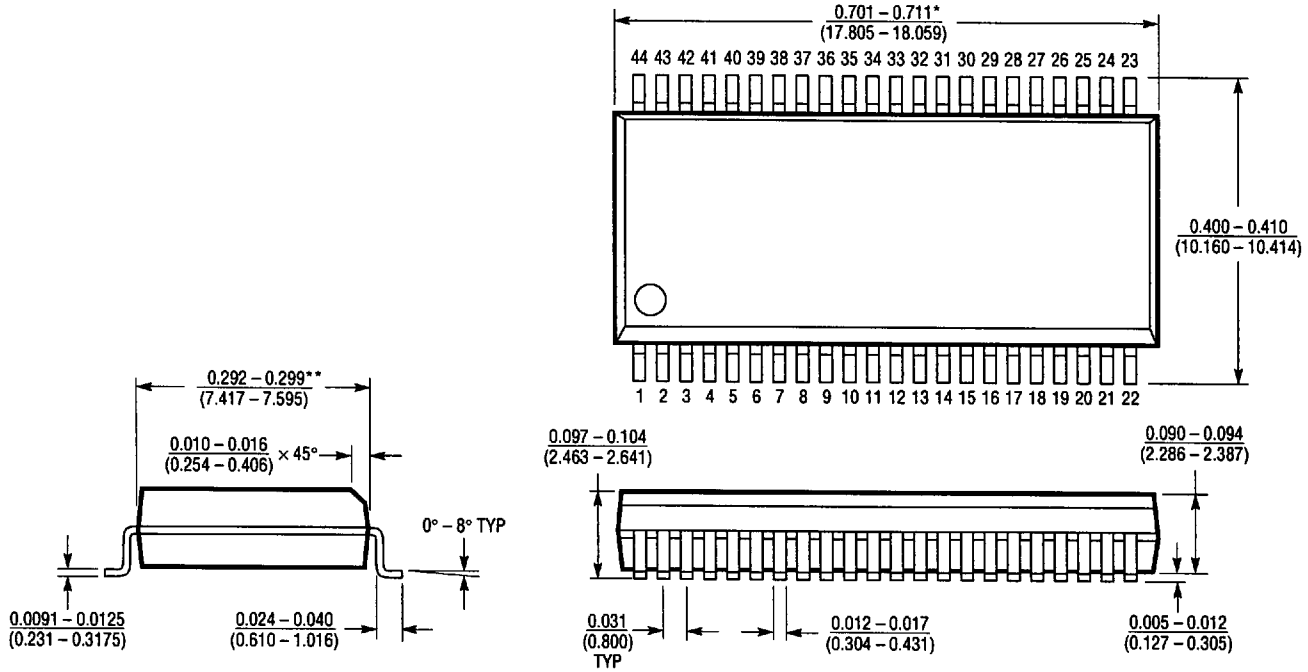
LT/HP 0896 REV A 500 • PRINTED IN USA

GW Package
44-Lead Plastic SSOP (Wide 0.300)
(LTC DWG # 05-08-1642)

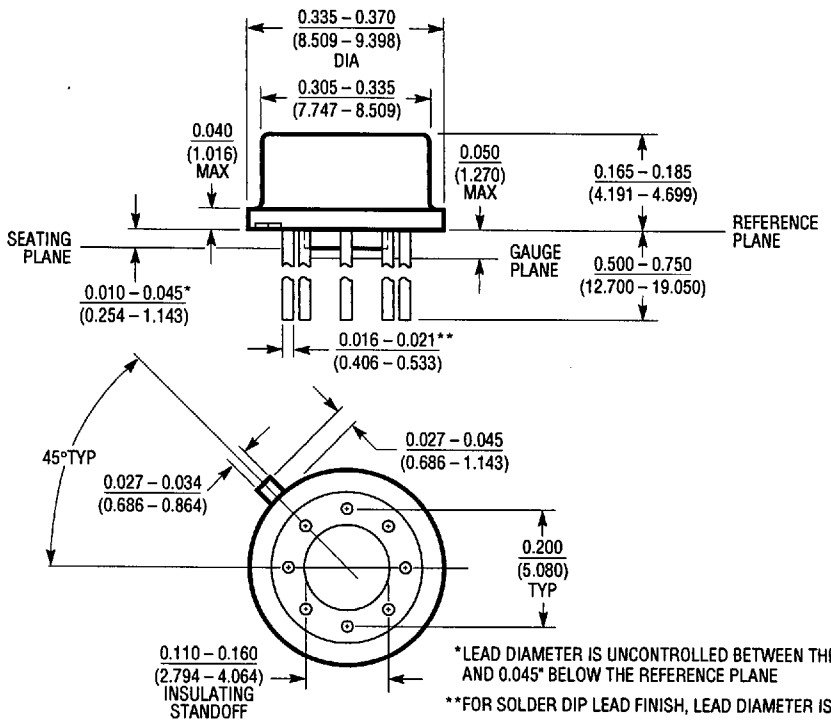


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G44 SSOP 0695

H Package
8-Lead TO-5 Metal Can (0.200 PCD)
(LTC DWG # 05-08-1320)

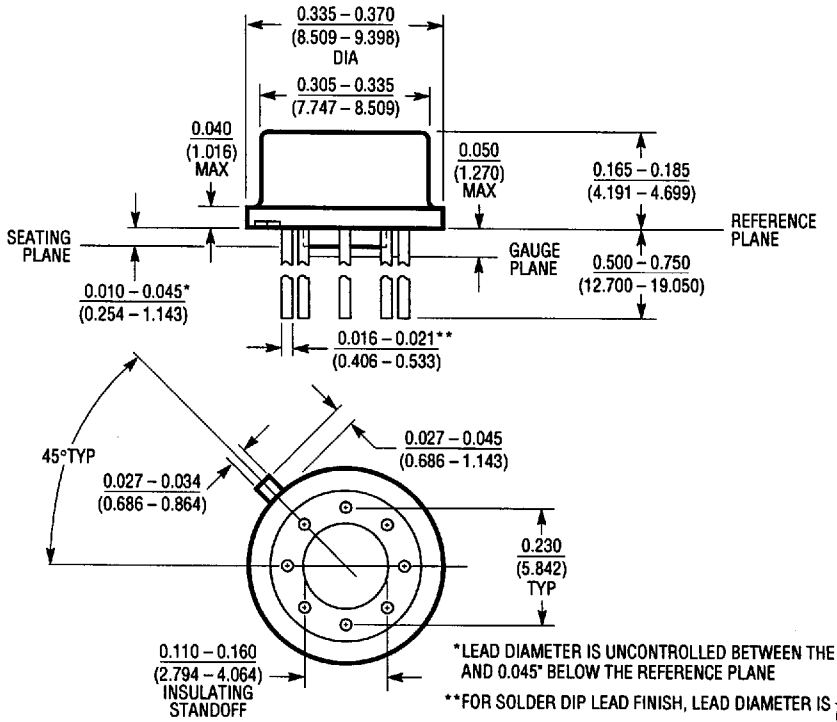


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H8(TO-5) 0.200 PCD 0595

H Package
8-Lead TO-5 Metal Can (0.230 PCD)
(LTC DWG # 05-08-1321)

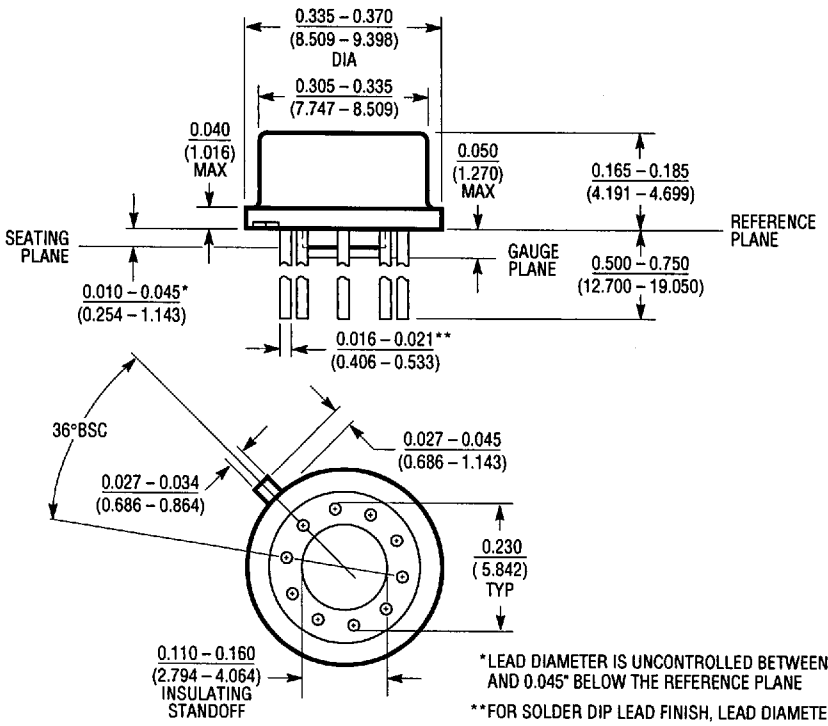


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

H8 (TO-5) 0.230 PCD 0595

H Package
10-Lead TO-5 Metal Can
(LTC DWG # 05-08-1322)

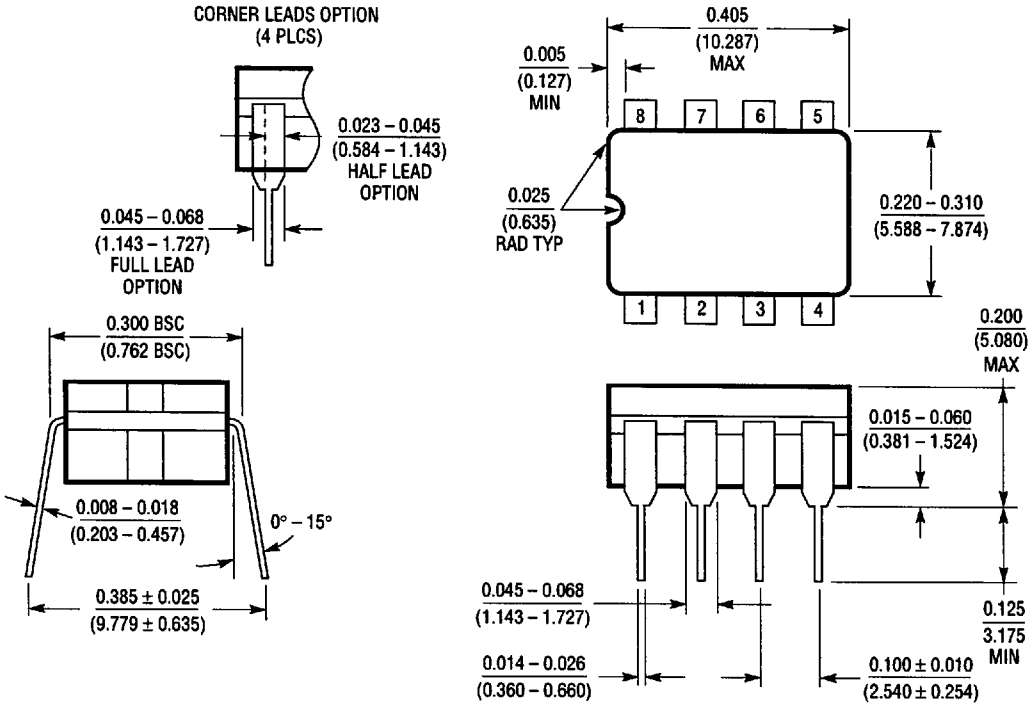


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

H10(TO-5) 0595

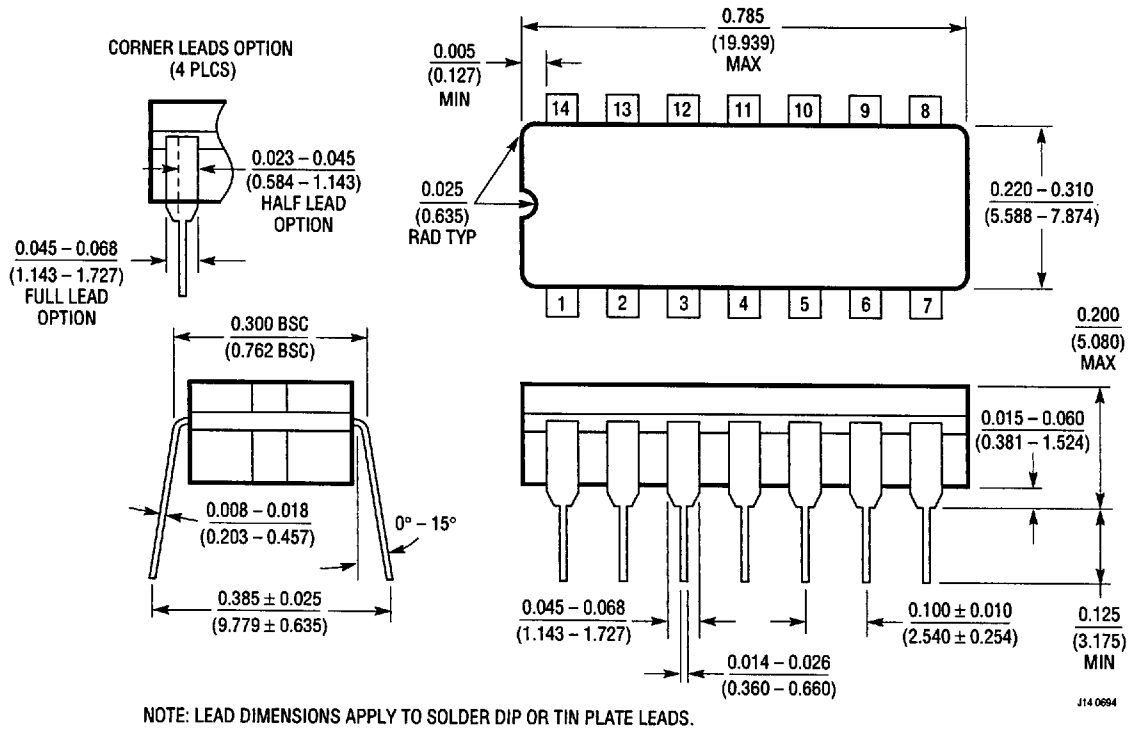
J8 Package
8-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J8 0694

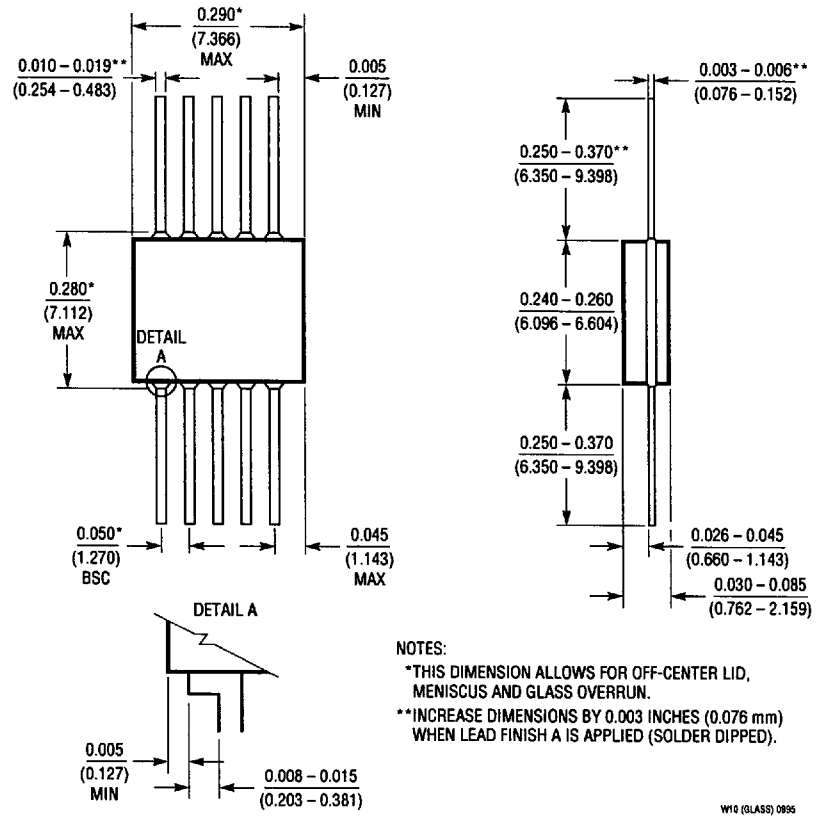
J Package
14-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

J14 0694

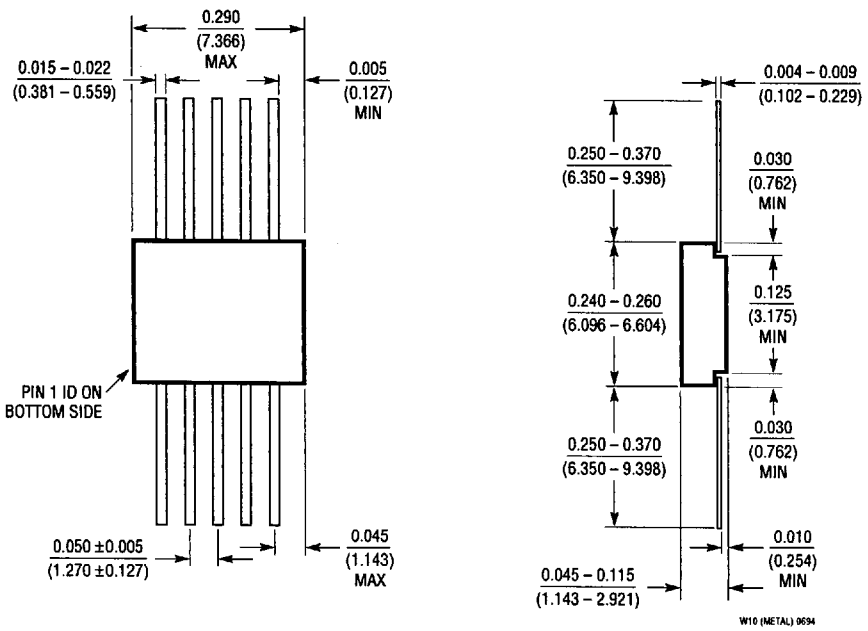
W Package
10-Lead Flatpak Glass Sealed (Hermetic)
(LTC DWG # 05-08-1130)



NOTES:
*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
**INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED).

W10 (GLASS) 0695

WB Package
10-Lead Flatpak Metal Sealed Bottom Brazed (Hermetic)
(LTC DWG # 05-08-1230)



W10 (METAL) 0694