PM8315

TEMUX™

TEMUX

High Density T1/E1 Framer with Integrated VT/TU Mapper and M13 Mux

Errata for the Production Released Device

Proprietary and Confidential

Released

Issue 4: June 2002

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4	June 2002	Notification of additional information and errors to TEMUX Data Sheet Issue R7, TEMUX Register Description R5 and TEMUX Programmer's Reference Guide R3. Added items 2.3 to 2.6, 3.7 to 3.18.
3	October, 2001	Notification of additional information and errors to TEMUX Data Sheet Issue R7 and TEMUX Register Description R5.
2	August, 2001	Notification of additional information and errors to TEMUX Data Sheet Issue R7 and TEMUX Register Description R5.
1	April 23, 2001	Document created.

Table of Contents

1 Introduction

In this document:

- Section 2 lists the known functional errata for the Production Released Version of the PM8315 TEMUX.
- Section 3 lists documentation errors found in Issue 7 of the PM8315 TEMUX Datasheet (PMC-1981125), Issue 5 of the PM8315 TEMUX Register Description (PMC-1990495) and Issue 4 of the PM8315 TEMUX Programmer's Reference Guide (PMC-1991268).

1.1 Device Identification

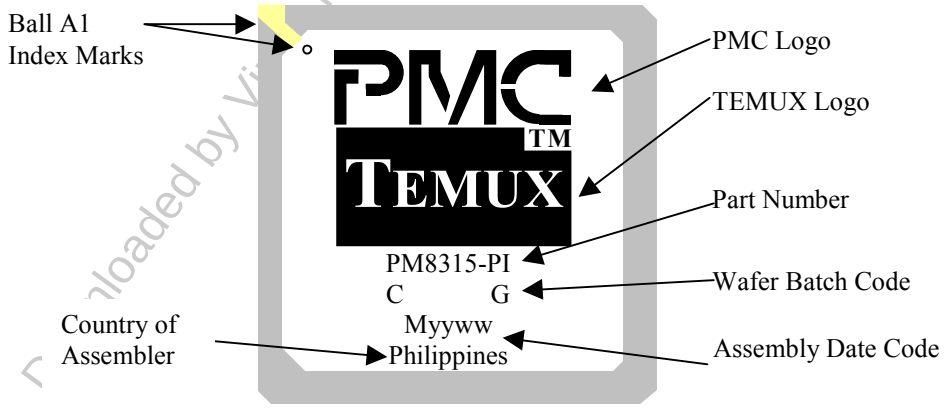
The information contained in Section 2 relates to the Production Released version of the PM8315 TEMUX device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

Register 0002H: Revision/Global PMON Update identifies the Production Release revision of the PM8315 TEMUX using the type identification bits 0101.

Note: This errata only applies to issues specific to the production released PM8315-PI TEMUX device. It does not apply to any of the prototype TEMUX devices.

The prototype TEMUX devices are denoted with a –P following the part number that is labeled on the device (ie. PM8315-PI-P signifies a prototype while PM8315-PI signifies a production part). The errata for the prototype TEMUX devices is contained in the PM8315 TEMUX Datasheet Errata (PMC-1990677, R9) available from your local sales representative.

Figure 1 PM8315 Branding Diagram



1.2 References

- Issue 7 of the PM8315 TEMUX Datasheet (PMC-1981125).
- Issue 4 of the PM8315 TEMUX Programmer's Reference Guide (PMC-1991268).
- Issue 5 of the PM8315 TEMUX Register Description (PMC-1990495)

2 Device Functional Deficiency List

This section lists the known functional deficiencies for the Production Released version of the PM8315 TEMUX as of the publication date of this document.

Please report any functional deficiencies not covered in this errata to PMC-Sierra.

2.1 Use of HDLC Controller in E1 Mode

When using the internal HDLC controllers in E1 mode there are some restrictions to be aware of:

- If data is inserted into a timeslot from the internal HDLC controller and the previous timeslot has an idle code byte inserted from the TPSC, the last two bits of the idle code can be corrupted. This means that if timeslot 4 has data inserted from the HDLC controller, and an idle code has been inserted in timeslot 3 from the TPSC, the least significant two bits of timeslot 3 can be corrupted. It is recommended that HDLC traffic be inserted from the backplane rather than the internal controller if idle codes are being transmitted in the preceding timeslot.
- If data is inserted into timeslot 1 from the internal HDLC controller, the least significant bit in timeslot 0 for NFAS frames only (i.e., Sa8) can be corrupted if configured to come from the backplane. The National Use Bits codeword, however, operates correctly on Sa8 if enabled. It is recommended that timeslot 1 not be used for HDLC traffic inserted from the internal controller.
- In normal operation, if a timeslot is configured for both HDLC transmission and idle code insertion, HDLC is supposed to be transmitted and the idle code ignored. It is possible in TEMUX for the last two bits of the HDLC data to be corrupted. To get around this, simply disable idle code insertion for that timeslot when HDLC data is being transmitted.
- Inserting HDLC data into the National bits Sa8, Sa7, Sa6, or Sa5 can cause the neighboring more significant bit to be corrupted. For example, if HDLC is inserted into Sa7, then Sa6 can be corrupted, but only if Sa6 is inserted from the backplane. The National bits are always inserted error-free when they are generated via the National Bits Codeword register of the E1-TRAN block.
- Inserting HDLC data into the Si bit in TS0 (i.e., the international bit) can cause the least significant two bits of an IDLE code in TS31 to be corrupted.

2.2 VT-AIS Tributary Corruption

An issue in the TEMUX demapper results in the VT-AIS causing corruption to the previous tributary of SPE#3 only.

To circumvent this issue, apply the software workaround outlined in Section 16 of the Programmer's Reference Guide (PMC-1991268).

2.3 DS3 PRGD block limits useable repeating patterns in unchannelized M23 mode

2.3.1 Description

As described in the TEMUX Data Sheet, Section 12.1: DS3 Framing Format, the TEMUX device provides support for both the C-bit parity and M23 DS3 framing formats. The DS3 frame format is shown in Figure 13 of the Data Sheet (copied below):

	84 bits		84 bits		84 bits		84 bits		84 bits		84 bits		84 bits	
M-subframe 1	X_1		F_1		C_1		F_2		C_2		F_3		C_3		F_4	
M-subframe 2	X_2		F_1		C_1		F_2		C_2		F_3		C_3		F_4	
M-subframe 3	P_1		F_1		C_1		F_2		C_2		F_3		C_3		F_4	
M-subframe 4	P_2		F_1		C_1		F_2		C_2		F_3		C_3		F_4	
M-subframe 5	M_1		F_1		C_1		F_2		C_2		F_3		C_3		F_4	
M-subframe 6	M_2		F_1		C_1		F_2		C_2		F_3		C_3		F_4	
M-subframe 7	M_3		F_1		C_1		F_2		C_2		F_3		C_3		F_4	

The C-bit Parity ID bit is the first C-bit (C_1) of the M-subframe 1. In the receive direction, the CBITV register bit in the DS3 FRMR Status register is used to report the state of this C-bit Parity ID. If the ID bit is 1, the DS3 frame received is assumed to be C-bit parity. If the C-bit Parity ID is 0 or toggling, the DS3 signal stream received is assumed to be M23.

Unchannelized repeating patterns are regenerated each time the PRGD Pattern Insertion Register #4 is written to (Register 103BH). In M23 mode, the DS3 PRGD always sets all C-bits to the same value, a value based on the last transmitted bit. For an all-1's pattern, all C-bits will be 1. Similarly for an all-0's pattern, all C-bits will be 0. For an alternating 10101010 pattern for instance, there is a 50/50 chance of all C-bits being 1.

An issue arises when attempting to generate an unchannelized all-1's M23 pattern. Recall that an M23 signal stream would require the C-bit Parity ID to be 0 or toggling. However, the DS3 PRGD will set all C-bits (and hence the C-Bit Parity ID) to 1 when generating an all-1's pattern. The receiver will therefore interpret the DS3 frame to be C-bit parity rather than the correct M23 format. As a result, a frame mismatch would be declared if an all-1's is generated in M23 mode.

Similarly, an alternating 10101010 M23 pattern has a 50/50 chance of being misinterpreted as a C-bit parity DS3 stream while in unchannelized DS3. For patterns containing one or more 0's, the occurrence of this problem is related to the 1's density of the pattern. An example is a 31-ones, 1-zero pattern in M23 mode. On average, this pattern will work without frame mismatch one every 32 tries, as there is a 1/32 chance of C-bit parity ID being 0.

In C-bit parity mode, there are no problems passing all-1's because the ID bit is always overwritten with a 1.

2.3.2 Workaround

There is no way to generate an all-1s pattern while in unchannelized M23 mode without seeing frame mismatch errors. Because the DS3 PRGD block limitation applies to unchannelized DS3 only, utilizing C-bit parity mode (instead of M23) allows the generation of an all-1's pattern.

In the event that unchannelized M23 mode must be used, several other patterns can be used without declaring DS3 frame mismatch. For patterns containing one or more 0's, the occurrence of this mistaken M23 signal for C-bit parity is related to the 1's density of the pattern.

The following algorithm can be used to to generate patterns other than all-1's in M23 mode:

- Write to PRGD Pattern Insertion Register #4 (Register 103BH) to generate unchannelized repeating patterns.
- At the receiver, check the framer for a DS3 frame mismatch. If using a loopback or another TEMUX, the DS3 framing circuitry of the TEMUX reports the frame mismatch using DS3 FRMR status bit CBITV.
- If frame mismatch has occurred, repeat. Else, transmitted pattern is correct.

An all-0's pattern can always be transmitted correctly while the TEMUX is in unchannelized M23 mode.

2.3.3 Performance with Workaround

There is no workaround to implement the generation of an all-1s pattern while in unchannelized M23 mode. Using C-bit parity DS3 framing format is recommended to generate all-1's.

The TEMUX device will operate normally in DS3 testing scenarios with the suggested workaround in place for M23 mode.

2.3.4 Performance without Workaround

DS3 Frame Mismatch will be declared when attempting to generate all-1's pattern in unchannelized M23 mode.

2.4 Demapping DS3 when CLK52M = 51.84 MHz is not recommended

2.4.1 Description

In the TEMUX Data Sheet, there is a choice between two clock frequencies for **CLK52M** input (Pin P3):

> " The 52Mhz clock reference is used to generate a gapped DS3 clock when demapping a DS3 from the SONET stream and also to generate a gapped DS3 clock when receiving a DS3 from the SBI bus interface. This clock has two nominal values.

The first is a nominal 51.84MHz 50% duty cycle clock. The second is a nominal 44.928MHz 50% duty cycle clock.

When this clock is not used this input must be connected to ground."

Repetitive data corruption with demapped DS3 may occur in systems using the 51.84 MHz clock. It has been confirmed that this is not an issue if the alternate clock frequency, 44.928 MHz, is used.

When 51.84MHz is synchronized to LREFCLK, errors still occur as long as the incoming DS3 ppm offset is greater than the relative offset of the 51.84MHz. The data corruption is theoretically possible with or without incoming STS level pointer movements. At this time however, no errors have ever been observed in the absence of STS level pointer movements. Also, standard test equipment used as the mapped DS3 source has yet to produce the error condition. Only a TEMUX device mapping the DS3 causes the errors.

2.4.2 Workaround

When configured to demap DS3 payloads from SONET STS1/SDH AU3, the CLK52M input being 44.928MHz would avoid this possible data corruption to the DS3 stream. Thus, the FASTCLKFREQ bit of Register 1209H must be cleared to logic 0. Using the 44.928MHz clock has always been a fully supported mode of the TEMUX.

2.4.3 Performance with Workaround

If the 44.928MHz clock frequency is used for CLK52M while demapping DS3s from SONET STS1/SDH AU3, the risk of data corruption in this mode no longer exists. It is highly recommended to use this clock frequency when demapping DS3s in new TEMUX designs going forward.

2.4.4 Performance without Workaround

When demapping DS3s from SONET/SDH payloads, if the CLK52M input is set to 51.84MHz, there is a risk of data corruption. It is highly recommended to use 44.928MHz crystals for new designs.

2.5 Incorrect Link Rate Octet generated when demapping DS3 from SONET

2.5.1 Description

When the TEMUX device is in DS3 framer-only mode, the linkrate clock rate field over the SBI bus tolerates approximately 4 UI of jitter in a 500uS (2kHz) period. When demapping a DS3 from SONET, gapping the CLK52M reference clock generates the serial DS3 clock. The gapping procedure utilizes FIFO depth to control the gapping algorithm.

The gapping algorithm used by the DS3 demapper exceeds the jitter tolerance of the SBI linkrate. Data taken by the link layer SBI devices via their EXSBI FIFO is derived from these faulty linkrate values. These values no longer match the actual data rate. With the clock rate octet enabled in layer 2 SBI devices, the DS3 clock could only be varied by a few ppm before the EXSBI FIFO underflows or overflows. As a result, data corruption can occur.

Therefore, when demapping DS3s from SONET in the TEMUX, the layer 2 SBI devices cannot rely upon link rate octet to regenerate clocking. Rather, the DS3 serial clocks need to be routed around the SBI bus.

The only affected applications are those in which link rate may be relied upon:

1. AAL1 circuit emulation, involving TEMUX and AAL1gator devices. In fact, for this application, it is always recommended to route the DS3 timing around the SBI bus even in DS3 LIU applications. For DS3 mapping applications, an additional external DS3 JAT is required to smooth the DS3 clock before it is fed into the AAL1gator32 device.

2. Back-to-back TEMUX devices over SBI.

Data applications, such as those involving TEMUX and FREEDM packet processing or IMA ATM are completely unaffected by this problem. These particular link layer devices do not utilize link rate values.

2.5.2 Workaround

In data applications involving FREEDM packet processing and IMA ATM, the FIFO method is used to pass data across the SBI bus when demapping DS3 from SONET. Hence, an incorrect link rate octet does not affect these applications.

However, for AAL1 circuit emulation (CES) applications that demap DS3 from SONET, the serial DS3 clocks (generated by gapping CLK52M) need to be routed around the SBI bus. This is normally done for serial DS3 but in addition, a DS3 JAT is required for demapping applications.

Refer to PMC-1990887 "AAL1gator-32 CES Reference Design", Issue 5 for details.

2.5.3 Performance with Workaround

If the serial DS3 clocks are routed around the SBI bus in DS3 demapping CES applications, there will be no excess jitter introduced.

2.5.4 Performance without Workaround

Data corruption may occur when demapping DS3s from SONET in AAL1 circuit emulation.

2.6 Automatic SBI tributary reset not available when mixing sync and async tributaries per SPE

2.6.1 Description

In the INSBI Control Register 1720H, the DC_RSTEN bit controls the INSBI automatic depth check logic, whereby the link will automatically reset upon detection of a depth check error, i.e. INSBI underrun or overflow. When the DC_RSTEN bit is set to 1, the automatic reset is enabled. If DC_RSTEN is set to 0, the link must be manually reset upon depth interrupt.

However, there is a limitation to this automatic depth check logic. In Register 1726H: INSBI Tributary Control Indirect Access Data, the SYNCH_TRIB bit controls whether tributaries operate in synchronous mode on the SBI DROP bus. However, when there is a mix of synchronous and non-synchronous tributaries, i.e. SYNCH_TRIB = 1 for some and SYNCH_TRIB=0 for others, the INSBI automatic depth check logic does not operate properly. Hence, underflows or overflows in the SBI FIFOs are not serviced with a link reset. Data corruption may occur as result.

As stated in Errata item 3.17, DC_RSTEN should not be set to 1 when INSBI SYNCH_TRIB bit (Register 1726H: INSBI Tributary Control Indirect Access Data) settings are mixed between 0 and 1, indicating only some tributaries are synchronous to the SBI bus".

2.6.2 Workaround

When underruns or overruns are detected via the interrupt indications of Registers 1721H or 1722H respectively, the tributary must be manually reset to clear the error condition.

To reset a given tributary, an indirect write access must be performed to Register 1726: Tributary Control RAM Indirect Data Register for the errored tributary, with the last value written to the register. This will write a logic 1 to the ENBL bit that will trigger a reset of that tributary.

2.6.3 Performance with Workaround

Device operates normally after a manual reset of the errored tributary

2.6.4 Performance without Workaround

Without manually resetting the tributary, it may never exit the errored state and data corruption will result.

3 Documentation Deficiency List

This section of the document is a notification of additional information to Issue 7 of the PM8315 TEMUX Datasheet (PMC-1981125) and Issue 5 of the PM8315 TEMUX Register Description (PMC-1990495).

This section also lists the known documentation deficiencies for Issue 7 of the PM8315 TEMUX Datasheet (PMC-1981125) and Issue 5 of the PM8315 TEMUX Register Description (PMC-1990495) as of the publication date of this document.

Please report any documentation deficiencies not covered in this errata to PMC-Sierra.

3.1 Connecting to the Telecom ADD bus via an External Mux

The pin description for LAC1J1V1 may need clarification. When connecting the TEMUX to the TelecomBus via an external mux (instead of simply tri-stating the bus), the LAC1J1V1 signal should not be muxed. This means that when there are three TEMUXs connected to a SPECTRA's TelecomBus through the mux, the LAC1J1V1 signal from only one of the three TEMUXs should be connected to the SPECTRA. The other two LAC1J1V1 signals should remain unconnected. All TEMUXs must have the LOCK0 bit in registers 1202H and 15E5H set the same.

3.2 Telecom Bus Parity Generation

3.2.1 Telecom ADD Bus Parity Generation

The TEMUX device cannot generate parity on the Telecom ADD bus when LAC1J1V1 is set to participate in the egress parity generation. Parity generation only helps check integrity of the bus connections and have no effect on the data path or with control of the device. If egress parity needs to be generated, LAC1J1V1 should not be used.

3.2.2 Telecom DROP Bus Parity Detection

The TEMUX device *can* correctly detect parity on the Telecom DROP bus when LDC1J1V1 Is set to participate in the ingress parity detection. The Register Description documentation is erroneously missing this optionally selectable feature.

Accordingly, Register 1201H of the Register Description document should be amended as shown in the following table:

Register 1201H: SONET/SDH Master Ingress Configuration

Bit	Type	Function	Default
Bit 7	R/W	LDPE	0
Bit 6	R/W	ITMFEN	0
Bit 5	R/W	IVTPPBYP	0
Bit 4	R/W	ITSEN	0
Bit 3	R/W	INCLDPL	0
Bit 2	**R/W**	**INCLDC1J1V1**	**0**
Bit 1	R/W	LDOP	0
Bit 0	R/W	ICONCAT	0

INCLDC1J1V1:

The INCLDC1J1V1 bit controls whether the LDC1J1V1 input signal participates in the incoming parity calculations. When INCLDC1J1V1 is set high, the parity signal set includes the LDC1J1V1 input. When INCLDC1J1V1 is set low, parity is calculated without regard to the state of LDC1J1V1. Selection of odd or even parity is controlled by the LDOP bit.

3.3 Byte Deletion/Insertion in VT/TU Mapping Mode

While rare, it is possible for jitter on XCLK or the selected T1/ E1 transmit clock to cause an overflow or underflow in the transmit mapper (TTMP) FIFO. The T1/E1 transmit timing can be sourced from the two clock master sources, the CTCLK input or the recovered T1/E1 clock, or from the four clock slave sources, the CECLK input, the H-MVIP clock input, an ECLK[x] input or the SBI tributary rate received on the SBI add bus. By design, underflow or overflow will result in the loss of a byte of data. The initialization procedure shown in Section 16 of the Programmer's Reference Guide will push the FIFO closer to the center such that it can withstand more jitter from these clocks to reduce any impact on the datapath. If the FIFO is close to an underflow or overflow condition and jitter does push it over or under, the FIFO will insert or delete a byte of data, pushing itself away from these states and giving itself at least another 8 UI of margin against future jitter events on XCLK or the selected T1/E1 transmit clock.

You should use the initialization sequence shown in Section 16 of the Programmer's Reference Guide (PMC-1991268).

3.4 Duplication of Ground Pin Descriptions

The description of ground pins N3, Y12, L20 and B12 has been duplicated in two rows of the pin description section, pins VSSQ[1:4] and VSS3.3[19:22]. These pins should only be described in the VSS3.3 row. The VSSQ row should be eliminated. In any event these pins should be connected to GND as described.

3.5 AIS Insertion in DS3 Diagnostic Loopback

In the datasheet, Figure 2: DS3 Diagnostic Loopback Diagram states that AIS can optionally be inserted into the transmit datapath when a DS3 is in diagnostic loopback. This is incorrect. AIS cannot be inserted in the transmit path when in DS3 diagnostic loopback mode.

3.6 Path Signal Label Mismatch State

In the datasheet, Table 1: Path Signal Label Mismatch State is incorrect. It incorrectly references PDI code.

The table should read as follows:

Table 2 - Path Signal Label Mismatch State

Expected PSL	Accepted PSL	PSLM State
000	000	MATCH
000	001	MISMATCH
000	XXX ≠ 000	MISMATCH
001	000	MISMATCH
001	001	MATCH
001	XXX ≠ 001	MATCH
XXX ≠ 000, 001	000	MISMATCH
XXX ≠ 000, 001	001	MATCH
XXX ≠ 000, 001	XXX	MATCH
XXX ≠ 000, 001	YYY	MISMATCH

3.7 Transmultiplexing Mode Clarification

Transmultiplexing mode ("transmux") is not adequately described in the current TEMUX datasheet. This mode enables the exchange of 1.544Mbps tributaries between SONET/SDH TelecomBus and DS3 line interface.

The following excerpt should be added to Section 9: Functional Description:

Transmultiplexing ("transmux") is the operating mode that enables 1.544 Mb/s clear-channel tributaries to be exchanged between the SONET/SDH Telecom Bus and the DS3 line interface. It is enabled by setting the TEMUX Configuration register's OPMODE[1:0] bits to 10 and its LINEOPT [1:0] bits to 00. The system interface is unused in this mode.

The TEMUX will receive a channelized DS3 stream from the serial DS3 interface. It will frame up to the DS3 and de-multiplex the individual 1.544 Mb/s tributaries. The tributaries are jitter attenuated, bit asynchronously mapped into VT1.5/TU11s and presented on the Telecom Add bus.

In the reverse direction, VT1.5/TU11s are bit asynchronously de-mapped from the Telecom Drop bus. The 1.544 Mb/s tributaries are jitter attenuated and multiplexed into a DS3, which is presented on the serial DS3 interface.

Performance monitoring of T1 framing status and errors can be performed on the tributaries. On a per-tributary basis, the TXPMON context bit programmed through Register 000H+80H*N: T1/E1 Master Configuration register selects either the SONET/SDH mapper transmit or DS3 transmit T1 tributary for performance monitoring.

3.8 E1 Multiframe pulse configurations

The IMFPCFG[1:0] bits in Register 005H+80H*N (T1/E1 Ingress Serial Interface Mode Select) select whether IFP[x] (ingress frame pulse) indicates E1 CRC, signaling or both CRC and signaling multiframe boundaries. These bits must be configured in E1 or SBI modes. These IFP[x] modes are listed in Table 3 in the TEMUX Register Description as follows:

Table 3: Ingress Frame Alignment Configuration

IMFPCFG[1]	IMFPCFG[0]	Operation
0	0	Both E1 CRC and Signaling multiframe
0	1	E1 CRC multiframe
1	0	E1 Signaling multiframe
1	1	Both E1 CRC and Signaling multiframe

However, these bits should be set to signaling MF pulses in E1 mode of the TEMUX as follows:

1. Basic framing without CAS: must use signaling multiframe pulse, IMFPCFG[1:0]=10
2. CRC-4 multiframe without CAS:
    a. Signaling multiframe pulse IMFPCFG[1:0]=10, or
    b. CRC multiframe pulse IMFPCFG[1:0]=01

3. CAS modes: Basic Framing with CAS or CRC-4 multiframe with CAS:

    a. Signaling multiframe pulse IMFPCFG[1:0]=10

3.9 CENT bit description of TJAT and RJAT Configuration registers are incorrect

The following text should be ignored from the CENT bit description of the T1/E1 TJAT and RJAT Configuration Registers, Register 0017H + 80H*N and Register 0013H + 80H*N respectively:

> "It is recommended to set this bit to 1".

For the recommended setting of the TJAT and RJAT Configuration Register bits, refer to Section 16 of the TEMUX Programmer's Guide for VT/TU mapping modes and to Errata item 3.10 below for the DS3 M13 operational modes.

3.10 M13 TJAT and RJAT settings incorrect in Programmer's Guide

The TJAT and RJAT Configuration Register recommendations are incorrect in the TEMUX Programmer's Guide for channelized DS3 applications.

Sections 6.2.1 (T1) and 7.1.1 (E1) state the TJAT and RJAT manual centering procedures setting Register 0017H + 80H*N TJAT Configuration and Register 0013H + 80H*N RJAT Configuration to values of **0x20**.

Neither centering procedure should be followed for channelized DS3 T1 or E1 applications. Rather, these two registers should be programmed with values of **0x31** upon initialization for all modes. The only exception is where PM73122 AAL1gator-32 is connected to the TEMUX's system side SBI bus and operating in SRTS mode. In this particular application, the RJAT Configuration Register 0013H + 80H*N must be set to **0x23**.

The TEMUX Programmers Guide's TU mapping mode recommendations for TJAT and RJAT Configuration registers in Section 16 are correct and should be followed. This includes the manual centering routine for the TJAT and RJAT in Section 16.1.1.

3.11 IILPU max spec limit has been revised

In Table 44, the D.C. Characteristics table, the input low current parameter, IILPU maximum has been changed from +100µA to +150µA.

3.12 Revision ID Bits Section incorrect

The TEMUX Revision ID is located in ID[3:0] bits of Register 0x02, not TYPE[3:0] as incorrectly stated in a previous errata document (PMC-1990677, TEMUX Datasheet Errata, Issue 9, Section 7).

3.13 Egress mode settings incorrect for Clock Slave: Clear Channel

In Register 006H+80H*N: T1/E1 Egress Serial Interface Mode Select, the egress clock mode, EMODE, bit determines which serial interface mode is being used for this tributary.

In Table 44 of TEMUX Register Description Issue 5, the Clock Slave: Clear Channel operation should be configured by EMODE[2:0] = 010, not 01X.

The correct table should read as follows:

EMODE[2]	EMODE[1]	EMODE[0]	Operation
1	0	X	Clock Master: NxChannel
1	1	X	Clock Master: Clear Channel
0	0	1	Clock Slave: EFP Enabled
0	0	0	Clock Slave: External Signaling
0	1	**0**	Clock Slave: Clear Channel

3.14 CLK52M Clarification

In Section 9.32.3 DS3 Desynchronizer of the TEMUX Data Sheet, the following statement is misleading:

> "The Desynchronizer monitors the Elastic Store level to control the de-stuffing algorithm to avoid overflow and underflow conditions. **The Desynchronizer assumes either a 51.84 MHz clock (provided internally)** or a 44.928 MHz clock (provided via input CLK52M)."

The 51.84MHz clock option is not provided internally within the TEMUX device. Hence, DS3 signals cannot be transported without connecting CLK52M.Refer also to Errata Section 2.4 for CLK52M discussion when demapping DS3s.

3.15 Recommended RTDM Leak Rate incorrect

It was incorrectly recommended in the TEMUX Programmer's Guide, Section 16.4 b) "Register 12E0H: RTDM Pointer Justification Rate Control" that E1RATE[1:0] be set to 10.

The recommended settings should read E1RATE[1:0]=00, the default and slowest leak rate settings to ensure no degradation of jitter performance.

3.16 Behavior of FIFO status handling needs clarification

In the extract and insert SBI (EXSBI, INSBI) FIFOs, the TEMUX has a priority mechanism for reporting underruns and overruns on certain tributaries. In general, lower-numbered tributaries can seemingly block the reporting of FIFO events on higher-numbered tributaries.

Consider an example where all tributaries underrun continuously. After reading status register errors for the first few tributaries, it may be the case that new underrun events are registered. In this case, errors will appear again for lower number tributaries before errors for higher number tributaries can be read.

In general, errors for a particular tributary cannot be read from the status register if an error on any lower numbered tributary has not been read.

This behaviour will only become evident in the rare event that several tributaries are simultaneously exhibiting FIFO errors. Note that this priority mechanism does not inhibit normal behavior of the TEMUX device.

3.17 INSBI automatic depth check logic behavior clarification

The following clarification needs to be made regarding the behavior of the INSBI automatic depth check logic:

Append the following statement to the DC_RSTEN bit description found in Register 1720H: INSBI Control and SYNCH_TRIB bit description in Register 1726H: INSBI Tributary Control Indirect Access Data:

> "The INSBI automatic depth check logic does not support a mix of synchronous and non-synchronous tributaries, i.e. DC_RSTEN should not be set to 1 when INSBI SYNCH_TRIB bit (Register 1726H: INSBI Tributary Control Indirect Access Data) settings are mixed between 0 and 1, indicating only some tributaries are synchronous to the SBI bus".

3.18 RJAT SYNC bit description in EXSBI CLK_MODE field clarified

In Register 1716H: EXSBI Tributary Control Indirect Access Data, the CLK_MODE[1:0] bit bndescription includes the following statement:

> "When using the **phase field** of the Link Rate octet, the SYNC bit in the RJAT configuration register needs to be set."

For clarification, the TEMUX RJAT is not usually connected to the TEMUX EXSBI. Hence, this comment about the "phase field" is more relevant to the device that uses this information, PM73122 AAL1gator-32's EXSBI, rather than TEMUX.

Notes