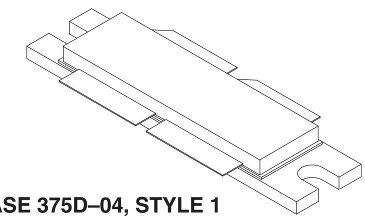
The RF Sub–Micron MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21180
MRF21180S

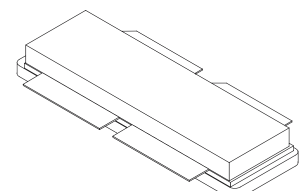
2170 MHz, 170 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs

Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 2 x 850 mA, f1 = 2135 MHz, f2 = 2145 MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ f1 – 5 MHz and f2 + 5 MHz. Distortion Products Measured over a 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz, Each Carrier Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
  Output Power — 38 Watts (Avg.)
  Power Gain — 12.1 dB
  Efficiency — 22%
  IM3 — 37.5 dBc
  ACPR — –41 dBc
- Internally Input and Output Matched, for Ease of Use
- High Gain, High Efficiency, and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2110 MHz, 170 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters



CASE 375D–04, STYLE 1
NI–1230
MRF21180



CASE 375E–03, STYLE 1
NI–1230S
MRF21180S

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	380 2.17	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.46	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 850 mAdc)	$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.18	0.22	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	6	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) 2–Carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers. Each carrier has Peak/Avg. ratio = 8.3 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	11	12.1	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	19	22	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured over 3.84 MHz BW @ f1 –10 MHz and f2 +10 MHz)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured over 3.84 MHz BW @ f1 – 5 MHz and f2 +5 MHz.)	ACPR	—	–41	–39	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 38 W Avg., I_{DQ} = 2 x 850 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 170 W CW, I_{DQ} = 2 x 850 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Each side of device measured separately. Part is internally matched both on input and output.
(2) Measurements made with device in push–pull configuration.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	12	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	33	—	%
Two–Tone Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–30	—	dBc
Two–Tone Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 170 W, I_{DQ} = 2 x 850 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, I_{DQ} = 2 x 850 mA, f = 2170 MHz)	P1dB	—	180	—	W

(2) Measurements made with device in push–pull configuration.

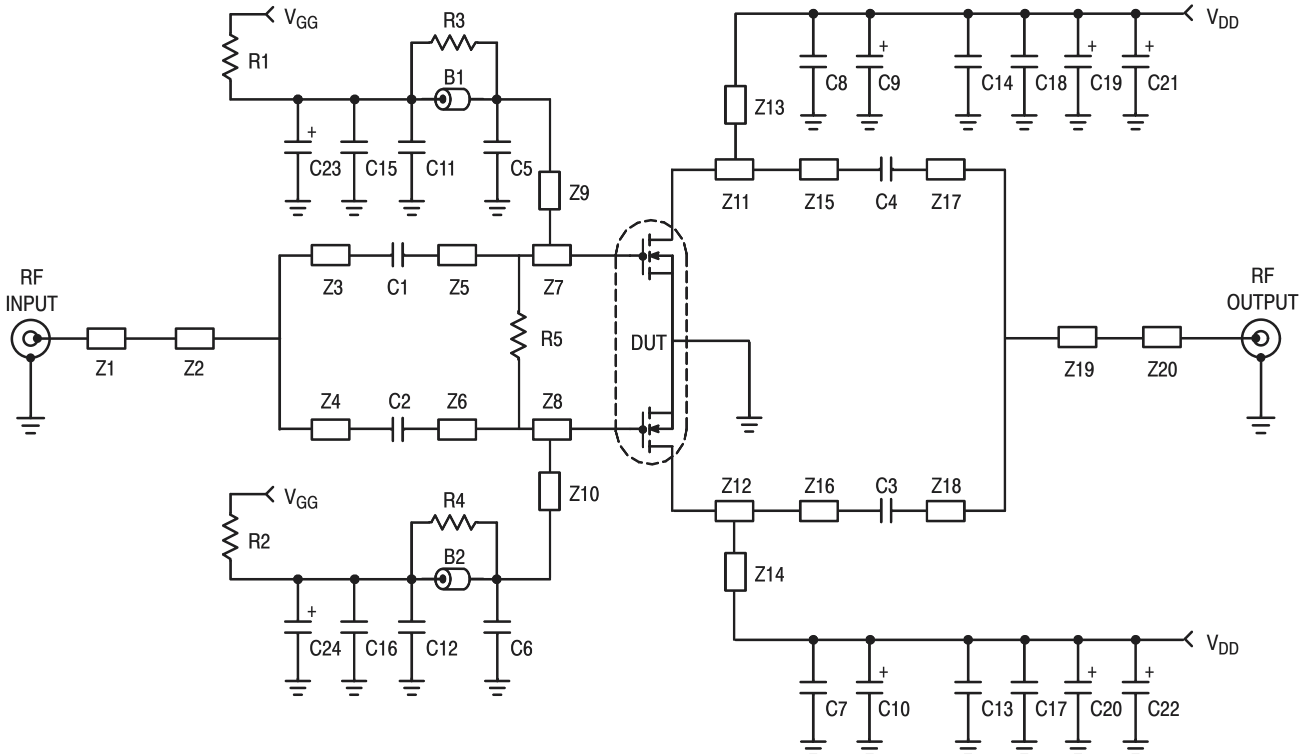


Figure 1. MRF21180 Test Circuit Schematic

Table 1. MRF21180 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
B1, B2	Short Ferrite Beads	2743019447	Fair Rite
C1, C2, C3, C4	30 pF Chip Capacitors	100B300JCA500X	ATC
C5, C6, C7, C8	5.6 pF Chip Capacitors	100B5R6JCA500X	ATC
C9, C10	10 μF Tantalum Capacitors	T495X106K035AS4394	Kemet
C11, C12, C13, C14	1000 pF Chip Capacitors	100B102JCA500X	ATC
C15, C16, C17, C18	0.1 μF Chip Capacitors	CDR33BX104AKWS	Kemet
C19, C20	1.0 μF Tantalum Capacitors	T491C105M050	Kemet
C21, C22, C23, C24	22 μF Tantalum Capacitors	T491X226K035AS4394	Kemet
N1, N2	Type N Flange Mounts	3052-1648-10	Omni Spectra
R1, R2, R3, R4	10 Ω, 1/8 W Chip Resistors		
R5	1.0 kΩ, 1/8 W Chip Resistor		
Z1, Z20	Microstrip	0.790″ x 0.065″	
Z2, Z19	Microstrip	0.830″ x 0.112″	
Z3, Z18	Microstrip	0.145″ x 0.065″	
Z4, Z17	Microstrip	1.700″ x 0.065″	
Z5, Z6	Microstrip	0.340″ x 0.065″	
Z7, Z8	Microstrip	0.455″ x 0.600″	
Z9, Z10	Microstrip	0.980″ x 0.035″	
Z11, Z12	Microstrip	0.510″ x 0.645″	
Z13, Z14	Microstrip	0.770″ x 0.058″	
Z15, Z16	Microstrip	0.280″ x 0.065″	
WB1, WB2, WB3, WB4	Wear Blocks		
Board	0.030″ Glass Teflon®	RF-35, ε_r = 3.50	Taconic
PCB	Etched Circuit Boards	MRF21180 Rev. 4	CMR

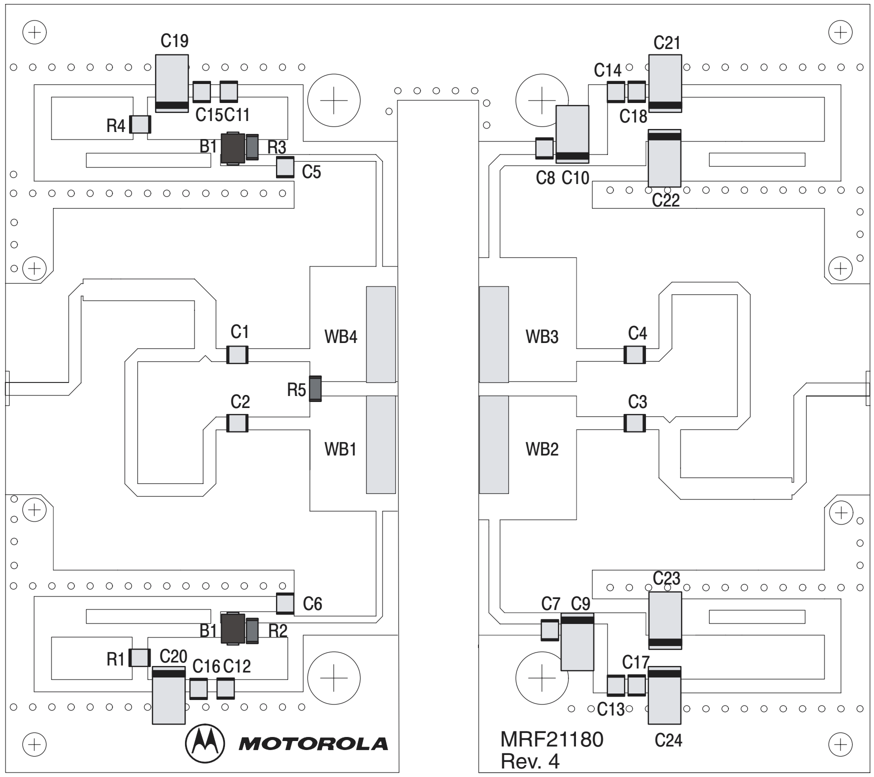


Figure 2. MRF21180 Test Circuit Component Layout

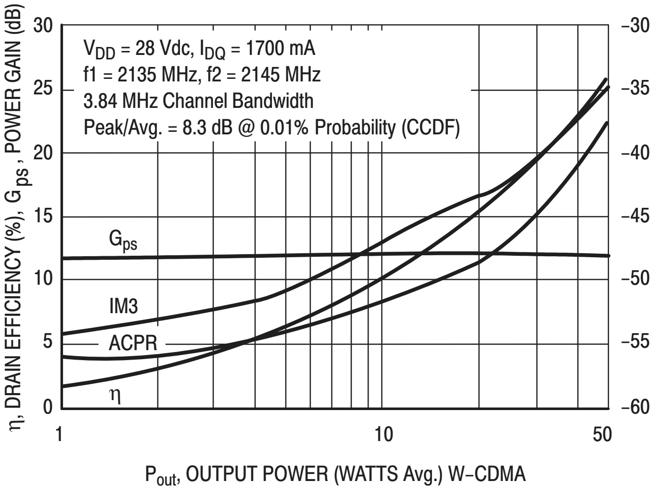


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

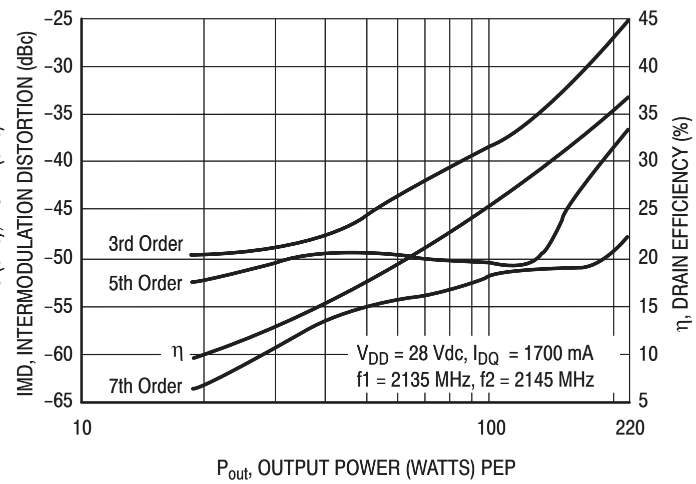


Figure 4. Intermodulation Distortion Products versus Output Power

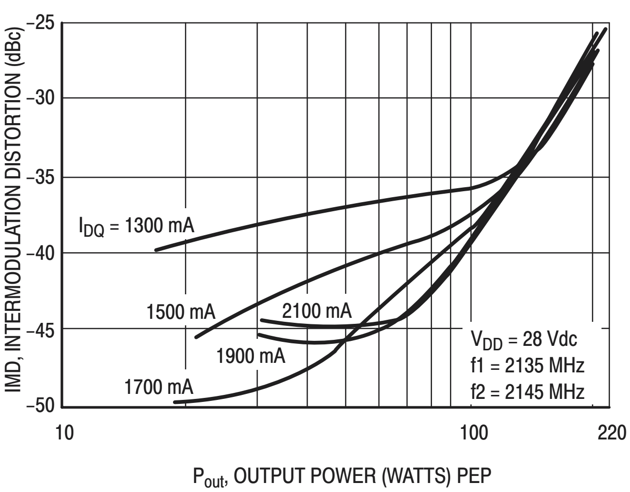


Figure 5. Intermodulation Distortion versus Output Power

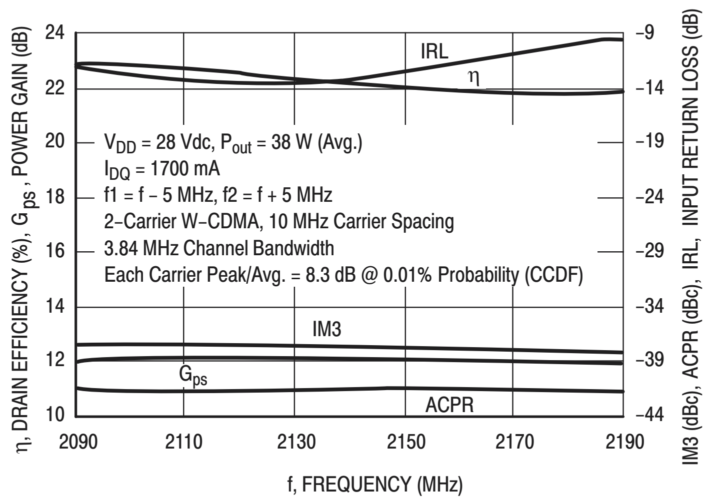


Figure 6. 2–Carrier W–CDMA Broadband Performance

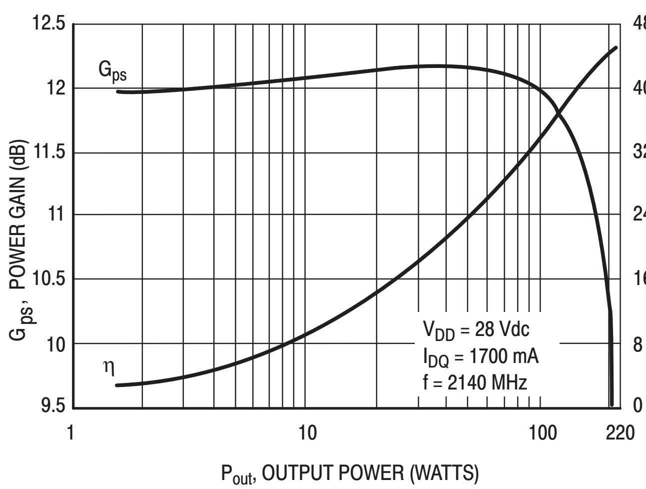


Figure 7. CW Performance

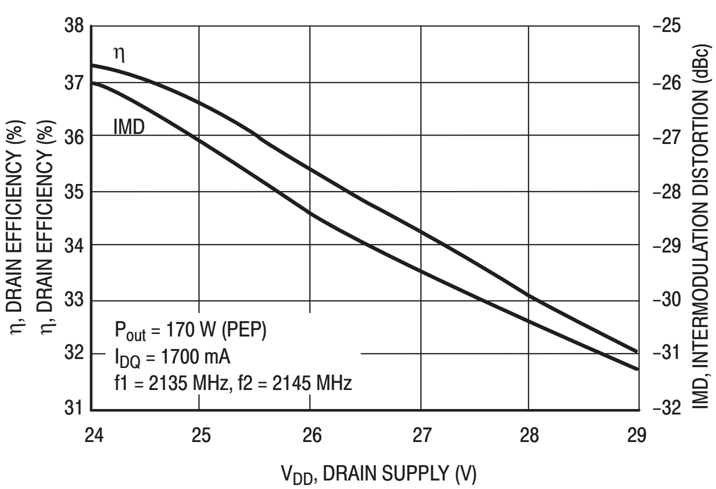


Figure 8. Two–Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

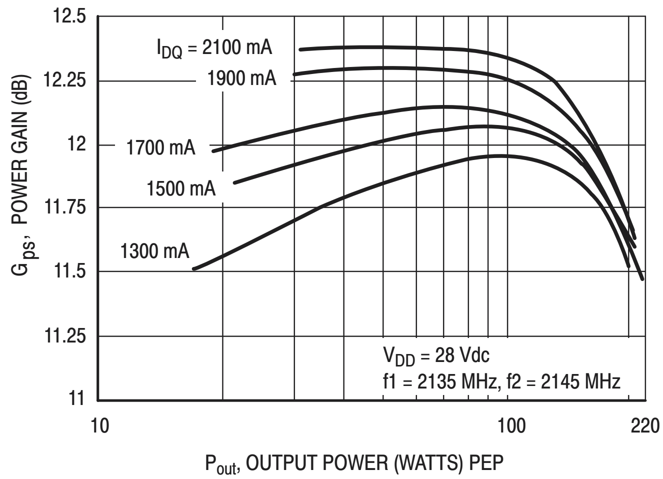


Figure 9. Two-Tone Power Gain versus Output Power

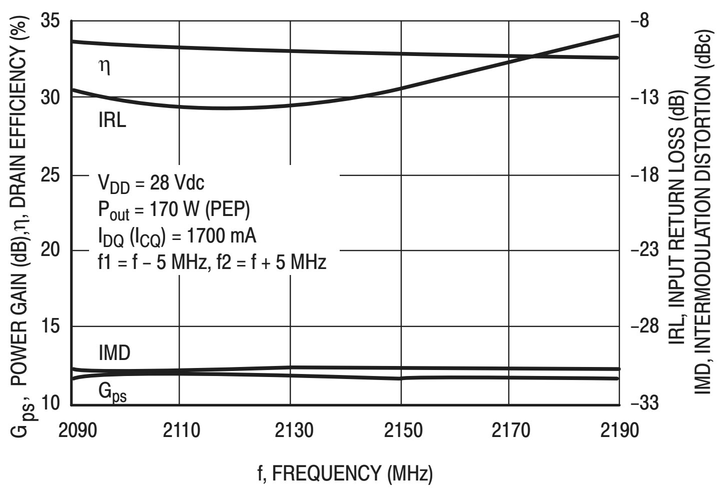


Figure 10. Two-Tone Broadband Performance

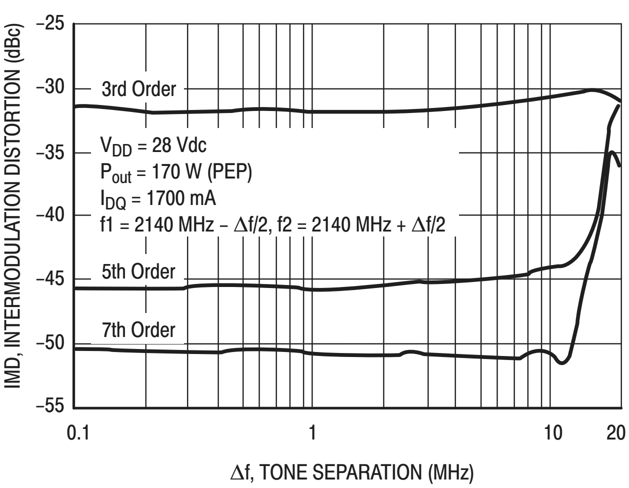


Figure 11. Intermodulation Distortion Products versus Two–Tone Spacing

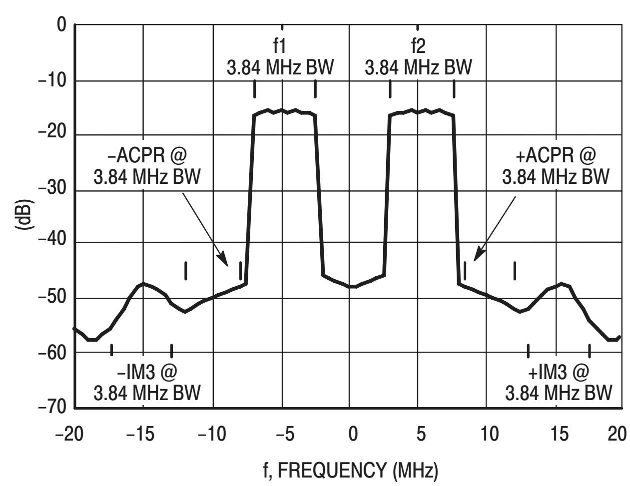
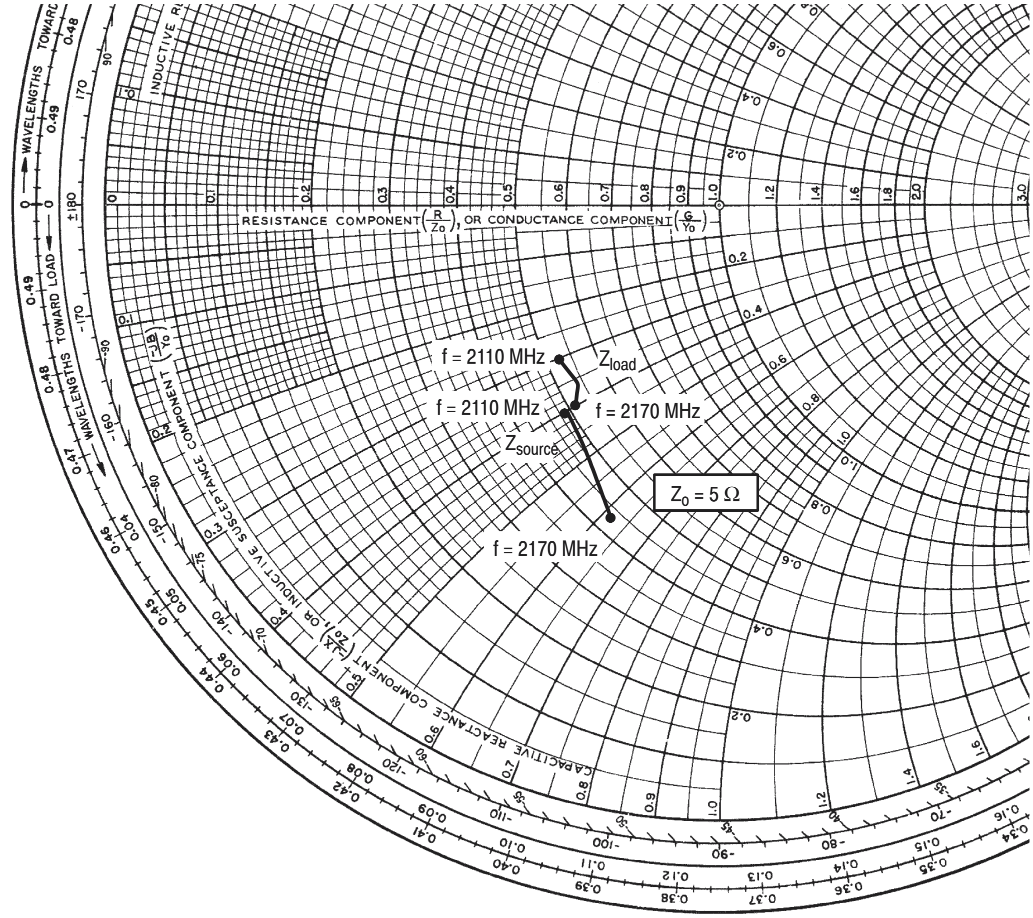


Figure 12. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 2 X 850 mA, P_{out} = 38 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
2110	2.45 – j2.08	2.65 – j1.52
2140	2.39 – j2.51	2.71 – j1.80
2170	2.16 – j3.14	2.64 – j2.04

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

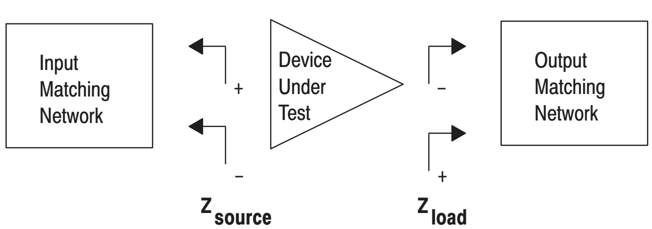
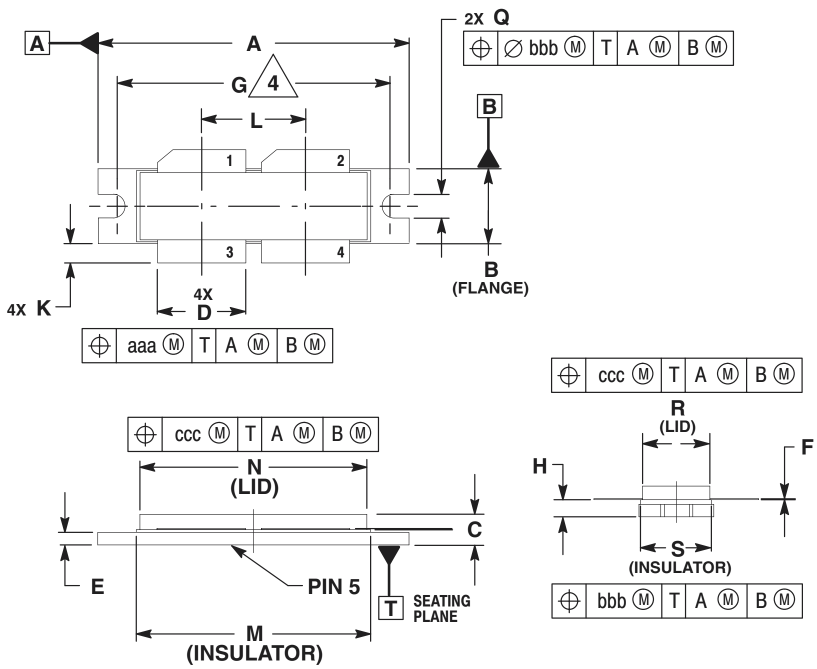


Figure 13. Series Equivalent Input and Output Impedance

NOTES

NOTES

PACKAGE DIMENSIONS

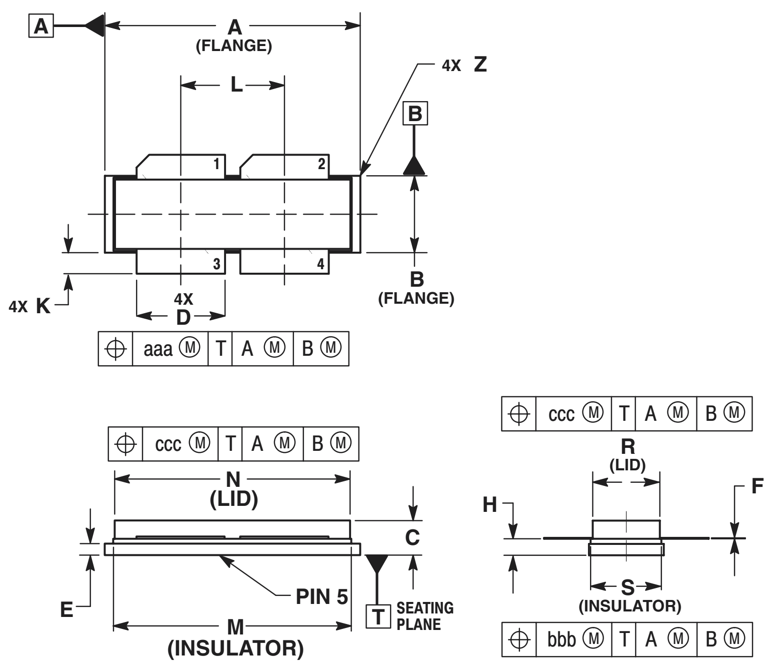


CASE 375D–04
ISSUE C
NI–1230
MRF21180

NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
G	1.400 BSC		35.56 BSC	
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
Q	0.120	0.130	3.05	3.30
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE



CASE 375E–03
ISSUE C
NI–1230S
MRF21180S

NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.325	1.335	33.66	33.91
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
Z	0	0.040	0	1.02
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

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