MOTOROLA

MC3480

Advance Specifications and Applications Information

DYNAMIC
MEMORY CONTROLLER

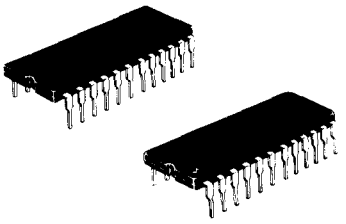
SCHOTTKY MONOLITHIC
INTEGRATED CIRCUIT

MEMORY CONTROLLER FOR 16 PIN 4K AND 16K DYNAMIC RAMs

The memory controller chip is designed to greatly simplify the interface logic required to control the popular 16 pin 4K or 16K dynamic NMOS RAM in a microprocessor system such as the M6800. The controller will generate, on command from the microprocessor, the proper timing signals required to successfully transfer data between the microprocessor and the NMOS memories. The controller, in conjunction with an oscillator, will also generate the necessary signals required to insure that the dynamic memories are refreshed for the retention of data.

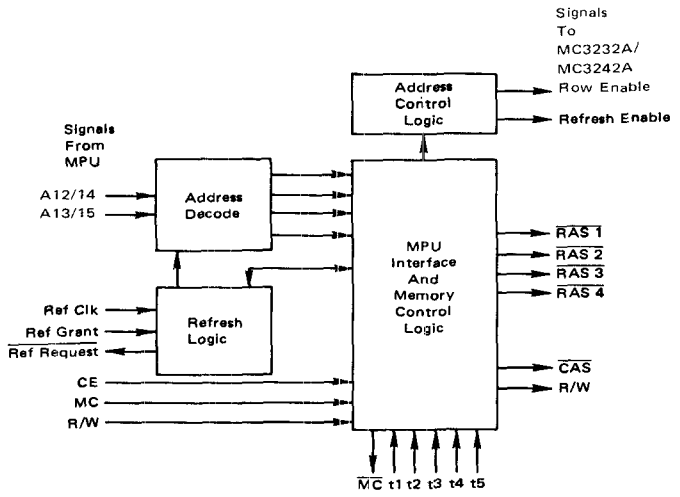
- Greatly Simplify the MPU-Dynamic Memory Interface
- Reduce Package Count and System Access/Cycle Times 30%
- Chip Enable for Expansion to Larger Word Capacity
- Generate 1 of 4 $\overline{RAS}$ Signals for an Optimum 16K/64K Memory System
- High Input Impedance for Minimum Loading of MPU Bus
- Schottky TTL Technology for High Performance
- Useful with 4K and 16K and Future Expanded Dynamic RAMs

L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649

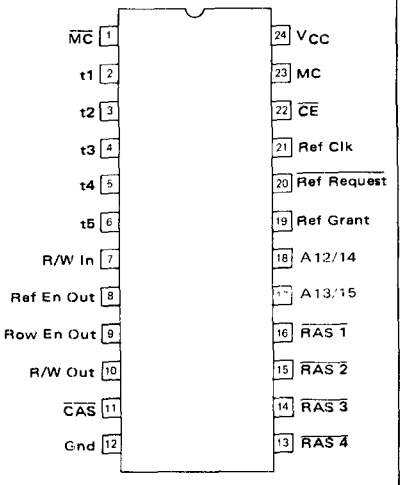
BLOCK DIAGRAM



Several methods may be employed to generate the required time delay:

1. One shots
2. High frequency counters
3. High frequency shift registers
4. Delay lines
5. Signals from MPU Clock

PIN CONNECTIONS



See Pin Descriptions

This is advance information and specifications are subject to change without notice.

ADI-517

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	-0.5 to +7.0	Vdc
Output Voltage	V_O	-0.5 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Due to the advanced nature of this specification, final electrical limits are not yet given on all parameters. A final version may be obtained after October, 1978 by writing:

Motorola Linear IC Marketing – M250
P.O. Box 20912
Phoenix, AZ 85036

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-250	μA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	–	–	40 100	μA
Input Clamp Voltages (I_{IC} 18 mA)	V_{IC}	–	–	-1.5	V
Output Voltage – Low Logic State (I_{OL} = 24 mA for $\overline{RAS}$, $\overline{CAS}$, and R/W) (I_{OL} = 8.0 mA for Row En, Ref En, $\overline{MC}$, $\overline{Ref\ Req}$)	V_{OL}	 – –	 – –	 0.5 0.5	V
Output Voltage – High Logic State (I_{OH} = -1.0 mA for $\overline{RAS}$, $\overline{CAS}$, and R/W) (I_{OH} = -0.4 mA for Row En, Ref En, and $\overline{MC}$) I_{OH} = -0.2 mA for $\overline{Ref\ Req}$ (Note: $\overline{Ref\ Req}$ output has internal 5.0 k resistive pullup to V_{CC}.)	V_{OH}	 3.0 2.4 2.4	 – – –	 – – –	V
Power Supply Current	I_{CC}	–	–	70	mA
Output Short-Circuit Current (V_{OL} = 0 V for Row En, Ref En, and $\overline{MC}$)	I_{OS}	-10	–	-55	mA

SWITCHING CHARACTERISTICS Typical values measured at V_{CC} = 5.0 V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
MC to $\overline{MC}$	tPMC	–	8	–	
t1 to $\overline{RAS}$	tPT1	–	30	–	
t2 to Row En	tPT2	–	30	–	
t3 to $\overline{CAS}$	tPT3	–	30	–	
t4 to R/$\overline{W}$	tPT4	–	30	–	
t5 to $\overline{CAS}$, $\overline{RAS}$	tPT5A	–	30	–	
t5 to R/W, Row En, Ref En	tPT5	–	45	–	
Ref Clk to $\overline{Ref\ Req}$	tPCQ	–	45	–	
Ref Grant to Row En or Ref En	tPGR	–	30	–	
t1 to $\overline{Ref\ Req}$ (Refresh Cycle only)	tPTQ		30		
Setup Times					ns
Ref Clk before Ref Grant	tSCG	–	30	–	
A12, A13 before t1	tSAT	–	-10	–	
R/W Input before t4	tSRW	–	10	–	
$\overline{CE}$ before t1	tSCE	–	15	–	
Hold Times					ns
A12, A13 after t5	tHAT	–	10	–	
$\overline{CE}$ after t1	tHCE	–	0	–	
R/W after t4	tHRW	–	0	–	
Minimum Delay Times (see Note 2)	tDEL				ns
t1 Low to High to t2 Low to High	(1-2)	–	30	–	
t1 Low to High to t4 Low to High	(1-4)	–	30	–	
t2 Low to High to t3 Low to High	(2-3)	–	30	–	
t3 Low to High to t5 Low to High	(3-5)	–	30	–	

Note 2: If delays between pins are less than the minimum specified, the succeeding outputs may not switch.

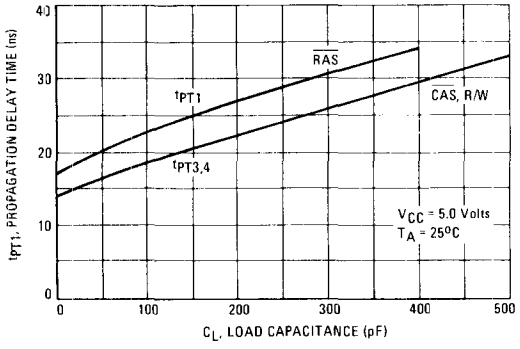
AC Loads (Note 3)

R/$\overline{W}$ and $\overline{CAS}$ Outputs	450 pF to Gnd*
$\overline{RAS}$ Outputs	150 pF to Gnd*
$\overline{MC}$, Row En, Ref En, and $\overline{Ref\ Req}$ Outputs	15 pF to Gnd*

*Includes probe and jig capacitance.

NOTE 3: All outputs can drive larger capacitive loads than those shown with a small decrease in speed. See Figure 1.

FIGURE 1 – TYPICAL $t_{PT1,3,and\,4}$ (HIGH TO LOW) versus LOAD CAPACITANCE – $\overline{RAS}$, $\overline{CAS}$ and R/$\overline{W}$



PIN DESCRIPTION TABLE

Name	No.	Function
$\overline{RAS1}$ *	16	Row Address Strobe pins which connect to each of the dynamic RAMs to latch in Row Address on memory chips. Decoded to 1 of 4 during R/W cycle. All 4 go low during refresh cycle.
$\overline{RAS2}$	15	
$\overline{RAS3}$	14	
$\overline{RAS4}$	13	
$\overline{CAS}$ *	11	Column Address Strobe pin which connects to each dynamic RAM to latch in column address.
R/W Out *	10	This pin signals the dynamic RAM whether the RAM is to be read from or written into.
Row En	9	Row Enable output which goes to the MC3232A (MC3242A). It signals the Address Multiplexer that the lower half (Row Addresses) or the upper half (Column Addresses) of the address lines are to be multiplexed into the dynamic RAM address inputs. A Logic 1 on this output indicates the Row Addresses, and a Logic 0 indicates Column Addresses.
Ref En	8	Refresh Enable output. A Logic 1 signals the Address Multiplexer that a refresh cycle is to be done, and a Logic 0 indicates that address multiplexing should be done.
$\overline{CE}$	22	Chip Enable Input. A Logic 1 on this pin disables all chip functions, except that of Refresh and the $\overline{MC}$ output. $\overline{CE}$ must be low during t1 low to high transition to initiate R/W cycle. Once t1 is initiated, the cycle is independent of $\overline{CE}$.
R/W In	7	The Read/Write input pin receives information from the M6800 MPU as to the direction of data exchange in the dynamic RAM. It transmits a Logic 0 to the R/W output for a Write Cycle and a Logic 1 for a Read Cycle.
A12 (A14)	17	Upper Order Address lines from the M6800. These two inputs decode to four signals controlling the four $\overline{RAS}$ outputs. A14 and A15 apply to 16K RAMs.
A13 (A15)	18	
MC	23	Memory Clock input which comes from the microprocessor clock generator. This input must rise after the rising edge of t1 to avoid a potential internal race condition.
$\overline{MC}$	1	The complement of MC. It is a buffered output which may be used to drive the circuitry creating the time delays used on inputs t2 through t5.
t1	2	These pins use external timing delays to sequentially select the outputs to be enabled. They are positive-edge triggered inputs. Assuming a Read/Write cycle is to be executed, a positive edge on t1 forces a logic 0 on one of the four $\overline{RAS}$ outputs as determined by the A12/14, A13/15 inputs. After a delay, a positive edge on t2 causes Row En to go to a Logic 0, providing address-multiplexing information to the MC3232A or MC3242A. t3 enables the $\overline{CAS}$ output and it goes low. t4 enables the R/W output and it goes low, assuming the R/W input was low. t5 resets all the outputs to a Logic 1 (with the exception of $\overline{MC}$, Ref En, and $\overline{Ref\ Req}$). The inputs t1, t2, t3, and t5 are daisy-chained, so they must be sequentially driven to obtain the desired output signals. t4 can be driven at any time after t1.
t2	3	
t3	4	
t4	5	
t5	6	
Ref Clk	21	The 32 kHz (64 kHz) Refresh Clock signals this pin that another refresh cycle is required. It is a positive-edge triggered input, and upon triggering, the $\overline{Ref\ Req}$ pin goes to a Logic 0.
$\overline{Ref\ Req}$	20	The Refresh Request output acts as an input to the MPU system, requesting a refresh cycle. This output has a 5 kΩ pullup resistor to the V_{CC} supply to allow wire-ORing if desired.
Ref Grant	19	Through the Refresh Grant input, the MC6875 initiates a refresh cycle. This input is positive-edge triggered and is enabled only after the $\overline{Ref\ Req}$ pin has gone low. This allows the MC3480 to discern between a Refresh Grant or a DMA Grant even though they appear on the same line. When employing both dynamic memory (refresh) and DMA in a microprocessor-based system with a combined Refresh/DMA Request control on the clock, provision must be made for holding off a DMA request during a refresh period (and visa versa). If this provision is not made, clock stretching (cycle stealing) will continue indefinitely and dynamic microprocessor data will be lost. The positive edge on Ref Grant causes Row En output to go low and Ref En output to go high. This signals the MC3232A (MC3242A) that a refresh address is required. The refresh cycle occurs with the succeeding pulses on t1-t5. A positive edge on t1 causes $\overline{Ref\ Req}$ to go high and all the $\overline{RAS}$ outputs to go low. A positive going edge on t2 causes no change in the outputs, since it controls the address multiplexing (Row En) during the Read/Write cycles. There is no output change when t5 and t4 go high because no $\overline{CAS}$ or R/W signal is needed during refresh. A positive edge on t5 resets the $\overline{RAS}$ to a Logic 1 state, and Ref En to a Logic 0 state, ready for the next Read/Write cycle.
V_{CC}	24	+5.0 V supply. A 0.1 μF capacitor is recommended to bypass pin 24 to ground.
Gnd	12	System Ground.

*These outputs are designed to drive the highly capacitive inputs of multiple dynamic RAMS/(150 pF for $\overline{RAS}$ outputs, and 450 pF for $\overline{CAS}$ and R/W outputs). Consequently, these outputs have no short circuit limit and must be handled accordingly.
Note: All other outputs are LS TTL totem pole configuration unless otherwise noted. Good high capacitance load driving techniques usually include a 10Ω or greater series damping resistor. It is highly recommended that this be done on $\overline{RAS}$, $\overline{CAS}$ and R/W outputs of the MC3480.

TIME DELAY INFORMATION

TIMING REQUIREMENT CONSTRAINTS

Δt1 — Minimum is determined by MPU Address Delay (t_{AD}), plus RAM Row Address Set-Up Time (t_{ASR}), minus MC3480 Propagation Delay (t_{pT1}).

Δt2 - Δt1 — Minimum is determined by RAM Row Address Hold Time (t_{RAH}) minus the minimum MC3232A/3242A Row Enable to Output Delay (t_{00MIN}).*

Δt3 - Δt2 — Minimum is determined by RAM Column Address Set-Up Time ($t_{ASC\ minimum}$) plus maximum MC3232A/3242A Row Enable to Output Delay (t_{001MAX}).*

Δt4 - Δt3 — No Minimum

Δt5 - Δt3 — Minimum is determined by RAM minimum $\overline{CAS}$ Pulse Width (t_{CAS}) or Access Time from $\overline{CAS}$ (t_{CAC}) plus Data Set-Up Time of MPU (t_{DSR}).

Δt5 - Δt4 — Minimum is determined by the RAM minimum Write Pulse Width (t_{WP}).

*The MC3480 has propagation delays also, but they cancel each other in these delay requirements.

Note: Also required in computing time delays are the various delays incurred by the particular delay scheme used; i.e., delays between $4 \times f_o$, $2 \times f_o$, and f_o from the MC6875 which are used as inputs or the gate delays of the gates used in Figures 4A through 4C.

TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs

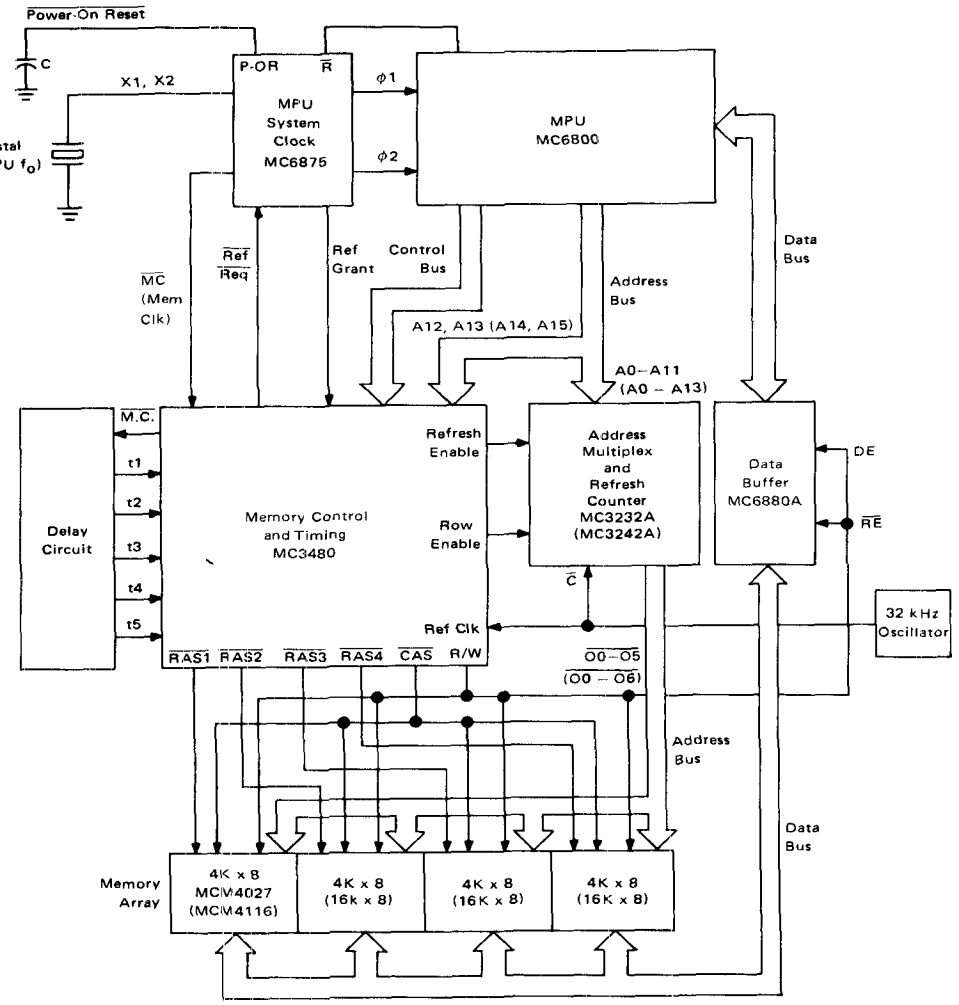


FIGURE 2 – READ/WRITE TIMING CYCLE

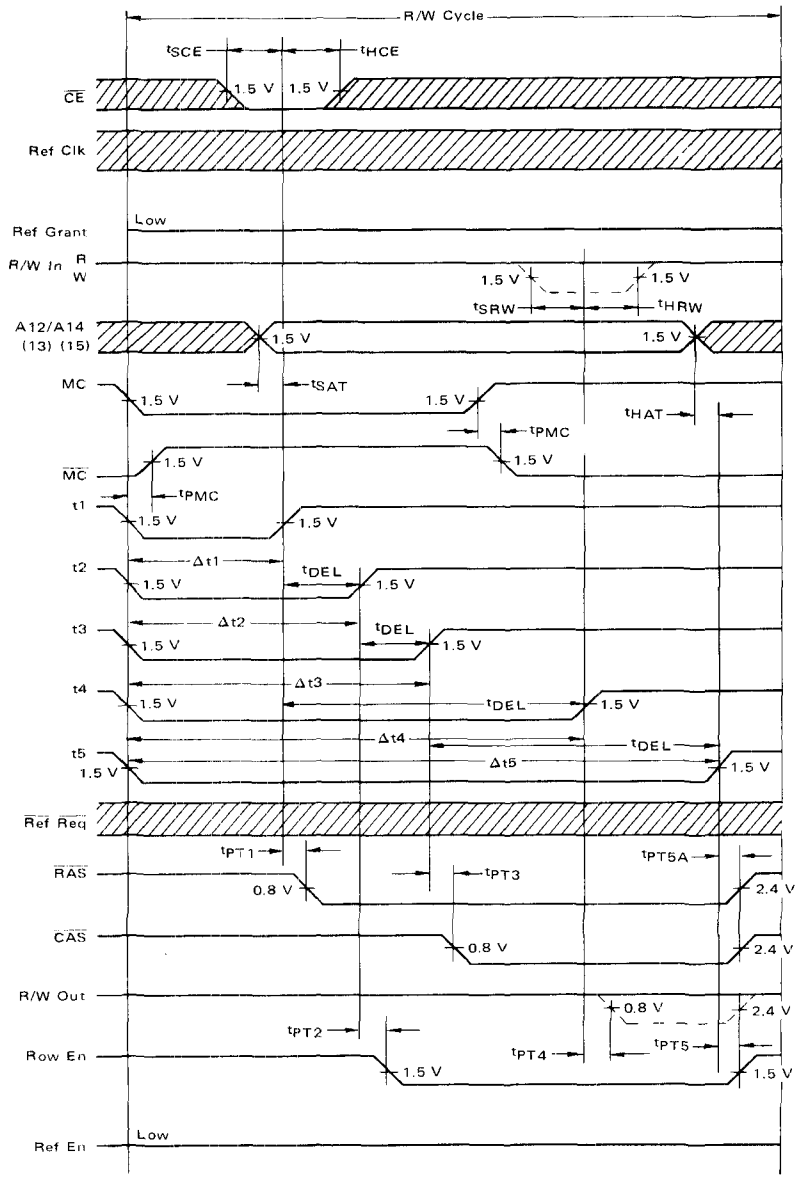
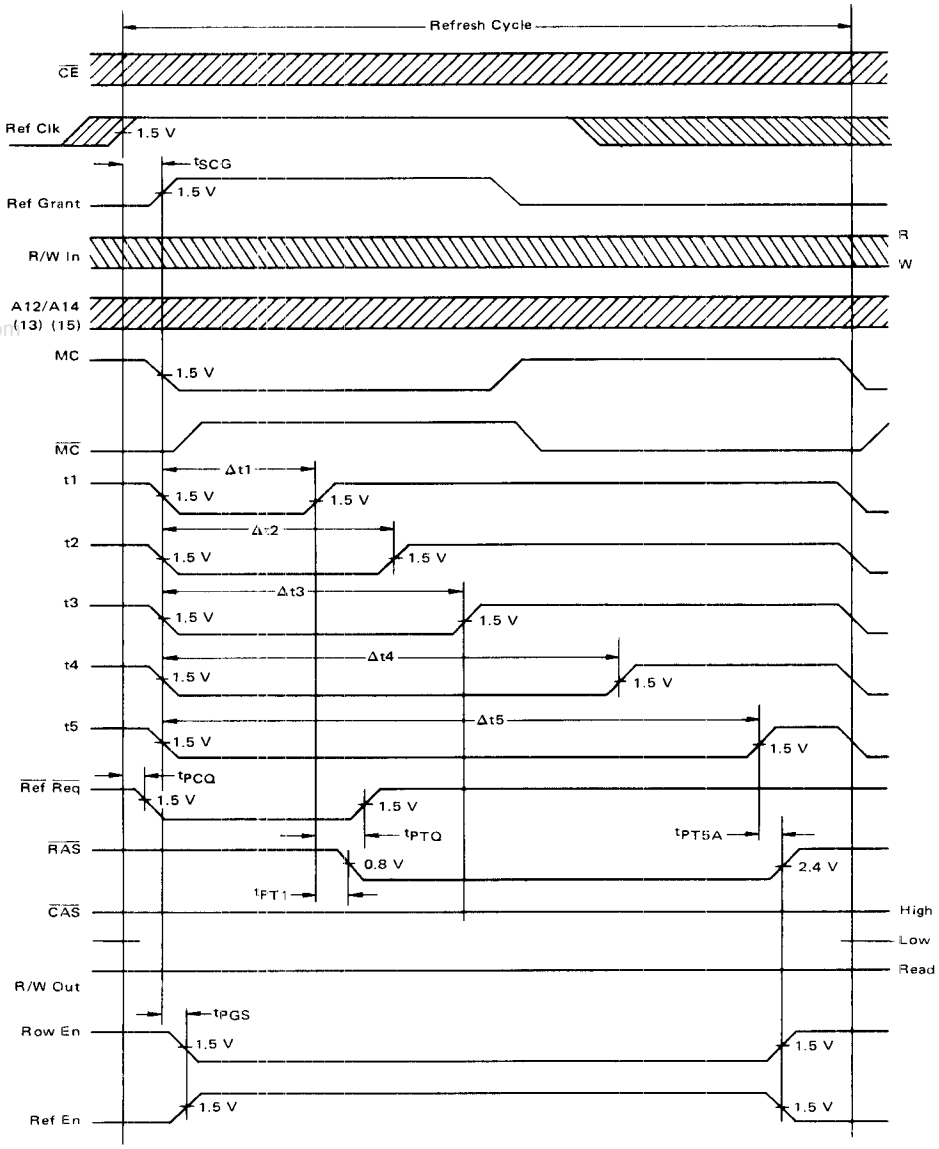


FIGURE 3 – REFRESH TIMING CYCLE

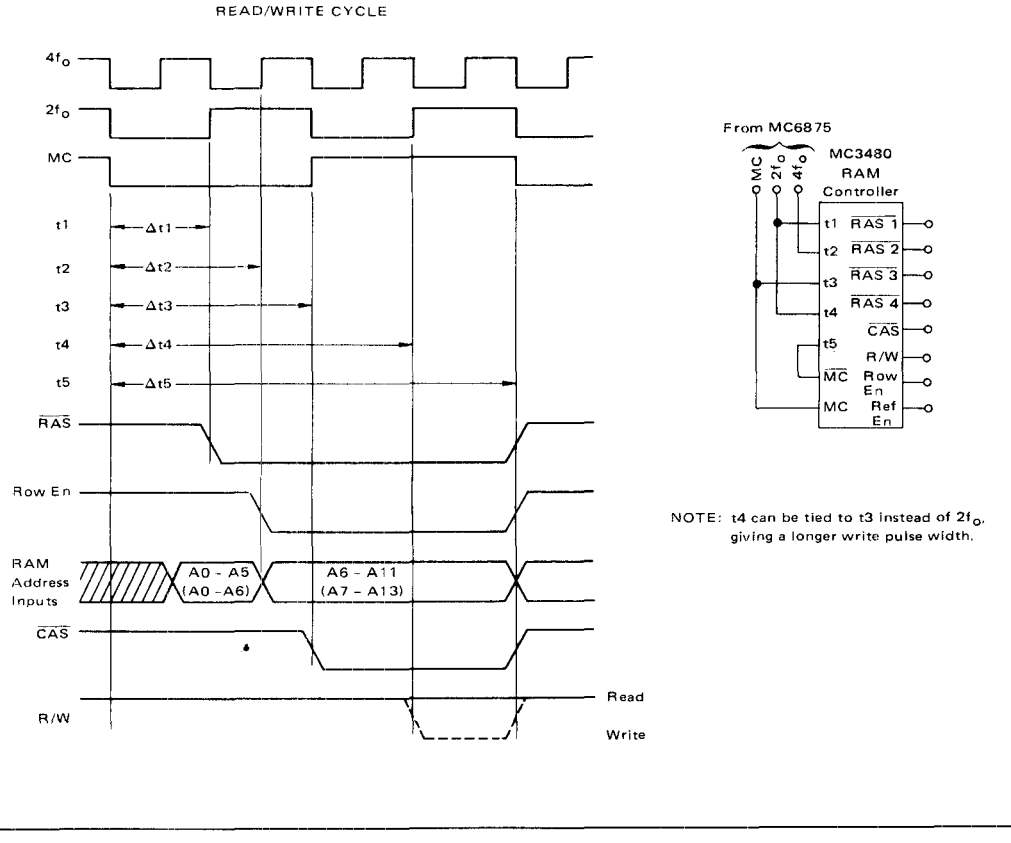


APPLICATIONS INFORMATION

GENERAL DESCRIPTION

The MC3480 uses five general timing inputs in place of a master clock with on-chip timing generation. This gives the system designer optimum flexibility in interfacing with the various microprocessor families and dynamic memories that are available. In simpler slow speed systems, the timing signals required can be directly obtained from those available from the microprocessor. In systems requiring high speed memory/microprocessor cycle times, timing input t1-t5 can be obtained using delay lines or a range of techniques as shown in Figures 4 thru 8. It is only necessary to maintain the time delay relationships shown under time delay information.

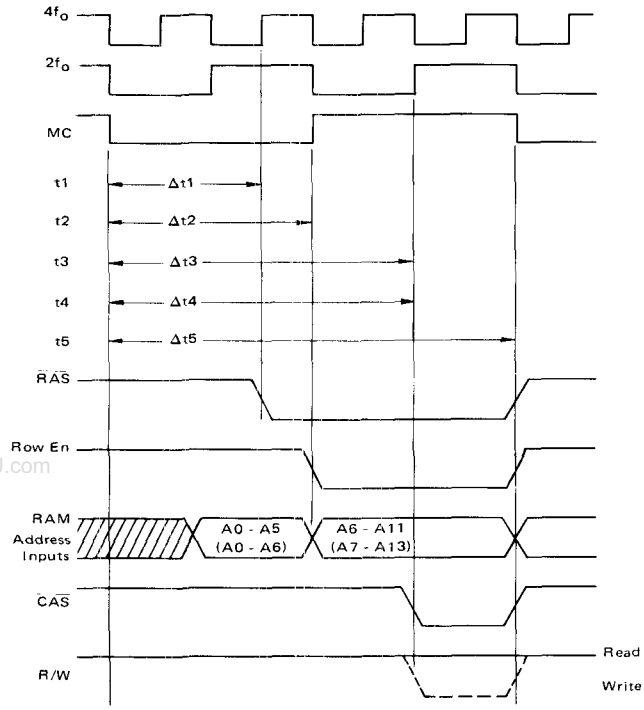
FIGURE 4 -- UNIVERSAL TIME DELAY USING MC6875

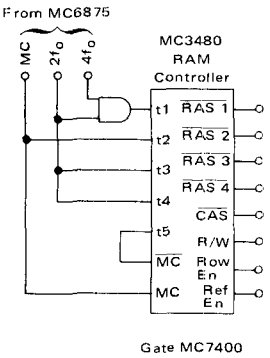


NOTE: t4 can be tied to t3 instead of $2f_o$, giving a longer write pulse width.

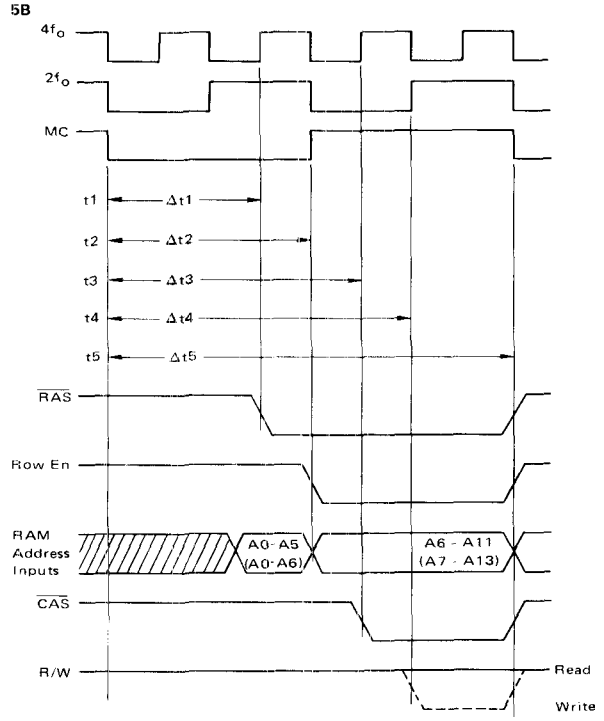
FIGURE 5 – ALTERNATE TIME DELAYS USING MC6875
(Read/Write Cycle Shown)

5A





5B



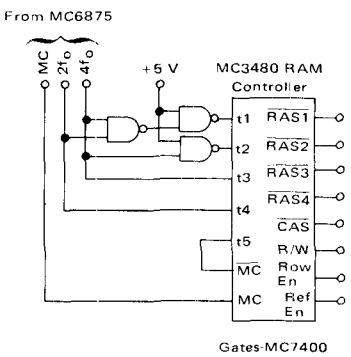
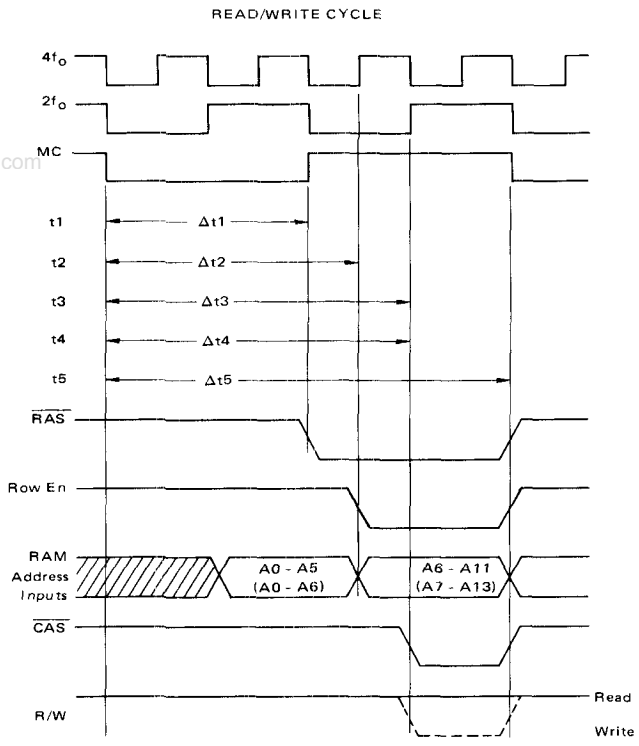
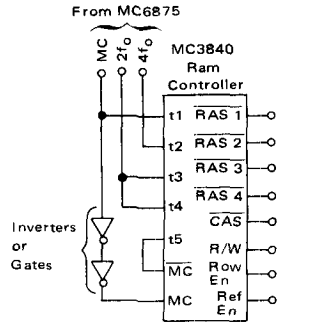


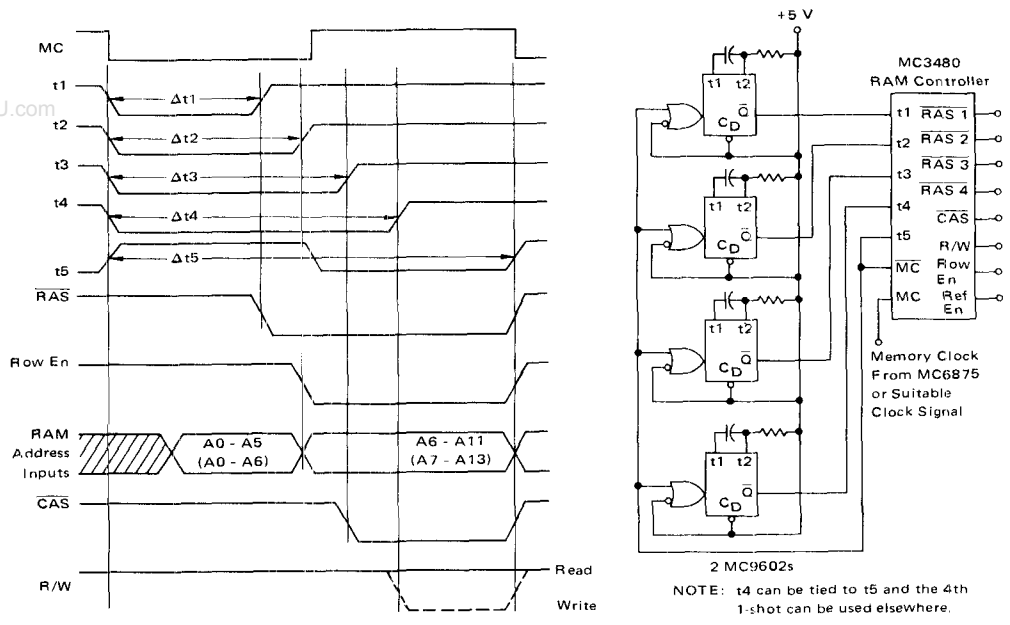
FIGURE 5C – ALTERNATE TIME DELAYS USING MC6875





NOTE: MC of MC3480 is delayed by two gate delays after t1 because of possible race problems, if they are wired together.

FIGURE 6 – ONE SHOT TIME DELAY METHOD



NOTE: t4 can be tied to t5 and the 4th 1-shot can be used elsewhere.

FIGURE 7 – DELAY LINE TIME DELAY METHOD

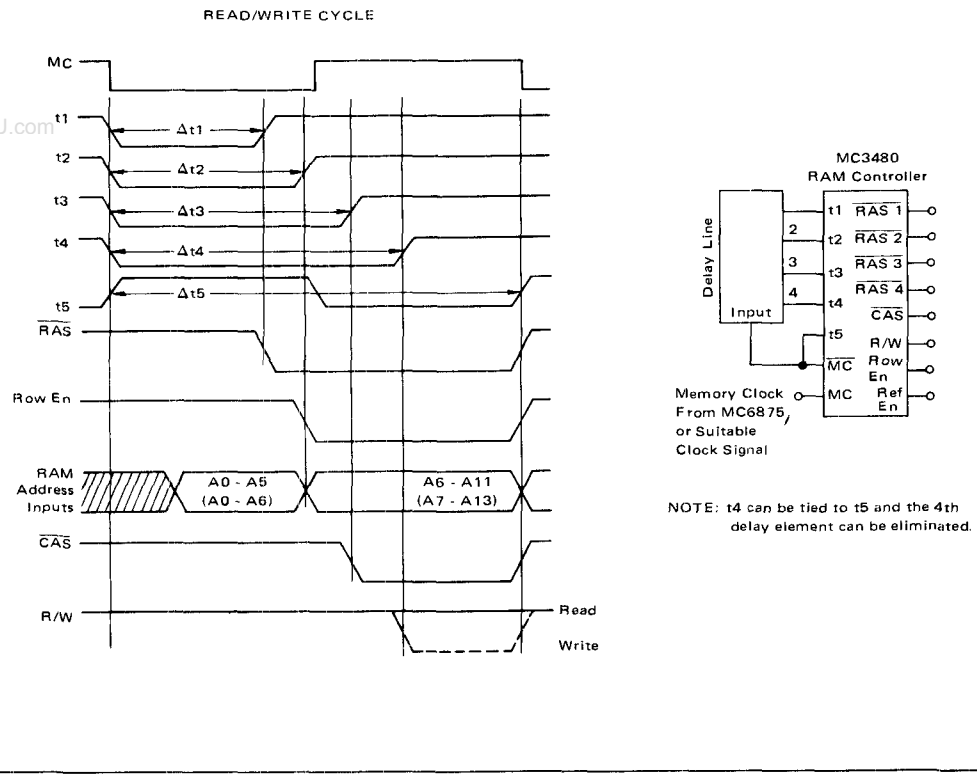
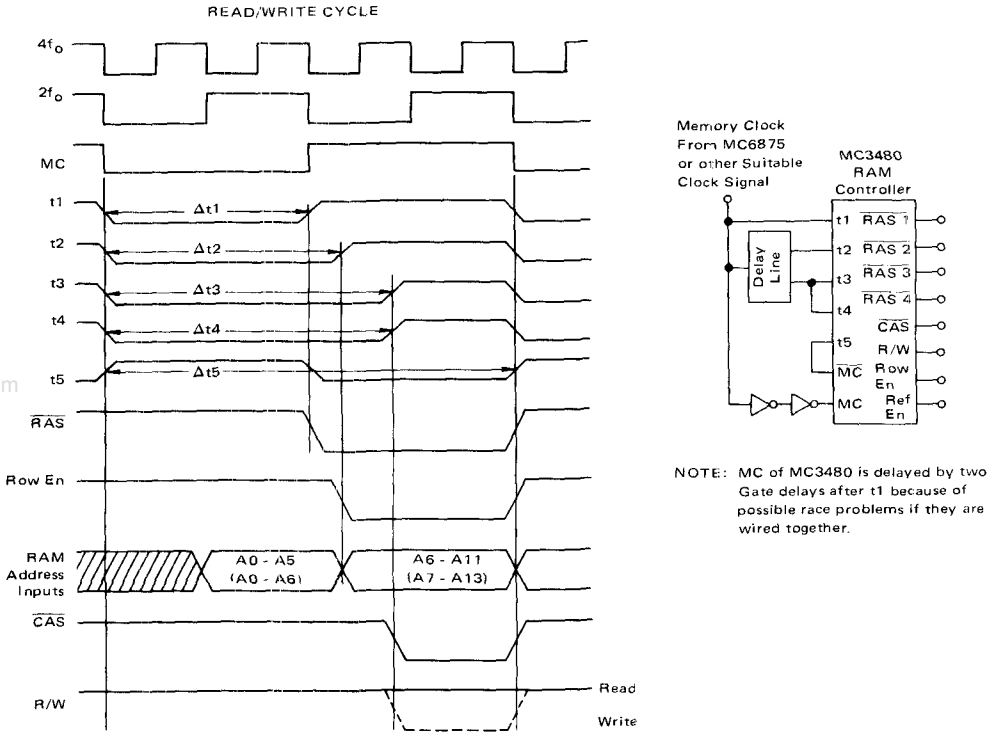


FIGURE 8 – DELAY LINE TIME DELAY (ALTERNATE METHOD)



NOTE: MC of MC3480 is delayed by two Gate delays after t1 because of possible race problems if they are wired together.

REFRESH CONSIDERATIONS

The MC3480/MC3232A (MC3242A) memory control system can be used with either cycle steal or transparent refresh methods. Figure 9 shows one transparent technique employing refresh during $\phi 2$ low in an M6800 microprocessor-based system. Using this technique requires that the memory be capable of completing a Read/Write Cycle and a Refresh Cycle sequentially during the M6800 cycle. The minimum cycle time at the time of printing for dynamic multiplexed RAMs is 320 ns, therefore limiting the mciroprocessor to 1.56 MHz operation. The D flip-flops of Figure 9 produce a trigger at the beginning of both $\phi 1$ and $\phi 2$. For a 1.0 MHz system, the t1–t5 inputs should be adjusted so that the following conditions occur at the specified period after the beginning of a cycle:

$\overline{RAS}$ falls at 100 ns (triggered by t1)
Row In falls at 200 ns (triggered by t2)
$\overline{CAS}$, R/W falls at 250 ns (triggered by t3)
t5 rises at 450 ns.

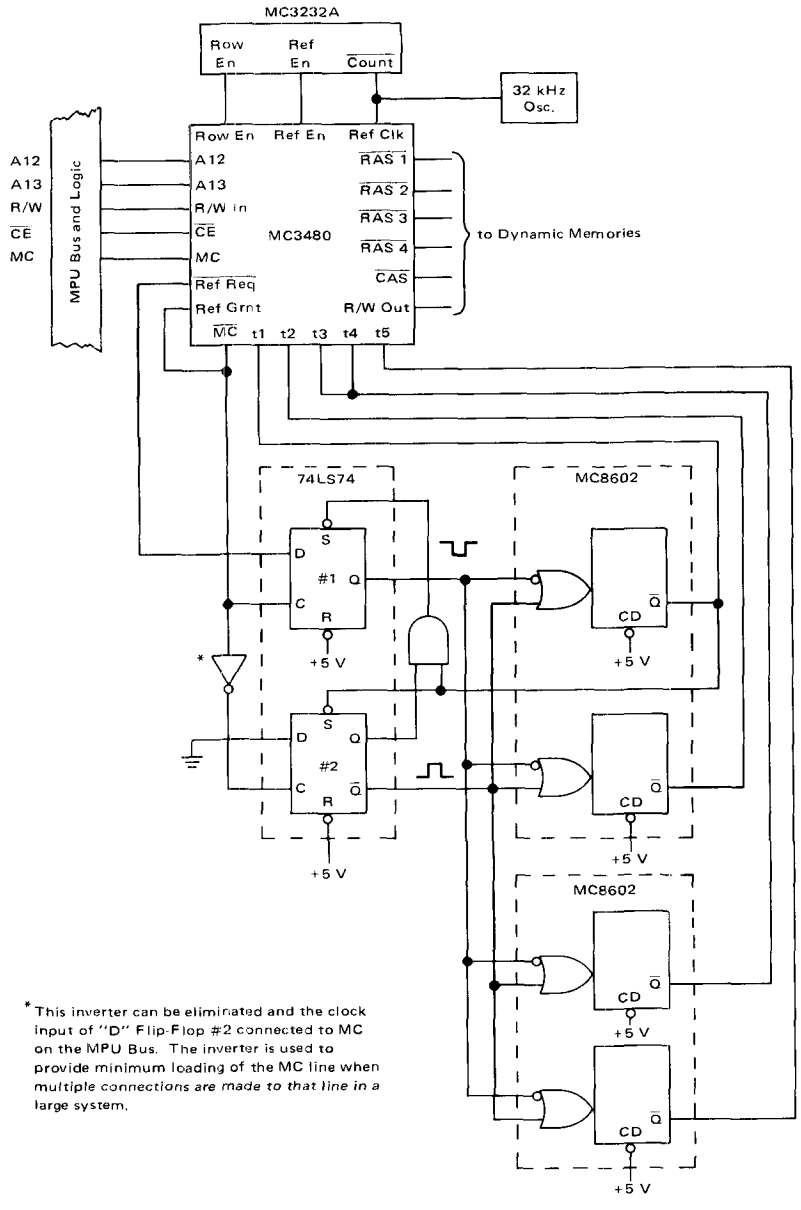
A delay line could be used to generate t1-t5 in place of the four monostables. For the 1.0 MHz system, it would require either two 5 tap delay lines with 50 ns per tap or a 10 tap line with 50 ns/tap. For use with a 600 kHz system, a delay line with 5 taps of 150 ns each could be used. For this case:

$\overline{RAS}$ falls at 150 ns
Row En falls at 300 ns
$\overline{CAS}$, R/W falls at 450 ns
t5 rises at 750 ns

Figure 10 shows typical refresh oscillator configurations for both 32 kHz (f_{REF} min for 4K) and 64 kHz (f_{REF} min for 16K). In the case of transparent refresh, if the designer is not concerned with power consumption, the refresh oscillator may be eliminated and the Ref Clk input connected to the MC input yielding a refresh every $\phi 1$.

For DMA operation combined with cycle stealing refresh, care must be taken not to allow a DMA request during a $\overline{\text{Refresh Request}}$/Grant period and to hold off a refresh during a DMA operation. See comments under pin descriptions, Pin 19.

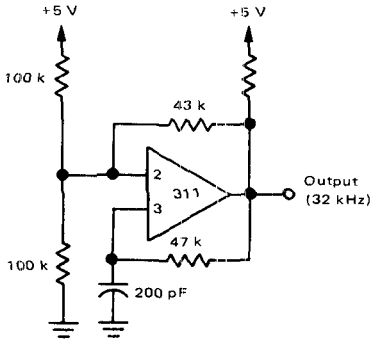
FIGURE 9 -- EXAMPLE OF $\phi 2$ LOW METHOD OF HIDDEN REFRESH USING MC3480 AND 4K RAMS



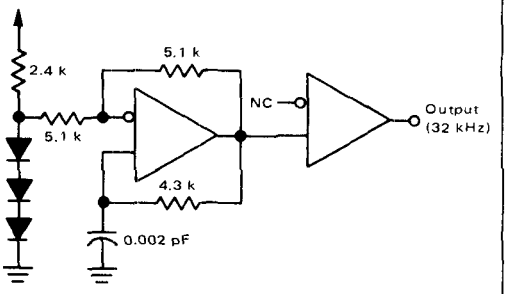
*This inverter can be eliminated and the clock input of "D" Flip-Flop #2 connected to MC on the MPU Bus. The inverter is used to provide minimum loading of the MC line when multiple connections are made to that line in a large system.

FIGURE 10 – SUGGESTED 32 kHz OSCILLATORS

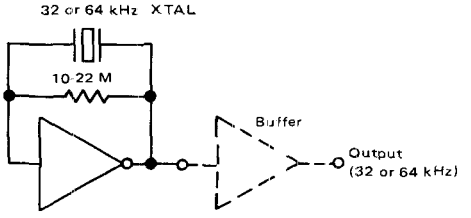
MLM311



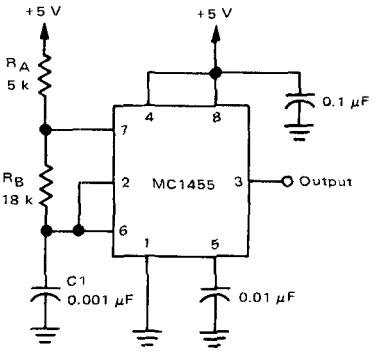
MC75140



OSCILLATOR USING ANY CMOS INVERTER

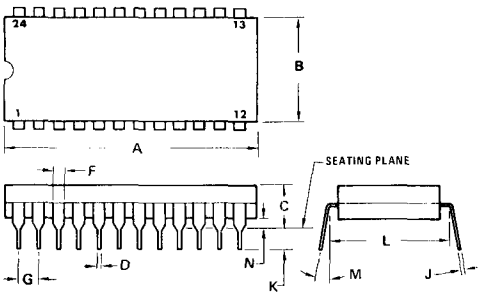


MC1455 OSCILLATOR (32 kHz COMPONENTS SHOWN)



For 64 kHz Example $R_A = 2.5$ k, $R_B = 9.0$ k, $C1 = 0.001\ \mu F$

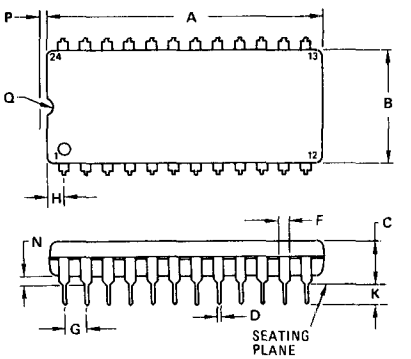
$$f_o = \frac{1.44}{(R_A + 2R_B)\,C1}$$



L SUFFIX
CERAMIC PACKAGE
CASE 623-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)



P SUFFIX
PLASTIC PACKAGE
CASE 649-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

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