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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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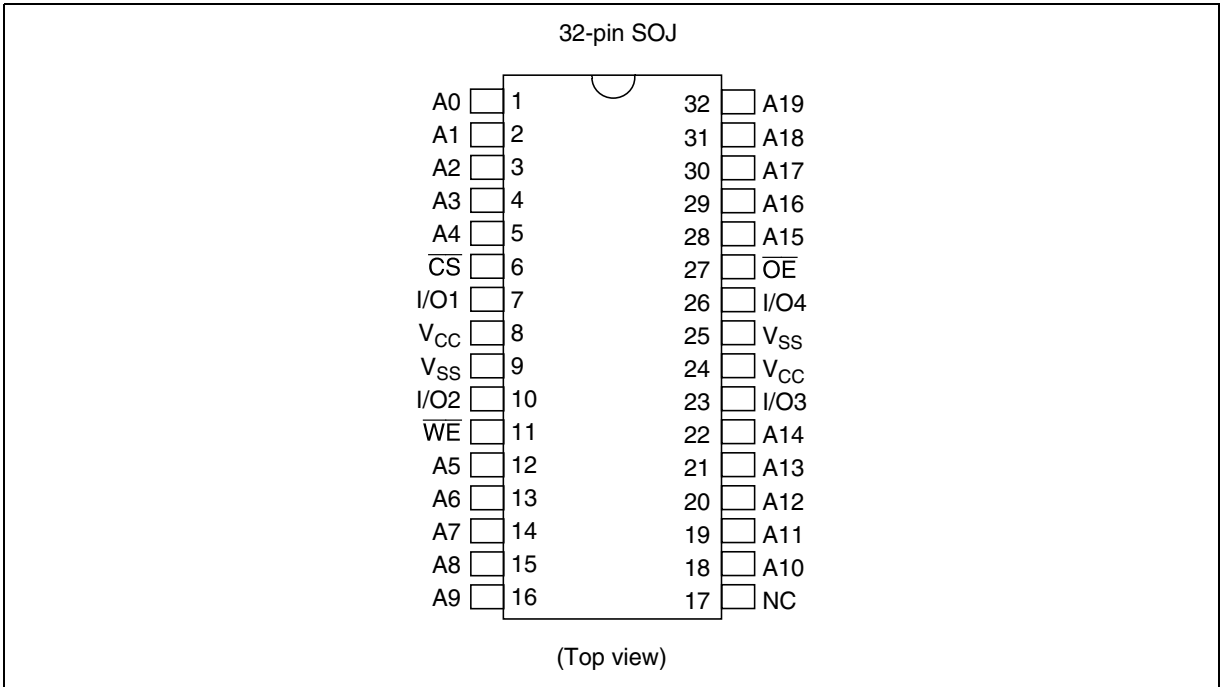
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HM624100HC Series

Ordering Information

Type No.	Access time	Device marking	Package
HM624100HCJP-10	10 ns	HM624100CJP10	400-mil 32-pin plastic SOJ (CP-32DB)
HM624100HCJP-12	12 ns	HM624100CJP12	
HM624100HCLJP-10	10 ns	HM624100CLJP10	
HM624100HCLJP-12	12 ns	HM624100CLJP12	

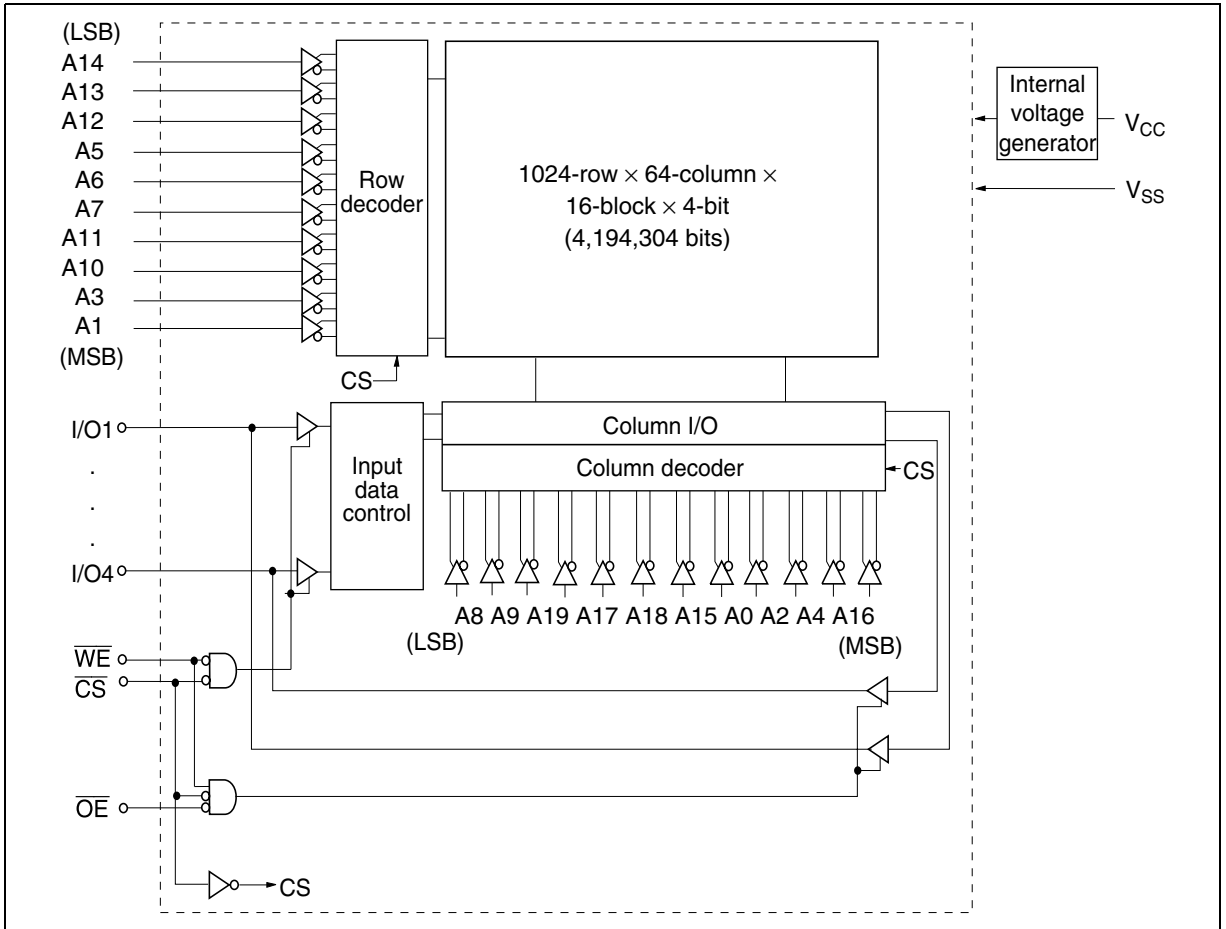
Pin Arrangement



Pin Description

Pin name	Function
A0 to A19	Address input
I/O1 to I/O4	Data input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram



Operation Table

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} current	I/O	Ref. cycle
H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disable	I_{CC}	High-Z	—
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC}+0.5$ * ²	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to +85	°C

Notes: 1. V_T (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_T (max) = $V_{CC} + 2.0$ V for pulse width (over shoot) ≤ 6 ns.

Recommended DC Operating Conditions

($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC} * ³	4.5	5.0	5.5	V
	V_{SS} * ⁴	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.5$ * ²	V
	V_{IL}	-0.5* ¹	—	0.8	V

Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns.

2. V_{IH} (max) = $V_{CC} + 2.0$ V for pulse width (over shoot) ≤ 6 ns.

3. The supply voltage with all V_{CC} pins must be on the same level.

4. The supply voltage with all V_{SS} pins must be on the same level.

HM624100HC Series

DC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions	
Input leakage current	I_{LI}	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}	
Output leakage current	I_{LO}	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}	
Operation power supply current	10 ns cycle	I_{CC}	—	—	140	mA	Min cycle $\overline{CS} = V_{IL}$, $I_{out} = 0\text{ mA}$ Other inputs = V_{IH}/V_{IL}
	12 ns cycle	I_{CC}	—	—	130	mA	
Standby power supply current	I_{SB}	—	—	40	mA	Min cycle, $\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL}	
	I_{SB1}	—	2.5	5	mA	f = 0 MHz $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2\text{ V}$, (1) $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2\text{ V}$	
	—* ²	—	0.6* ²	1.2* ²	—	—	
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8\text{ mA}$	
	V_{OH}	2.4	—	—	V	$I_{OH} = -4\text{ mA}$	

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristics is guaranteed only for L-version.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* ¹	$C_{I/O}$	—	—	8	pF	$V_{I/O} = 0\text{ V}$

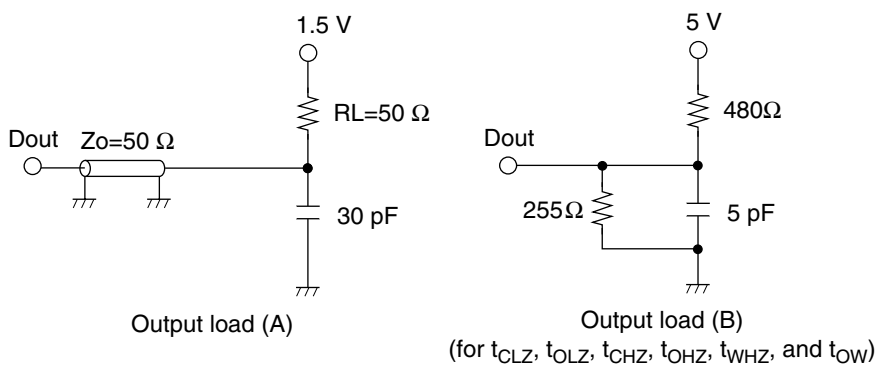
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM624100HC				Unit	Notes
		-10		-12			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	10	—	12	—	ns	
Address access time	t_{AA}	—	10	—	12	ns	
Chip select access time	t_{ACS}	—	10	—	12	ns	
Output enable to output valid	t_{OE}	—	5	—	6	ns	
Output hold from address change	t_{OH}	3	—	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	5	—	6	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	ns	1

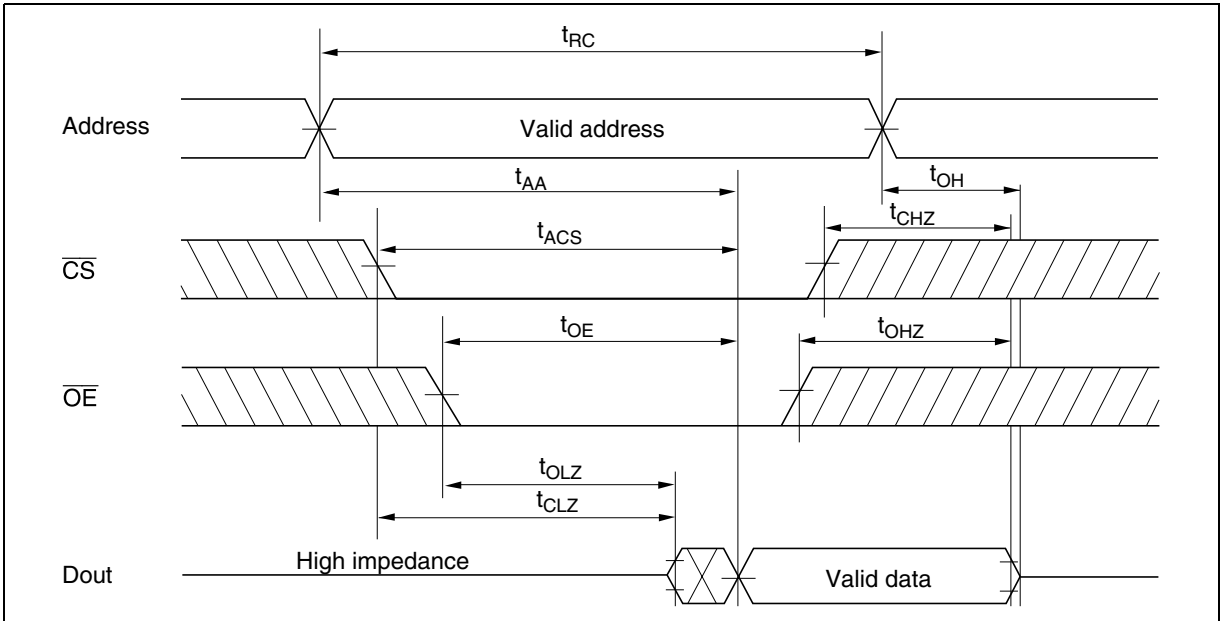
Write Cycle

Parameter	Symbol	HM624100HC				Unit	Notes
		-10		-12			
		Min	Max	Min	Max		
Write cycle time	t_{WC}	10	—	12	—	ns	
Address valid to end of write	t_{AW}	7	—	8	—	ns	
Chip select to end of write	t_{CW}	7	—	8	—	ns	9
Write pulse width	t_{WP}	7	—	8	—	ns	8
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	5	—	6	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	5	—	6	ns	1
Write enable to output in high-Z	t_{WHZ}	—	5	—	6	ns	1

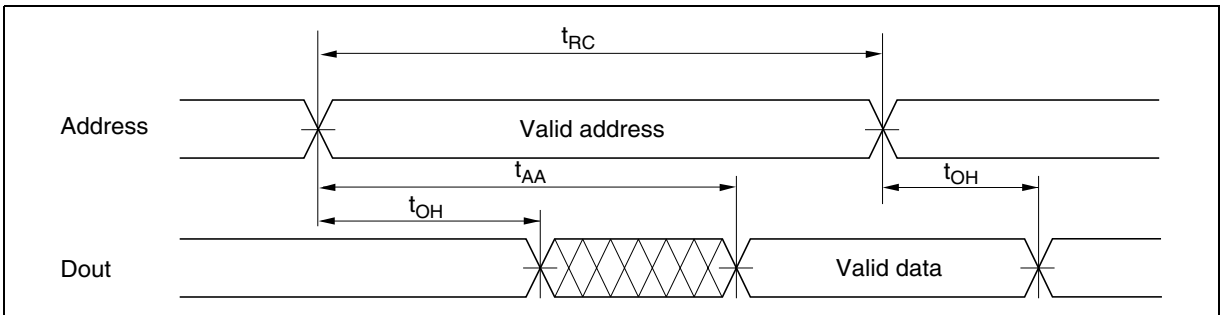
- Note:
1. Transition is measured ± 200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
 2. Address should be valid prior to or coincident with \overline{CS} transition low.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. If \overline{CS} and \overline{OE} are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
 5. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 6. t_{AS} is measured from the latest address transition to the later of \overline{CS} or \overline{WE} going low.
 7. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the first address transition.
 8. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going low and \overline{WE} going low. A write ends at the earliest transition among \overline{CS} going high and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 9. t_{CW} is measured from the later of \overline{CS} going low to the end of write.

Timing Waveforms

Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

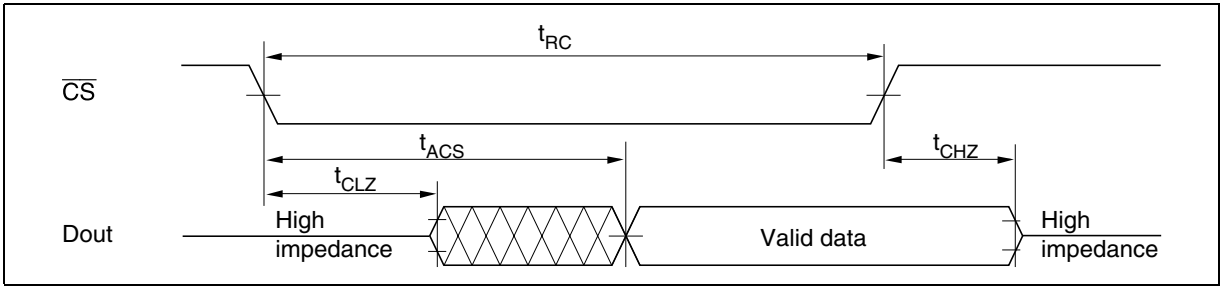


Read Timing Waveform (2) ($\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$)

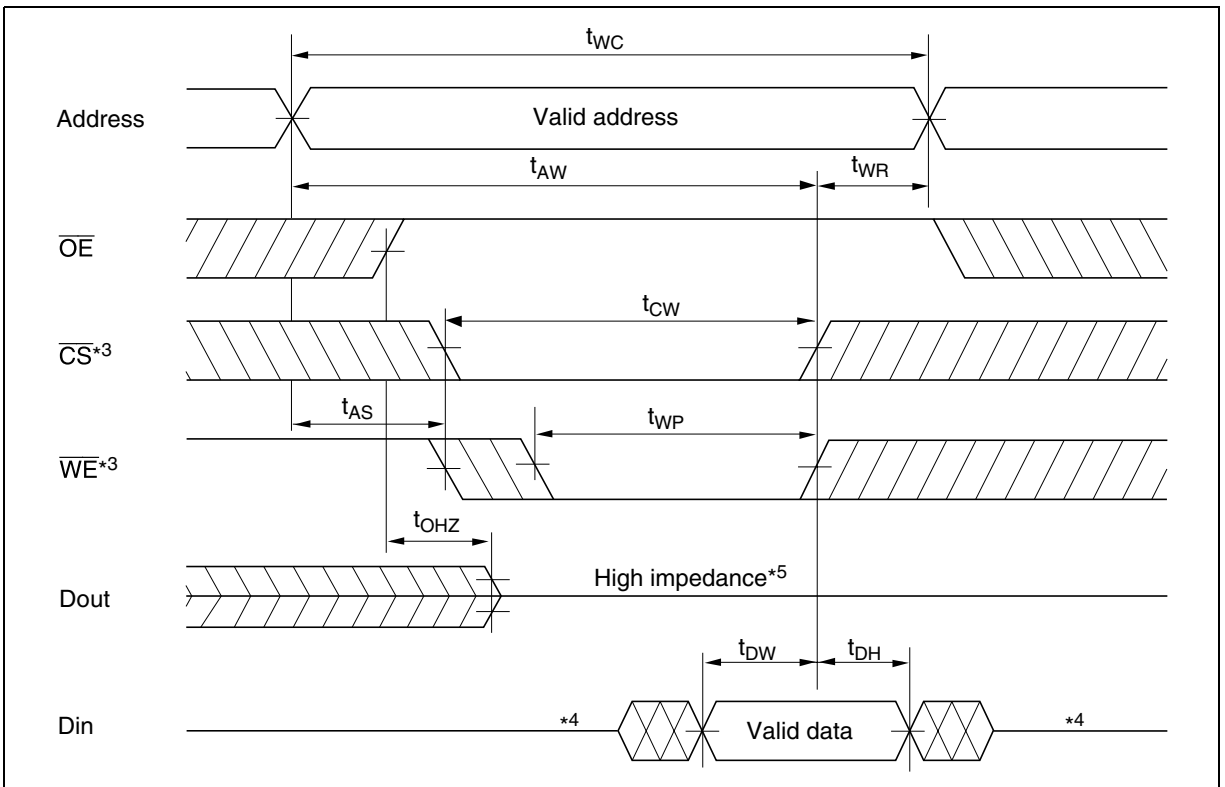


HM624100HC Series

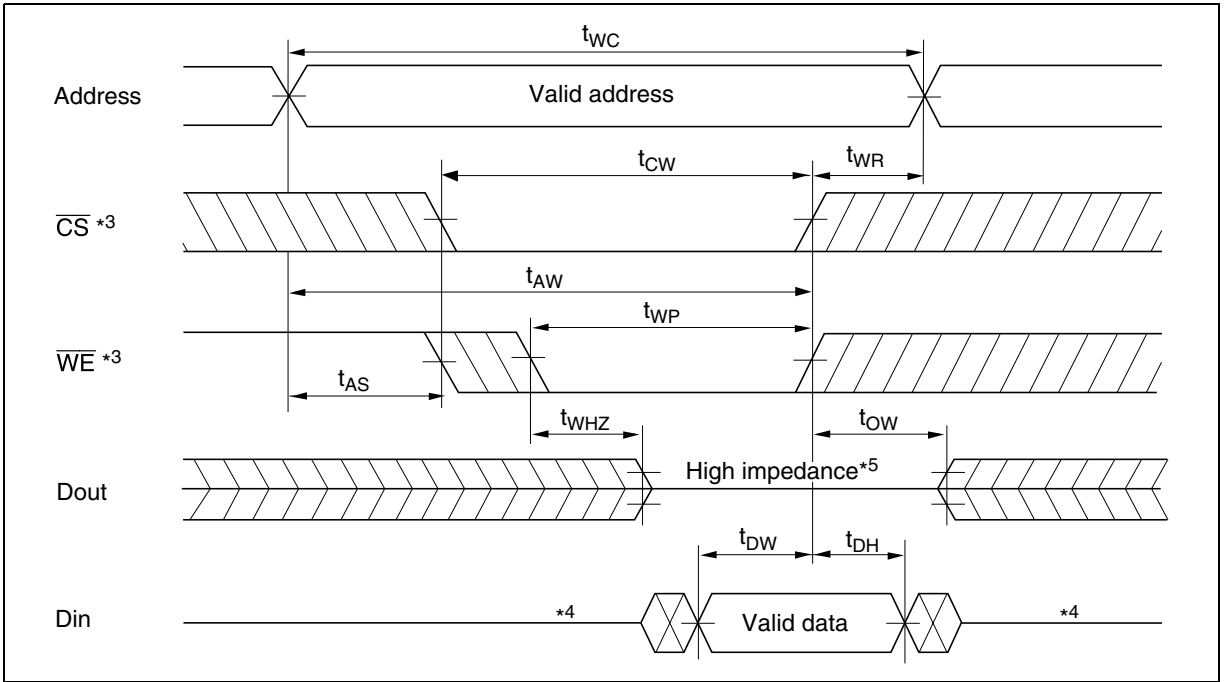
Read Timing Waveform (3) ($\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$)*²



Write Timing Waveform (1) (\overline{WE} Controlled)



Write Timing Waveform (2) (\overline{CS} Controlled)



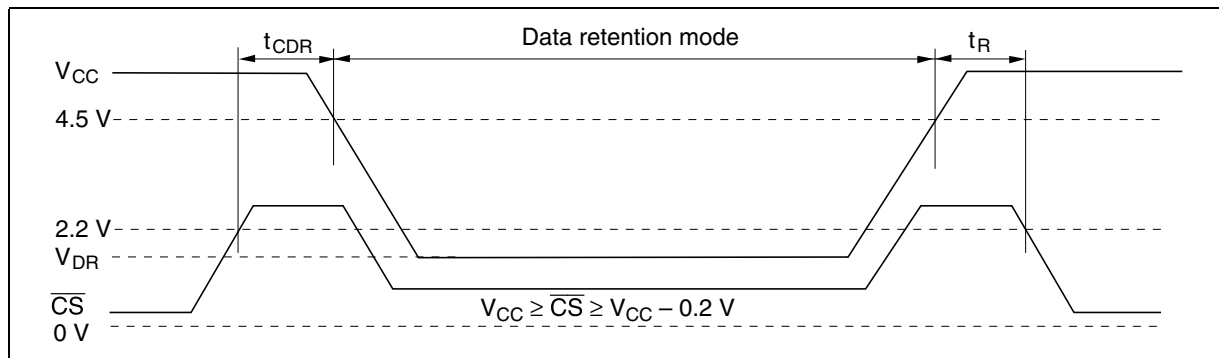
Low V_{CC} Data Retention Characteristics

($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V \leq $V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	—	800	μA	$V_{CC} = 3$ V, $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V (1) 0 V \leq $V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

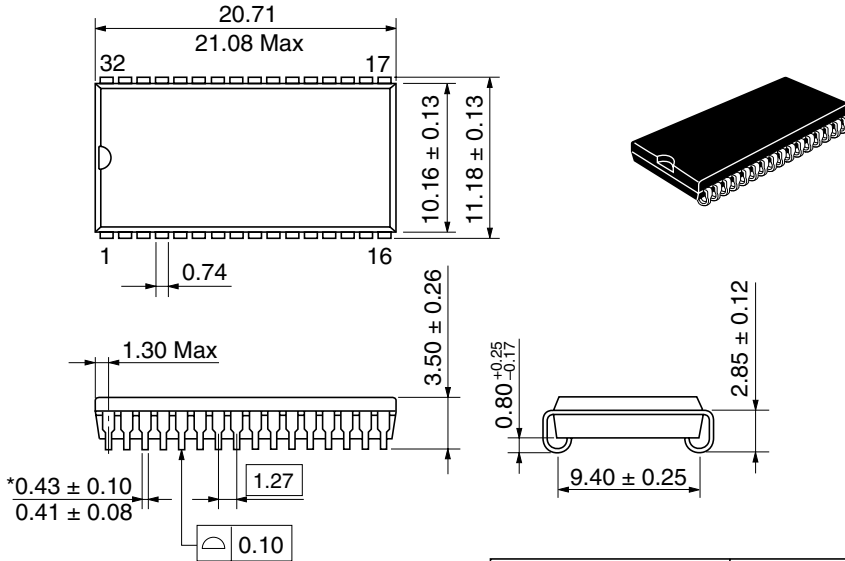
Low V_{CC} Data Retention Timing Waveform



Package Dimensions

HM624100HC/JP/HCLJP Series (CP-32DB)

As of July, 2002
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	CP-32DB
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.2 g

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