VTC Inc.
Value the Customer™

VM443
READ DATA PULSE QUALIFIER

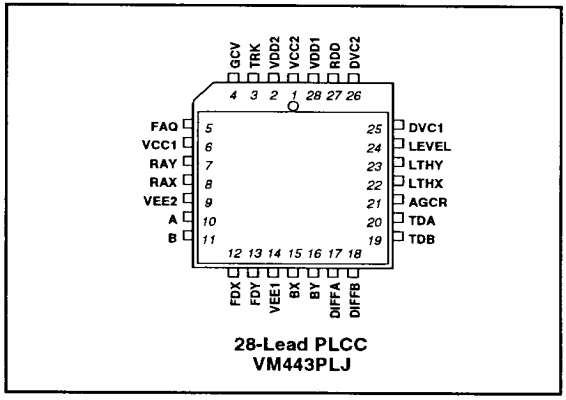
Refer to Application Note APN-1 and APN-2

July, 1992

FEATURES

- Operates with MFM, (2,7) or (1,7) RLL Codes
- Data Rates up to 20 Mbit/s (2,7) Code
- Fast Acquisition Mode for Rapid AGC Acquisition, 25µs max.
- Impedance Switch for Suppressing Capacitively-coupled Input Transients, 10:1 Impedance Change Ratio
- Pulse Pairing Grades of 2ns and 5ns Max Available
- Time and Gating Channel Pulse Qualification Based on Three Criteria: Pulse Amplitude, Width, and Slope
- AGC and Differentiator Time Constants Set by External Components
- Adjustable AGC Output Magnitude and Noise Threshold
- Adjustable Input Signal Amplitude Range
- Adjustable Validation Threshold Level
- Standard TTL Digital Inputs and Outputs
- Operates on Standard +5V, +12V Drive Supplies
- Available in 28-Lead PDIP or PLCC

CONNECTION DIAGRAM

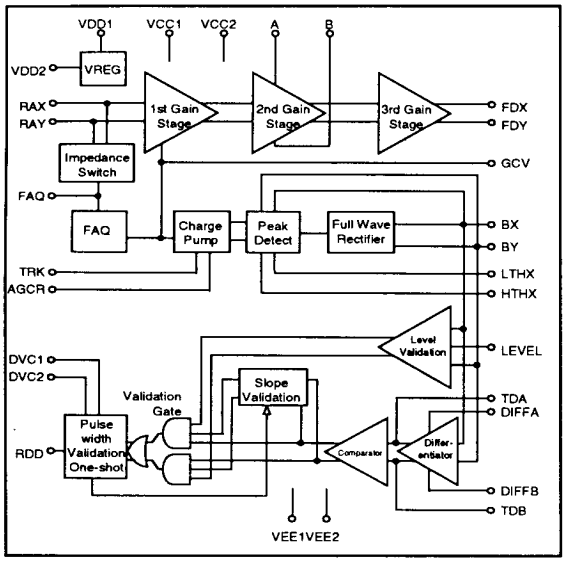


28-Lead PLCC
VM443PLJ

DESCRIPTION

The VM443 Read Data Pulse Qualifier is a bipolar integrated circuit used in rigid disk drives to provide complete read data signal processing. The VM443 accepts the differential capacitively-coupled signal from a read/write preamp integrated circuit. The positive and negative amplitude peaks of the input signal are detected and their time position is accurately replicated. The peak timing information is contained in the rising edge of an output TTL pulse. The rising edges of an output TTL pulse string represent valid flux reversals on the magnetic medium.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage:
- V_{DD1} 14V
- V_{CC1}, V_{CC2} 6V

TTL Input Voltage 5.5V
TTL Output Voltage 5.5V
AGC Differential Input Voltage ..... ± 2.4Vp-p
Validation Differential Input Voltage ..... ± 8Vp-p
Storage Temperature ..... -55° to 150°C
Lead Temperature (soldering 10 seconds) ..... 300°C
Thermal Characteristics, Θ_{JA}:
- Junction Temperature ..... 150°C
- 28-Lead PLCC ..... 53°C/W
- 28-Lead PDIP ..... 68°C/W

Power Dissipation at 25°C:
- 28-Lead PLCC 1560mW
- 28-Lead PDIP 1950mW

RECOMMENDED OPERATING CONDITIONS

Supply Voltage:
- V_{DD1} ..... 12V ± 10%
- V_{CC1}, V_{CC2} ..... 5V ± 10%
- Ambient Temperature T_A, ... 0 to 70°C

CIRCUIT OPERATION

The VM443 has two main sections: the AGC amplifier, and the pulse validation circuitry which is composed of the time and gating channels. The AGC circuitry contains a high bandwidth three-stage amplifier, full-wave rectifier, peak detector, and charge pump. The fast acquisition and impedance switch circuits can be used to reduce the AGC signal acquisition time. The validation circuitry includes a precision high speed differentiator and comparator. Other circuitry is included to qualify data pulses based on three criteria:

1. The pulse amplitude must be greater than the validation threshold level.
2. Pulses must be separated by a minimum time.
3. Alternating pulses must have opposite polarity.

After a pulse is validated, a TTL output pulse is generated by a one-shot circuit.

AGC Operation

Large input signal amplitude variations are expected due to head, disk and preamp variations. The input signal must be normalized to some known constant magnitude so that reliable pulse validation can be performed. If the signal used for validation is too small, then internal circuitry offsets could become a concern. Conversely, if the validation signal is too large, then it could be distorted if the amplifier clips or saturates. The VM443 will accept input signals with a wide magnitude range and produce a constant nominal 3.5Vp-p AGC output signal.

The AGC action begins by sensing if the input signal magnitude is larger than the low-level threshold. If it is, the charge pump pulls current out of the capacitor connected to the GCV pin, causing the gain of the amplifier to ramp upward. As the magnitude of the output signal appearing on the BX and BY pins crosses the high level threshold, the peaking flip-flop is set, telling the charge pump to inject current into the capacitor connected to the GCV pin. This ramps the gain of the amplifier down. After the AGC loop locks, the gain ramps up and down only a small amount, presenting a very smooth amplified waveform with a magnitude determined by the high level threshold at the BX and BY pins. When the AGC is locked and steady state the duty cycle of the pump up waveform will exactly equal the duty cycle of the pump down waveform, causing no net gain change at the amplifier output.

AGC ADJUSTMENT

The analog preamplified signal from the disk drive is capacitively coupled into the RAX and RAY pins of the VM443. The value of the coupling capacitors along with the impedance looking into the RAX and RAY pins forms a high pass filter. The roll-off frequency of the filter characteristic should be set so that it occurs at least 1.7 decades below the input signal fundamental frequency. This will minimize the phase distortion of the input signal due to the phase characteristics of the filter. The lower limit of the roll-off frequency is determined by the required system AGC access time. If the roll-off frequency is too low, the filter will be slow to recover from large differential transients, much as might be seen in a head select operation. This will greatly increase the AGC access time. The 1.7 decade frequency roll-off value is a good compromise between the two performance considerations.

The AGC amplifier is comprised of three gain stages. The first stage performs the AGC action, adjusting the gain through negative feedback until the output magnitude at the FDX and

FDY pins is correct. The second gain stage has adjustable gain so that the input range of the AGC amplifier can be customized. The gain of the second stage can be expressed by

$$A_{V2} = 6000 / Z_1$$

where Z_1 is the impedance connected externally between the A and B pins. If the impedance between the A and B pins is doubled, the gain of the second stage is reduced by half, and the input magnitude range is doubled to 50 to 600mVp-p. By reducing Z_1 by half, the gain of the second stage is doubled, and the input range is reduced to 12.5 to 150mVp-p. The roll-off frequency of the network connected between the A and B pins should be chosen to be much lower than the fundamental frequency of the input signal so that the signal will pass undistorted through the AGC amplifier. The same considerations apply for this filter as applied for the input filter connected to the RAX and RAY pins. The roll-off frequency should be chosen as a compromise between the signal distortion and the AGC access time. The third and final gain stage is an open collector filter driver. The outputs of this stage should be pulled up to VDD1 with 340Ω. The AGC loop is closed when the output at FDX and FDY is capacitively coupled to the BX and BY inputs.

The nominal closed-loop output swing of the AGC loop is 3.5Vp-p differential. If the AGC amplifier is connected open loop, the minimum guaranteed output swing the amplifier output stage will tolerate is 6.5Vp-p differential when the filter connected to FDX and FDY is pulled-up to the 12 volt supply. This minimum value is implied by the 3-stage amplifier CMOV and output offset specifications and is required to ensure that the output signal does not distort due to clipping or saturation in the output stage. The nominal output swing of the AGC amplifier can be adjusted up or down by connecting an external resistor from the HTHX pin ground or the 5 volt supply, respectively. Care should be taken not to adjust the nominal AGC output swing too high, as the signal may become distorted if the maximum output swing is exceeded during an input magnitude transient. The value of the nominal AGC output swing must be weighed carefully against the expected transient nature of the incoming data. The only fundamental concern when adjusting the output swing lower is the inherent offsets present in the circuitry in the VM443. In general, as the nominal AGC output swing is lowered, the pulse pairing of the output signal will increase. This is because the differential AGC output signal now has as lower slope as it passes through 0 volts, making input offsets in the differentiator more visible. The equation to increase the nominal AGC output magnitude in terms of RHTHX is

$$V_{OUT} = \frac{2230000 + (2624 \cdot RHTHX)}{75000 + (750 \cdot RHTHX)} Vp - p$$

for RHTHX connected to ground. Where RHTHX is expressed in ohms, and RHTHX > 1kΩ. The equation to decrease the nominal AGC output magnitude in terms of RHTHX is

$$V_{OUT} = \{3.52 - [32420 / (RHTHX + 102)]\} Vp\text{-}p$$

for RHTHX connected to V_{CC2}. Where RHTHX is expressed in ohms, and RHTHX > 15kΩ. These equations are a good approximation if only small output magnitude adjustments are desired. As the size of the magnitude adjustment increases, the variation over temperature and the predictability on a part-to-part basis will become worse. For large magnitude adjustments, these equations are only accurate to ± 30% over temperature and part-to-part variations.

The AGC loop also contains a low-level threshold. The low-level threshold blocks low-magnitude signals such as noise from normal AGC action. This improves the circuit's ability to coast over long interpulse spans of no data, such as certain types of address marks. The low-level threshold is set to be 20% of the nominal AGC output magnitude. Like the nominal AGC output magnitude, the low-level threshold can be adjusted up or down by connecting a resistor from the LTHX pin to ground or the 5 volt supply, respectively. The limit on how high the low-level threshold can be adjusted is determined by the expected dynamic magnitude range of the input signal. If the input magnitude can change by 50% instantaneously, and this change still represents a stream of valid data pulses, then it should be adjusted safely below the 50% level. If the low-level threshold is adjusted too high, then the AGC loop could lose lock while reading data. The equation to increase the low-level threshold in terms of RLTHX is

$$V_{BLK} = \frac{3940000 + (463 \cdot RHTHX)}{75000 + (750 \cdot RHTHX)} Vp - p$$

for RLTHX connected to ground. Where RLTHX is expressed in ohms, and RLTHX > 300Ω. The equation to decrease the blocking threshold in terms of RLTHX is

$$V_{BLK} = \{0.62 - [7258 / (RLTHX + 100)]\} Vp\text{-}p$$

for RLHTX connected to VCC2. Where RLHTX is expressed in ohms, and RLHTX > 15kΩ. As with the AGC nominal output swing equations, these equations are a good approximation if only small magnitude adjustments are desired. As the size of the magnitude adjustment increases, the variation over temperature and the predictability on a part-to-part basis will become worse. For large magnitude adjustments these equations are only accurate to ± 30% over temperature and part-to-part variations.

The AGC action of the loop can be synchronously suspended for a short period of time with the TRK pin. The TRK pin is a TTL input that will turn off the charge pump at the end of a pump up/down cycle. When the TRK pin is high, normal AGC action occurs. If the TRK pin is forced low, the gain of the three-stage amplifier is held constant, allowing slow input magnitude variations through the amplifier without AGC action. The TRK pin can only be held low for short periods of time determined by the maximum specified AGC hold current, capacitor size connected to the GCV pin, and maximum tolerable gain excursion. For instance, if the GCV capacitor is 0.02μF, and the maximum allowable gain excursion is one unit, then the maximum time that the loop can be forced to track can be calculated. The typical three-stage amplifier gain to GCV voltage ratio is $28A_V$ /Volt. If the gain can only be allowed to change 1 unit, then the GCV pin voltage can only be allowed to droop or rise 1/280V or 3.57mV. The relationship which describes the transfer characteristics of the GCV pin voltage is simply $I = C(dV/dt)$ or rearranged $dt = (C/I)dV$. Substituting with the specification values for hold current and GCV capacitor

value, the track time can be calculated as follows:

$$dt = \frac{(0.02 \times 10^{-6})(3.57 \times 10^{-3})}{1 \times 10^{-6}} = 71 \times 10^{-6}\text{ s or } 71\mu s$$

if more gain variation can be tolerated, or a larger GCV capacitor is used, the allowable tracking time can be increased.

The AGC attack and release time can be adjusted two different ways. The magnitude of the capacitance connected to the GCV pin can be increased or decreased to adjust the response of the loop. If no other adjustments are made, this capacitance must be larger than 0.01μF to ensure loop stability. The second way to adjust loop response is by adjusting the gain of the charge pump by increasing or decreasing the pump up and pump down current. The gain of the charge pump can be decreased by connecting a resistor from the AGCR pin to ground and increased by connecting the same resistor to V_{CC2}. The equation to calculate the increase in attack current in terms of the resistor value connected to the AGCR pin is as follows:

$$I_{ATK} = [(4.3 / RAGCR) + 100 \times 10^{-6}] \text{ amperes}$$

for RAGCR expressed in ohms connected to VCC2 and RAGCR > 10kΩ. The effective release current is simply one-half the attack current or $I_{RLS} = I_{ATK}/2$. This is a result of the method chosen for the peak detection in the internal circuitry. The equation to calculate the decrease in attack current in terms of the resistor value connected to the AGCR pin is as follows:

$$I_{ATK} = \frac{RAGCR \cdot 100 \times 10^{-6}}{RAGCR + 1325} \text{ amperes}$$

for RAGCR expressed in ohms connected to ground and RAGCR > 200Ω. As before, the effective release current is one-half the attack current. These equations are a good approximation if only small AGC response changes are desired. As the size of the adjustment increases, the variation over temperature and the predictability on a part-to-part basis will become worse. For large AGC response adjustments, these equations are only accurate to ± 30% over temperature and part-to-part variations. After the effective attack and release currents have been determined, the attack and release times can be calculated in a similar manner as the allowable tracking time was calculated. Assume for example that the input is experiencing a step change in amplitude of 25mVp-p to 62.5mVp-p. Also assume that the GCV capacitor is still 0.02μF and that the three-stage amplifier gain to GCV pin voltage ratio is still 280A_V/Volt. The necessary gain at the lowest input level is 4Vp-p/25mVp-p or 160. The gain at the highest input level is 4Vp-p/62.5mVp-p or 64. The gain change to adjust the AGC loop during a step change in magnitude is 160 - 64 or 96 gain units. This change in gain will correspond to 96A_V / [280 A_V/V] or 342mV change on the GCV pin. Using the relationship i = C[dV/dt] and rearranging to calculate the attack time:

$$dt = (C/I)dV = [(0.02 \times 10^{-6}/100 \times 10^{-6}) \cdot 0.342] = 68.4\mu s$$

the release time will be twice the attack time as explained previously. An interesting point to note is that the attack and release times will be slower with lower input magnitudes because the GCV pin voltage must slew farther to adjust the gain of the three-stage amplifier. This feature is noted in the specification by giving typical values for the attack and release times with two different input steps. Both input steps have the same step ratio, but the amplitudes are approximately an order of magnitude different. See Figure 3 for a graphical depiction of attack and release times.

FAST AGC ACQUISITION

During preamplifier head changes or other periods of time where data is not being read from the disk, it may be desirable to dynamically reduce the impedance looking into the RAX and RAY pins. By reducing the input impedance, large transient inputs, which are generated by switching preamplifier channels with different output offset voltages, can be allowed to settle out faster, reducing the required AGC acquisition time for the disk drive. The VM443 contains a circuit called an impedance switch, which dynamically reduces the impedance looking into the RAX and RAY pins by a factor of 10. This allows unwanted transients to settle out ten times faster than during normal read mode operation. The impedance switch is controlled by the FAQ input. When the FAQ input is forced to a TTL high, the impedance switch is off, and the VM443 is in the read mode. When the FAQ input is forced to a TTL low, the impedance switch is on, and the VM443 is in the idle mode.

A faster way to lock the AGC loop other than relying on normal AGC action is by using the fast acquisition or FAQ circuitry provided on the VM443. A FAQ cycle is initiated when the FAQ pin is switched from a TTL high to a TTL low. The high-to-low transition triggers circuitry that rapidly pulls the GCV pin voltage to a high value. This forces the AGC amplifier to the lowest possible gain state so that regardless of the input magnitude very little signal is present on the FDX and FDY pins. While the FAQ pin is low, the AGC loop will stay locked in this state. On the FAQ pin low-to-high transition, the internal circuitry begins to ramp the GCV voltage at a rate much faster than normal AGC action. The first signal peak at the FDX and FDY pins that exceeds the high-level threshold switches the FAQ circuitry off and normal AGC action continues. The FAQ function along with the impedance switch can speed up the AGC acquisition time by a factor of 10.

PULSE VALIDATION OPERATION

The differentiator turns the peaks of the input signal into zero crossings so that logical operations can be performed on the data stream. The level-sense circuitry decides if the signal level has exceeded a fixed magnitude threshold. If the magnitude of the input signal is large enough, the level-sense circuitry enables the validation gate. The output of the differentiator is input to a comparator that turns the data stream into a series of logic transitions that exactly reproduce the timing relationship of the positive and negative peaks of the input signal. The output of the comparator is input to the pulse width and slope validation logic. The pulse width validation checks to make sure that the time between input signal pulses is at least some nominal value. If the pulse period is too short, as might be seen if high-frequency noise was contaminating the input signal, the pulse width validation block will not enable the validation gate. The slope validation block ensures that the slope of two successive peaks are the opposite polarity. If the oppo-

site slope condition is not met, the validation gate will not be enabled. When all three conditions for validation are met by enabling the validation gate, a TTL pulse is output of the RDD pin. The stream of TTL pulses on the RDD pin exactly reproduces the timing relationship of the validated input signal peaks.

PULSE VALIDATION ADJUSTMENT

The BX and BY pins are not only used to close the AGC feedback loop, but are also used as the input for the differentiator and level-sensing circuitry. By connecting a filter between the FDX, FDY pins and the BX, BY pins as shown in the typical applications diagram, the input to the differentiator can be bandwidth-limited to a specified frequency range. The filter shown in the typical applications diagram is a fourth order Butterworth filter with a 5MHz roll-off frequency. If no filtering is desired, the FDX and FDY pins should be terminated to VDD1 with 340Ω.

The impedance connected between the DIFFA and DIFFB pins sets the gain of the differentiator according to the following equation:

$$A_{VD} = 700 / Z_D$$

where Z_D is the impedance connected between the DIFFA and DIFFB pins. The roll-off frequency of the differentiator network should be chosen so that it is at least 1.7 decades above the highest frequency component of the input signal and the highest required harmonic of that frequency.

The maximum output swing for the differentiator is 6Vp-p differential. The gain of the differentiator must be low enough so that the worst-case magnitude change at the output of the AGC loop will pass through the differentiator without clipping or saturation. This implies that the differentiator gain should be less than or equal to 1.

The BX and BY pins are also used as the input for the level-sensing circuit. This circuit checks the output signal of the AGC loop for a minimum peak-to-peak magnitude. If this magnitude is not reached, the validation gate will not be enabled. The validation level is nominally set to be 1.675Vp-p or 50% of the nominal unadjusted AGC output magnitude. The validation level can be externally modified up or down by connecting a resistor from the LEVEL pin to ground or V_{CC2}, respectively. The equation for increasing the validation level in terms of the resistor value R_{LEVEL} is

$$V_{LEVEL} = \frac{1.675 \cdot R_{LEVEL} + 1536}{R_{LEVEL} + 114.2} Vp - p$$

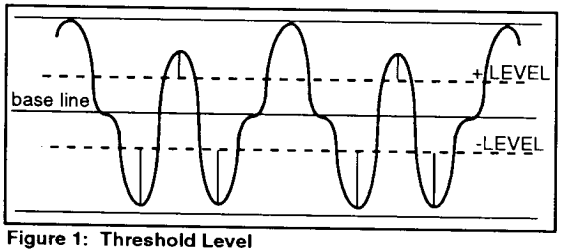


Figure 1: Threshold Level

for R_{LEVEL} expressed in ohms, connected to ground, and $R_{LEVEL} > 400\Omega$. The equation for decreasing the validation level in terms of the resistor value RLEVEL is

$$V_{LEVEL} = \frac{1.675 \cdot R_{LEVEL} - 20883.5}{R_{LEVEL} + 114.2} Vp - p$$

for R_{LEVEL} expressed in ohms, connected to V_{CC2} and $R_{LEVEL} > 25k\Omega$. These equations are a good approximation if small validation level changes are desired. As the size of the adjustment increases, the variation over temperature and the predictability on a part-to-part basis will become worse. For large validation level adjustments, these equations are only accurate to ± 30% over temperature and part-to-part variations. The validation level should not be set too high or valid data pulses might be lost. Conversely, if the validation level is set too low, low-level, low-frequency noise might be validated and output on the RDD pin.

The limiting case for the validation threshold is determined by a periodic input signal pattern consisting of three successive high-frequency transitions followed by a low-frequency transition as shown in Figure 1. Note that the second transition of the three successive high-frequency transitions does not rise above the baseline as high as the other two high-frequency transitions. This problem is primarily caused by pulse crowding and will be more pronounced for the inner tracks on the disk where the flux density is highest. In addition to this loss, a certain amount of amplitude margin must be allotted for media defects, crosstalk, and noise.

The output of the differentiator is input to a comparator where it is differentially compared and transitions are formed where the input signal peaks occurred. Offset in the comparator and differentiator can cause an effect called pulse pairing loss. The pulse pairing effect is created when the comparator or differentiator does not switch exactly when the input signals cross, but at some nominal offset voltage from the crossing point. This offset creates a skew in time for every other pulse of the output data stream. This error directly detracts from the system performance by consuming a portion of the bit cell window.

The primary source of pulse pairing error (or bit shift error) in the VM443 is due to offset in the comparator. For a sinusoidal input this offset causes a non-symmetric output as shown in Figure 2a. This asymmetry produces a bit shift at the RDD output between the pulses from the positive and negative portions of the sine wave.

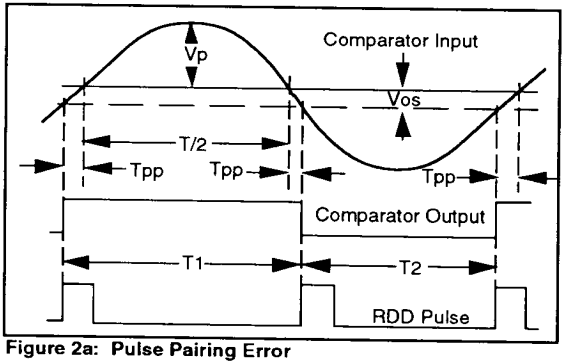


Figure 2a: Pulse Pairing Error

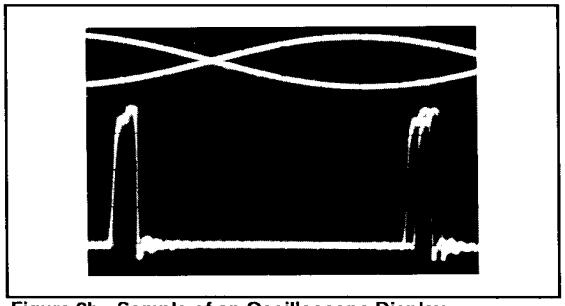


Figure 2b: Sample of an Oscilloscope Display

The pulse pairing error can be observed by inputting a constant frequency signal into the BX and BY pins and viewing the RDD pin output on an oscilloscope. Trigger the oscilloscope on successive leading edges by adjusting the trigger level and trigger hold-off. The second pulse after the trigger point will display two times the pulse pairing error since each of these pulses is shifted by the same amount only in opposite directions from their ideal position. A sample oscilloscope display is shown in Figure 2b.

Analytically, the contribution to pulse pairing error by comparator offset can be determined from Figure 2a. The shift of the comparator output relative to the sine wave zero crossing is given by Tpp in equation (1). The pulse pairing error PP can then be defined in terms of Tpp as in equation (2).

1. $Tpp = 1/(2\pi f) \arcsin (V_{OS}/Vp)$
2. $PP = (T1-T2)/2 = 2Tpp$
3. $PP = 1/(\pi f) \arcsin (V_{OS}/Vp)$

Combining equations (1) and (2) into (3) gives an expression for pulse pairing error (or most of it) in terms of signal frequency, signal amplitude V_p, and comparator offset V_{OS}.

The output of the comparator is coupled to the validation logic which performs the pulse width and slope validation. If the validation level has been exceeded, and the slope of the current data pulse is the opposite polarity of the previous pulse, then the pulse width validation begins by triggering the timing ramp block so it begins to ramp down. If the comparator changes state while the timing ramp is taking place, the timing ramp block is reset and no pulse is output from the RDD pin. If the comparator output pulse meets the minimum pulse duration criteria set by the timing capacitor CDVC and the internal current source, the timing ramp block will output a pulse to the TTL output buffer which has a pulse width equal to the time it takes the timing ramp block to recover to a state where it is ready to accept data. The pulse width validation time is therefore not only set by the ramp time but also by the output pulse width duration or timing ramp recovery time. Refer to Figure 4 for a functional logic diagram.

A typical value for the ramp and recovery time for a fixed capacitor value is given in the electrical characteristics section. The ramp and recovery thresholds as well as the current source value is fixed in the internal circuitry. To adjust the ramp time to twice the nominal value listed, simply double the CDVC capacitor value. Likewise, to reduce the ramp and recovery time by half, reduce the capacitor value by half.

The limitation to the length of the timing ramp and recovery time is the period of the highest frequency pattern of the input data stream. The pulse width validation time must be chosen to be less than this value. For example, assume the case of a system using (2,7) RLL code at a 10MBPS transfer rate. For this code, the nominal spacing between the highest frequency data transitions is 150ns. Allowing a margin of 35ns for worst-case data and noting that the ramp time is three times the recovery time, the capacitor CDVC should be chosen so that the ramp time is 86ns and the recovery time is 29ns. This would be a capacitor value of approximately 22pF.

Summarizing, three criteria must be met to generate a valid data pulse:

1. The pulse must have some minimum amplitude
2. The pulse must have some minimum width
3. The pulse must have alternating polarities.

The pulse amplitude and pulse width validation circuits can both be controlled externally to optimize the performance of the read data processor. With this flexibility, the response of the VM443 can be tailored so that the best possible operation is achieved, regardless of the wave shape of the input signal.

PIN DESCRIPTIONS

Pin Inputs:

RAX, RAY: Capacitively-coupled analog differential input from read/write preamp such as a VM117 or equivalent.

BX, BY: Input to differentiator and level-sense circuitry of validation channel. Capacitively coupled to the FDX and FDY outputs.

DIFFA, DIFFB: Gain setting pins for the differentiator. Connection points for CDIFF and RDIFF.

A, B: Gain setting points for the AGC loop. Connection points for RAB and CAB.

TRK: The track/hold input control pin. A TTL high enables the AGC loop. A TTL low temporarily disables the AGC loop.

HTHX: Adjustment pin for AGC loop nominal output magnitude. Connection point for RHTHX.

LTHX: Adjustment pin for AGC loop low-level threshold. Connection point for RLTHX.

AGCR: Adjustment pin for AGC attack and release time. Connection point for RAGCR.

FAQ: The FAQ or fast acquisition control pin. A low-to-high transition initiates the FAQ action by forcing the AGC gain very low. The low-to-high transition starts the fast AGC acquire.

LEVEL: Adjustment pin for the validation level. Connection point for the RLEVEL resistor.

DVC1, DVC2: Connection pins for CDVC capacitor to adjust the blockout time for pulse validation.

Pin Outputs:

RDD: Read data pulse output pin. TTL compatible.

FDX, FDY: Output of AGC loop. Capacitively coupled to BX and BY during closed loop operation.

GCV: AGC loop filter node. Connection point for CAGC the capacitor.

TDA, TDB: Test point for the differentiator. An open emitter level-shifted version of the differentiator output.

Pin Supplies:

VDD1: Positive 12 volt supply.

VDD2: On-chip voltage regulator output. Compensated with 0.01 µF capacitor to ground.

VCC1: Positive 5 volt supply for analog circuitry.

VCC2: Positive 5 volt supply for digital circuitry.

VEE1: Analog ground.

VEE2: Digital ground.

DC CHARACTERISTICS Unless otherwise specified, V_{DD1} = 12V ±10%, $V_{CC1} = V_{CC2}$ = 5V ±10%, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
POWER SUPPLY						
Supply Current	I_{DD1}		10	30	55	mA
	I_{CC1}		1.5	2.9	5.5	
	I_{CC2}	Measured with FAQ held to TTL high	10	21	45	
	I_{CC2}	Measured with FAQ held to TTL low	45	84	115	
Power Dissipation	P_D	Measured with FAQ held to TTL high		720	1150	mW
Regulator Voltage	V_{REG}		9.2	9.6	10.3	V
LOGIC SIGNALS						
Input High Voltage	V_{IH}	Tested at V_{CC2} = 4.75V; I_{IN} = -12mA				V
Input Low Voltage	V_{IL}				0.8	
Input Clamp Voltage	V_{IC}			-0.65	-1.5	
Input High Current	I_{IH}	Tested with V_{CC2} = 5.25V, V_{IN} = 2.0V; For TRK input		10	20	µA
		For FAQ input. FAQ input counts as 2 TTL loads		20	40	µA
Input Low Current	I_{IL}	Tested with V_{CC2} = 5.25V, V_{IN} = 0.4V; For TRK input		-0.3	-0.5	mA
		For FAQ input. FAQ input counts as 2 TTL loads		-0.6	-1.0	
Output Low Voltage	V_{OL}	Tested on R_{DD} output with I_{OUT} = 8 mA, V_{CC2} = 4.75V		0.35	0.5	V
Output High Voltage	V_{OH}	Tested on R_{DD} output with I_{OUT} = -400µA, V_{CC2} = 4.75V	2.7	3.4		V

READ CHARACTERISTICS Unless otherwise specified, AGC loop feedback is broken, R_{AB} = 1.5kΩ, C_{AB} = 0.01µF, FDX and FDY are terminated to V_{DD1} with 340Ω, FAQ pin is forced to a TTL high, and input signal frequency is 2.5MHz, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	Tested with GCV pin forced to 2.725V, V_{IN} = 12.5mVp-p	150	290	400	V/V
		Tested with GCV pin forced to 4.725V, V_{IN} = 250mVp-p	1.0	2.6	8.0	
Amp Bandwidth	BW	Tested with GCV pin forced to 2.725V, V_{IN} = 12.5mVp-p	20	25		MHz
		Tested with GCV pin forced to 4.725V, V_{IN} = 250mVp-p	20	25		
Differential Resistance	R_{IN}	Tested with the FAQ pin forced to a TTL low, T_A = 27°C	140	220	300	Ω
		Tested with the FAQ pin forced to a TTL high, T_A = 27°C	1400	2200	3000	
		Tested with the FAQ pin forced to a TTL low, $0 \le T_A \le 70°C$	130	242	330	
		Tested with the FAQ pin forced to a TTL high, $0 \le T_A \le 70°C$	1300	2420	3300	
Input Capacitance	C_{IN}				10	pF
Noise Voltage	e_{IN}	Tested with the GCV pin forced to 2.725V		3	10	$nV/\sqrt{Hz}$
Output Swing	V_{OP}		5.5	7		Vp-p
CMOV	V_{CM}		V_{DD1} -3.9	V_{DD1} -3.0	V_{DD1} -2.1	V
Output Offset	V_{OFF}		-1		+1	V
CMRR	CMRR	Tested with V_{CM} = 100mVp-p, F = 5MHz, with GCV pin forced to 2.73V	40	60		dB
PSRR	PSRR	Tested with V_{CM} = 100mVp-p, F = 5MHz, with GCV pin forced to 2.73V for either V_{DD1}, V_{CC2}, or V_{CC1}	40	55		dB

DIFFERENTIATOR Unless otherwise specified, C_{DIFF} = 3pF, R_{DIFF} = 150Ω, f_{VIN} = 5MHz, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differentiator Gain	A_V		0.6	0.8	1.3	V/V
Differentiator Bandwidth	B_W	Tested with R3 = 1kΩ, C3 = 0.1µF	50	90		MHz
Input Resistance	R_{IN}	Tested at F = 5MHz	3000	5000		Ω
Input Capacitance	C_{IN}				20	pF

AGC LOOP Unless otherwise specified, Cx = Cy = 0.1µF, R_{AB} = 1.5kΩ, C_{AB} = 0.01µF, C_{GVC} = 0.02µF, T_A = 25°C.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Input Range	V_{IR}		25		300	mVp-p
Output Swing	V_{OUT}		3.0	3.5	4.0	Vp-p
FAQ Response	T_{FAQ}	Tested from 50% of FAQ (low to high) to 90% of FDX, FDY envelope with FAQ pulsewidth = 6ns. Tested with 25mVp-p input		20	40	µs
FAQ Pulsewidth	T_{PW}		20			ns
Input Signal Ratio	B/A			20		%
Attack Time	T_{ATK}	Tested with A = 100mV, B = 250mV		20		µs
		Tested with A = 25mV, B = 62.5mV		75		
Release Time	T_{RL}	Tested with A = 100mV, B = 250mV		40		µs
		Tested with A = 25mV, B = 62.5mV		150		
DC Attack Current	I_{ATK}		50	80	110	µA
DC Release Current	I_{RL}		50	80	110	µA
AC Attack Current	I_{ATK}		75	100	125	µA
AC Release Current	I_{RL}		35	50	65	µA
Hold Current	I_H			0.1	1	µA
AGC Transfer Ratio	R_{AGC}			280		Av/V
Validation Level	V_{LV}			±830		mV
Validation Timeout	V_{TO}	Tested with 25pF connected from the DVC1 pin to the DVC2 pin		100		ns
RDD Pulsewidth	R_{PW}			35		ns
Pulse Pairing	P_P				2.5	ns

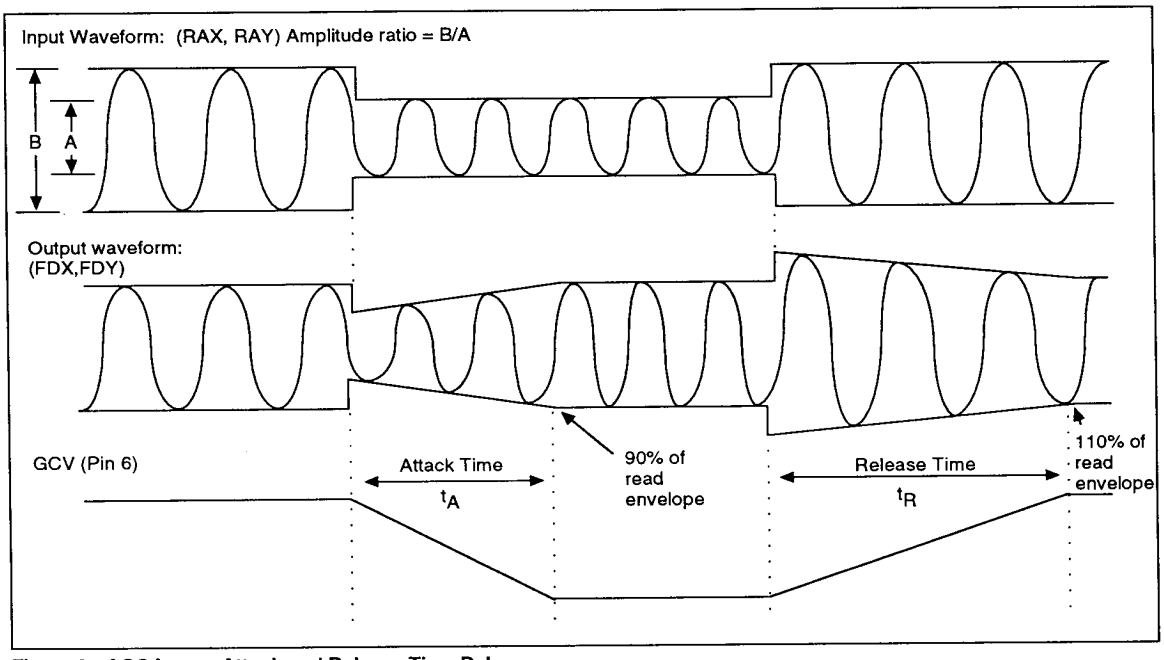


Figure 3: AGC Loop - Attack and Release Time Delays

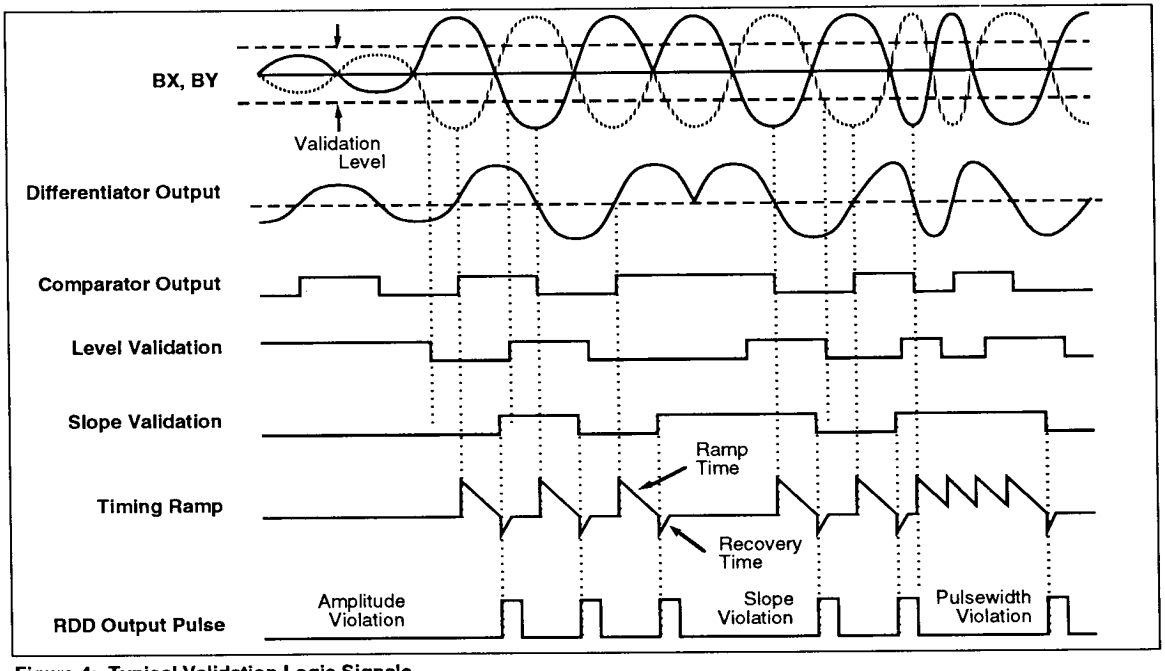


Figure 4: Typical Validation Logic Signals