NEC

MOS INTEGRATED CIRCUIT

μPD23C32082L

32M-BIT MASK PROGRAMMABLE ROM
2M-WORD BY 16-BIT (WORD MODE) / 1M-WORD BY 32-BIT (DOUBLE WORD MODE)
PAGE ACCESS MODE

Description

The μPD23C32082L is a 33,554,432 bits mask-programmable ROM. The word organization is selectable (WORD mode : 2,097,152 words by 16 bits, DOUBLE WORD mode : 1,048,576 words by 32 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C32082L are packed in 70-pin plastic SSOP.

Features

- Word organization

  2,097,152 words by 16 bits (WORD mode)

  1,048,576 words by 32 bits (DOUBLE WORD mode)

- Page access mode

  DOUBLE WORD mode : 8 double words random page access

  WORD mode : 16 words random page access

- Operating supply voltage : 3.3 V ± 0.3 V

	Operating supply voltage V_{CC}	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
★	3.3 V ± 0.3 V	100 / 30	80	30

★ Ordering Information

Part number	Package
μPD23C32082LG7-xxx	70-pin Plastic SSOP (500 mil)

(xxx : ROM code suffix No.)

The information in this document is subject to change without notice.

Document No. M12267EJ4V0DS00 (4th edition)
Date Published February 1998 NS CP (K)
Printed in Japan

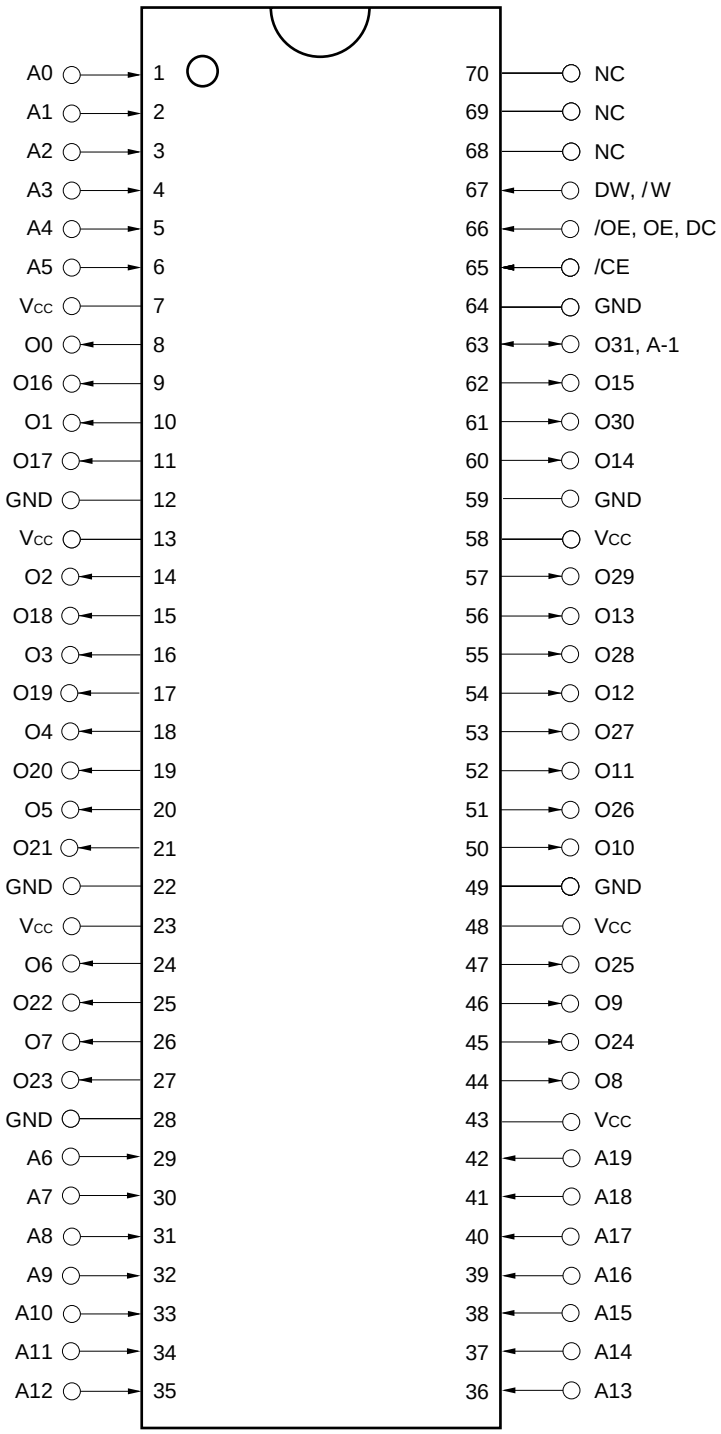
The mark ★ shows major revised points.

★ Pin Configuration (Marking Side)

/XXX indicates active low signal.

70-pin Plastic SSOP (500 mil)

[μPD23C32082LG7]



Pin Name

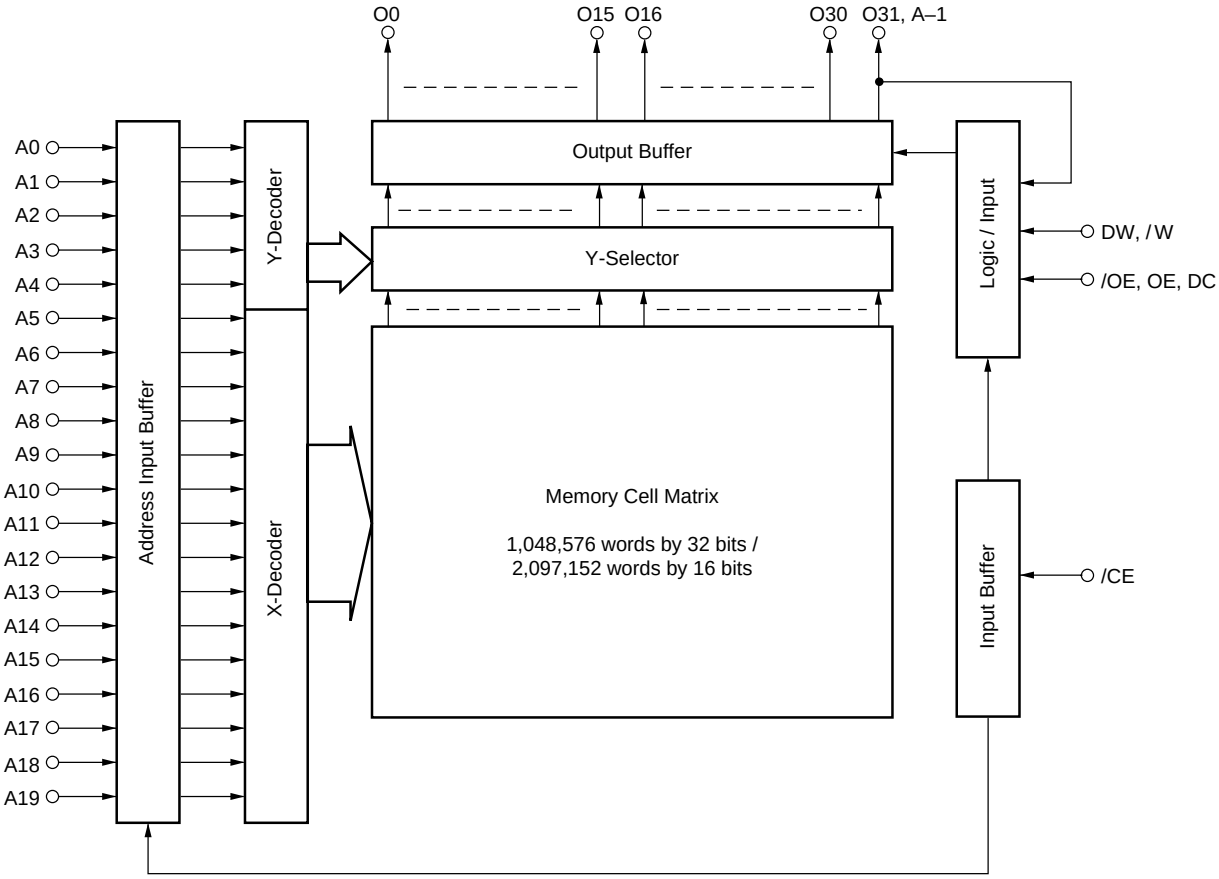
A0 - A19	:	Address Inputs
O0 - O15, O16 - O30	:	Data Outputs
O31, A–1	:	Data 31 Output (DOUBLE WORD mode), LSB Address Input (WORD mode)
DW, /W	:	Mode Select
/CE	:	Chip Enable
/OE, OE	:	Output Enable
V_{CC}	:	Supply Voltage
GND	:	Ground
NC [Note]	:	No Connection
DC	:	Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Input / Output Pin Functions

Pin name	Input / Output	Function
DW, /W	Input	The pin for switching DOUBLE WORD mode and WORD mode. **High level** : DOUBLE WORD mode (1M words by 32 bits) **Low level** : WORD mode (2M words by 16 bits)
A0 to A19 (Address inputs)	Output	Address bus. A0 to A19 are used differently in the DOUBLE WORD mode and the WORD mode. **DOUBLE WORD mode (1M words by 32 bits)** A0 to A19 are used as 20 bits address signals. **WORD mode (2M words by 16 bits)** A0 to A19 are used as the upper 20 bits of total 21 bits of address signal. (The least significant bit (A–1) is combined to O31.)
O0 to O15, O16 to O30 (Data output)	Output	Output data bus. O0 to O15, O16 to O30 are used differently in the DOUBLE WORD mode and the WORD mode. **DOUBLE WORD mode (1M words by 32 bits)** The lower 31 bits of 32 bits data outputs to O0 to O30. (The most significant bit (O31) combined to A–1.) **WORD mode (2M words by 16 bits)** 16 bits data outputs to O0 to O15 and also O16 to O30 is high impedance.
O31, A–1 (Data output 31, LSB address input)	Input, Output	O31, A–1 are used differently in the DOUBLE WORD mode and the WORD mode. **DOUBLE WORD mode (1M words by 32 bits)** The most significant output data bus (O31). **WORD mode (2M words by 16 bits)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High impedance **Low level** : Data out
/OE, OE, DC (Output Enable)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}		Supply voltage
GND		Ground
NC		Not internally connected (the signal can be connected).

Block Diagram



Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among “0”, “1”, “×” shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
×	DC	Don’t care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

/CE	/OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : ×)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L : Low level input

H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC} + 0.3	V
Output voltage	V_O		–0.3 to V_{CC} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
High level output voltage	V_{OH}	I_{OH} = –400 μA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}	–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected	–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode), I_O = 0 mA			80	mA
Standby current	I_{CC2}	/CE = V_{IH} (Standby mode)			1.5	mA
	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)			30	μA

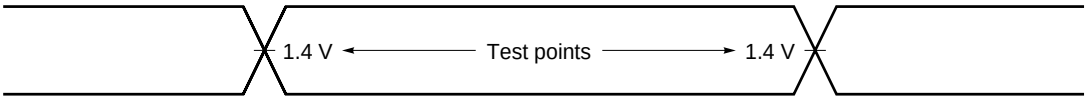
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 3.3 V ± 0.3 V)

	Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
★	Address access time	t_{ACC}				100	ns
★	Page access time	t_{PAC}				30	ns
★	Chip enable access time	t_{CE}				100	ns
★	Output enable access time	t_{OE}				30	ns
	Output hold time	t_{OH}		0			ns
	Output disable time	t_{DF}		0		25	ns
	DOUBLE WORD, WORD access time	t_{CBW}				100	ns

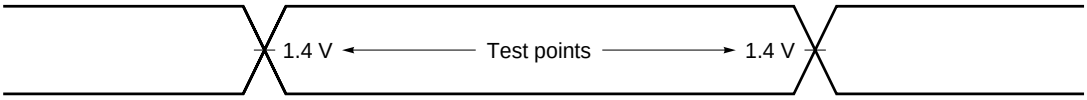
Remark t_{DF} is the time from inactivation of /CE or /OE, OE to high-impedance state output.

AC Test Conditions

Input Waveform (Rise / Fall Time ≤ 5 ns)



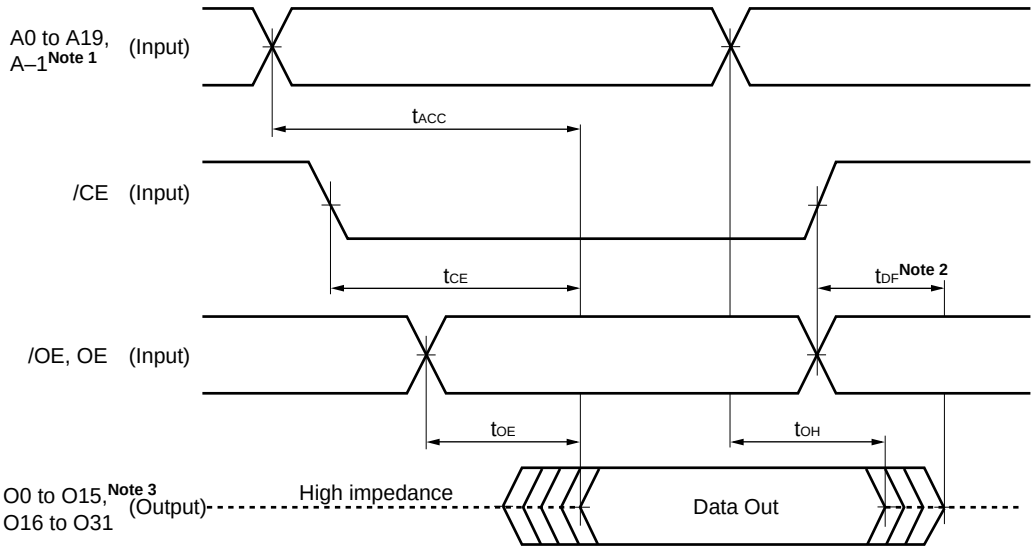
Output Waveform



Output Load

1 TTL + 100 pF

Read Cycle Timing Chart 1

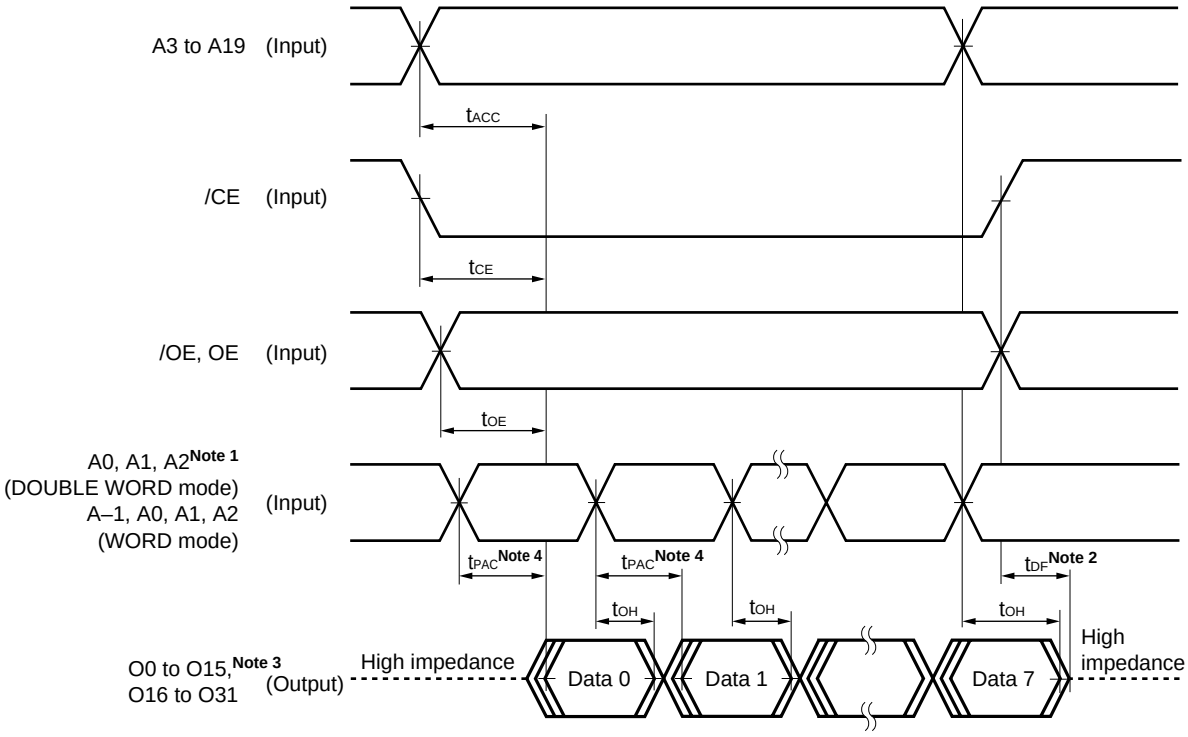


Notes 1. During DOUBLE WORD mode, A–1 is O31.

2. t_{DF} is specified when one of /CE, /OE, OE is inactivated.

3. During WORD mode, O16 to O30 are high impedance and O31 is A–1.

Read Cycle Timing Chart 2 (Page Access Mode)



Notes 1. During DOUBLE WORD mode, A–1 is O31.

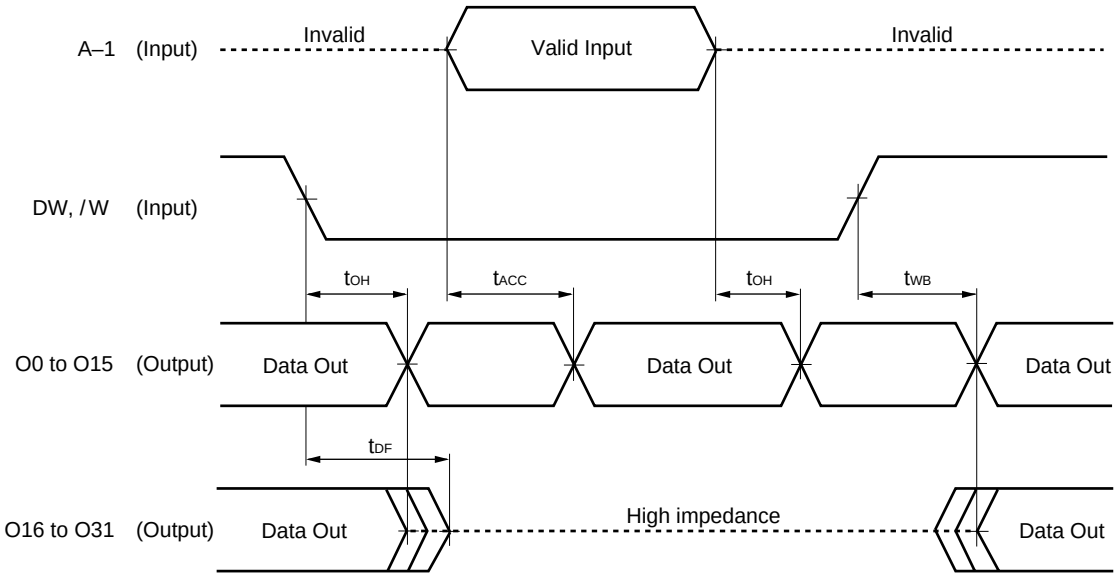
2. t_{DF} is specified when one of /CE, /OE, OE is inactivated.

3. During WORD mode, O16 to O30 are high impedance and O31 is A–1.

4. The definitions of page access time is as follows.

Page access time	Upper address (A3 to A19) inputs condition	/CE input condition	/OE, OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A–1, A0, A1, A2)

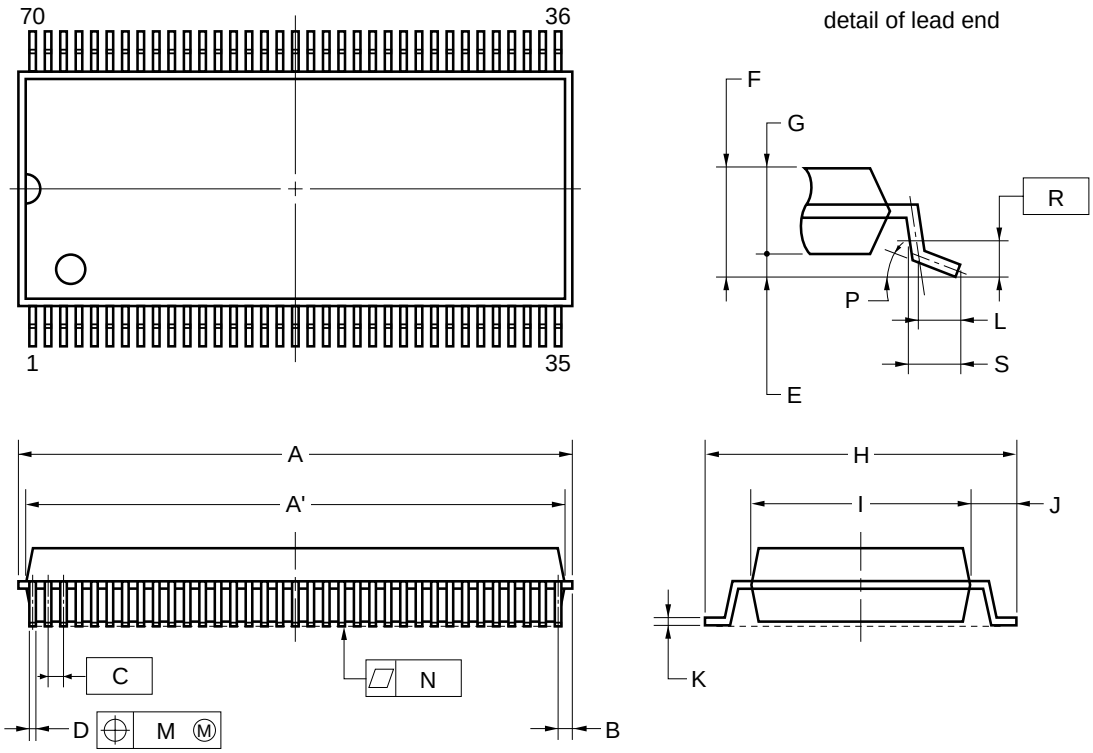
DOUBLE WORD Mode, /WORD Mode Switching Timing Chart



Remark /OE, OE and /CE : Active

★ **Package Drawing**

70 PIN PLASTIC SHRINK SOP (500 mil)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material conditions.

ITEM	MILLIMETERS	INCHES
A	28.87 MAX.	1.137
A'	28.57±0.1	$1.125^{+0.004}_{-0.005}$
B	0.89 MAX.	0.035
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.32^{+0.08}_{-0.07}$	$0.013^{+0.003}_{-0.004}$
E	0.1±0.05	0.004±0.002
F	3.0 MAX.	0.119 MAX.
G	2.7±0.15	$0.106^{+0.007}_{-0.006}$
H	15.9±0.3	0.626±0.012
I	12.7±0.1	0.500±0.004
J	1.6±0.2	0.063±0.008
K	$0.22^{+0.025}_{-0.015}$	0.009±0.001
L	0.8	0.031
M	0.10	0.004
N	0.10	0.004
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25	0.010
S	0.88±0.15	$0.035^{+0.006}_{-0.007}$

P70G7-80-500A

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C32082L.

★ **Types of Surface Mount Device**

μPD23C32082LG7 : 70-pin plastic SSOP (500 mil)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed imme-diately after power-on for devices having reset function.

[MEMO]

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