1. OUTLINE

The LI3010EC is an evaluator designed for use with the C-MOS 1 chip microcomputer SM-4. With a PROM externally added, it becomes equivalent in function to the SM-4. In addition, having a hold function, 1 step function and indication function of accumulator and RAM address contents, it is valid to debug programs for the SM-4.

< Features >

CMOS Process
ROM Capacity : Addressing possible up to 2268 bytes
RAM Capacity : 96 words
Instruction Set : 54 instructions
Subroutine Level : 1 level
Hold Function
1 Step Function
Auto Stop Function
Accumulator Contents Indication
RAM Address Contents Indication
108 Pin Quad Package (Ceramic)
Built-in 5V to 3V Level Shifter (I_1 to I_8, Ⓐ Ⓑ Ⓒ Sync.)

2. CONFIGURATION

Refer to Fig.1 on the following page.

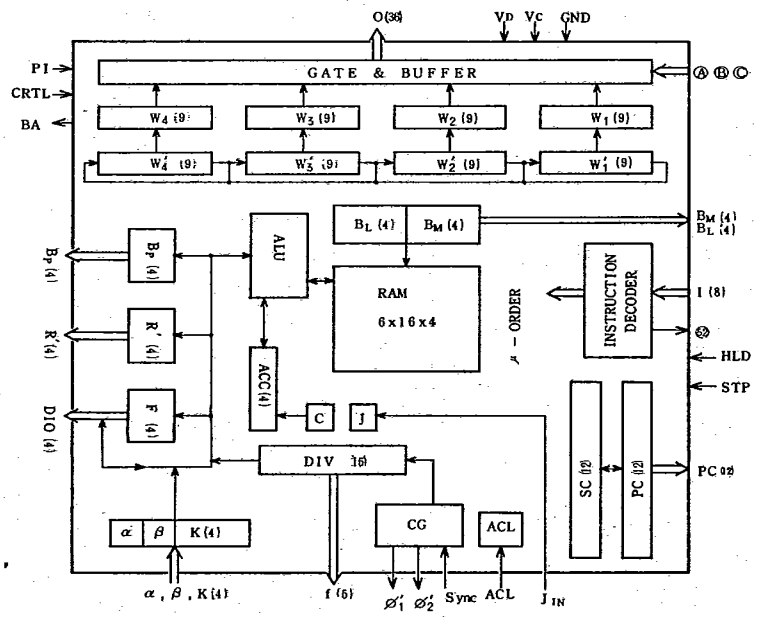


FIG.1 EVALUATION CHIP CONFIGURATION

3. TERMINAL DESCRIPTION

Described here are terminals except those in use on the SM-4.

Terminal Name	I/O	Description
I_1 to I_8	I	Instruction code input terminal
$PL_{1\sim6}$	O	Output terminals for the contents of program counters $PL_{1\sim6}$
$PU_{1\sim4}$	O	Output terminals for the contents of program counters $PL_{1\sim4}$
C_A	O	Output terminal for the contents of program counter C_A
C_X	O	Output terminal for the contents of program counter C_X
HLD	I	With HLD terminal set to "1", the CPU is turned to HOLD mode, and the PC and F/F hold their contents. With HLD terminal set to "0", the CPU is turned to RUN mode to continue the execution of the stopped program.
STP	I	With "1" transferred to STP terminal in HOLD mode, the CPU starts to execute only 1 step of instruction with the PC counting up 1, and stops.
$B_{L_{1\sim4}}$	O	Output terminals for the contents of RAM address registers $B_{L_{1\sim4}}$.
$B_{M_{1\sim4}}$	O	Output terminals for the contents of RAM address registers $B_{M_{1\sim4}}$.
J	O	With a skip executed by a conditional skip instruction, the J output is "1" during the cycle.
J_{IN}	I	Skip conditions a and b for RAM address register BL, one of the PLAs for the SM-4, can optionally be set by an external circuit. "1" must be transferred to the J_{IN} terminal when the skip conditions are matched.
CTRL	I	Control terminal for the clock stop circuit, one of the PALs for the SM-4. With CTRL terminal set to "1", the system clock stops by CEND instruction. The system clock starts at 0 page 0 step by a 1S signal or $K_{1\sim4}$ signal. (Pull up resistor provided).
PI	I	Input control terminal for R'F/F, one of the PLAs for the SM-4. With the PI set to "1", the R F/F is reset when the β input is "1".
V_C	I	The 5V power suppling port. $I_{1\sim8}$, Ⓐ Ⓑ Ⓒ sync, STP and HLD inputs are at 5V level. In this case, the level is shifted to 3V inside the LSI.
R'_1 to R'_4	O	R' F/F outputs and input signals to the PLA for R output.

Terminal Name	I/O	Description
B_{P_1} to B_{P_4}	O	B_P F/F outputs and input signals to the PLA for back plate signals H_1 to H_3 and O output switching signals Ⓐ Ⓑ and Ⓒ.
f_1, f_4, f_7, f_8, f_{13}	O	Divider output signals and input signals to the PLA. f_1=1Hz, f_4=8Hz, f_7=64Hz, f_8=128Hz, and f_{13}=4096Hz.
OS_3, OS_4	O	W register output signals and input signals to the PLA for R output.
㊿②	O	Micro order from READ and WRITE instructions, and input signal to the PLA.
T	O	Test F/F T output, and is "1" in TEST mode. Input signal to the PLA.
ϕ_1', ϕ_2'	O	Clock outputs. ϕ_1' is an input signal to the PLA for R output.
Ⓐ Ⓑ Ⓒ	I	O output switching signals, which transfer an output signal from the PLA.

4. FUNCTION DESCRIPTION

Hold Function

With HLD terminal set to "1", the CPU is turned to HOLD mode after the instruction execution has terminated to hold the contents of the program counter and each F/F, and then stops. With HLD terminal set to "0", the CPU releases HOLD mode to execute the program. PC outputs ($P_{L_{1\sim6}}$, $P_{U_{1\sim4}}$, CA and CX) indicate the addresses of the program to be executed next.

4-1. STEP MOTION FUNCTION

When "1" is transferred to the STP input to HOLD mode (with HLD terminal set to "1"), the CPU starts to execute only 1 step of instruction with the PC counting up 1, and then enters HOLD mode. (The signal to be transferred to the STP input requires to be free of keying chatter.)

Note 1: 2 step instructions (LBL, DTA, TAL, CEND and ST) are accesssed to HOLD mode after they have terminated.

Note 2: SBM, LAX, SSR and RTN1 instructions are accessed to HOLD mode after they have executed their next instruction.

Note 3: Instructions with skip conditions (INCB, DECB, ADD11, EXCI, EXCD, ADX, TA, TB, TC, TAM, TM, TAO, TABL, TIS and TAL are accessed to HOLD mode after they have skipped their next instruction when the skip conditions are matched. The J output at this time is "1".

4-2. ACCUMULATOR OUTPUT FUNCTION

In HOLD mode, the accumulators $A_{1\sim4}$ contents are transferred to the input/output terminals $DIO_{1\sim4}$.

4-3. RAM ADDRESS REGISTER CONTENTS INDICATION FUNCTION

RAM address registers $B_{L_{1\sim4}}$ and $B_{M_{1\sim4}}$ of the SM-4 are transferred, making it possible to indicate their contents.

4-4. AUTO STOP FUNCTION

With addition of an appropriate external circuit, the LI3010EC can be turned to HOLD mode at any optional address.

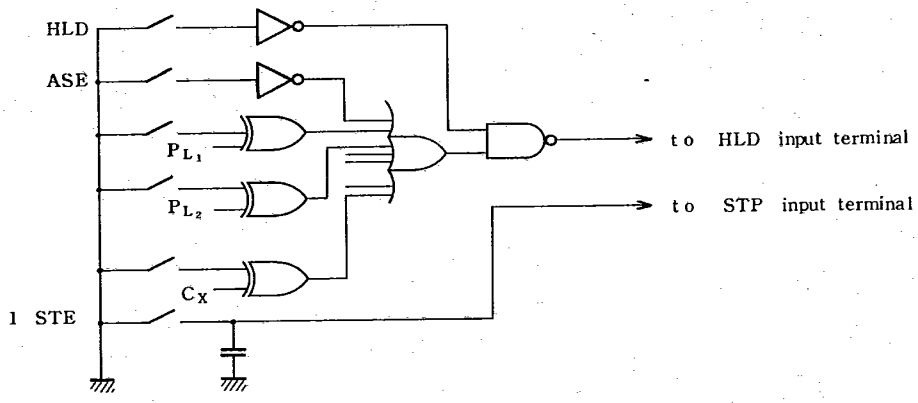


FIG.2 HOLD, AUTO STOP, ONE STEP CONTROL CIRCUIT

5. PLAs

The SM-4 has a number of PLAs which can be mask-altered. In the LI3010EC, however, these PLAs can be controlled by an external circuit and PLA control terminals (PT and CTRL).

5-1. RAM SKIP CONDITION SETTING PLA (PLA 1)

Skip conditions can be set by BL = a (2) under the INCB and EXCI instructions and B_L = b under the DECB and EXCD instructions. However, these conditions are determined by a $B_{L_{1\sim4}}$ and instruction I_4 combination. For example, when skipping is done at a = 7 and 15, and b = 0,

$\overline{I_4}\ (\overline{B_{L_4}}\ B_{L_3}\ B_{L_2}\ B_{L_1} + B_{L_1}\ B_{L_2}\ B_{L_3}\ B_{L_4}) + I_4\ \overline{B_{L_4}}\ \overline{B_{L_3}}\ \overline{B_{L_2}}\ \overline{B_{L_1}}$ must be transferred to input terminal J_{IN}.

5-2. RESETTING BY β SIGNAL OF R_1 F/F (PLA 2)

In the SM-4, R_1 F/F can be reset by the PLA when the β input signal is "1". In the LI3010EC, however, the R_1 F/F can be controlled by the PI terminal. (The PI is provided with a pull up resistor.)

5-3. SYSTEM CLOCK STOP CONTROL PLA (PLA 3)

In the SM-4, the system clock can be stopped by the CEND instruction, using the

PLA. At this time, part of input/output F/F and internal RAM contents are in storage. In the LI3010EC, this condition can be set by CTRL terminal. (The CTRL is provided with a pull up resistor.)

5-4. Ri OUTPUT (PLA 4)

$R_{1\sim4}$ outputs can be obtained by combining $R_{1\sim4}$ F/F outputs and O_{S_4}, O_{S_3}, fi, ϕ_1, I_1 and ⑤② outputs. The LI3010EC requires these logics to be externally lined up.

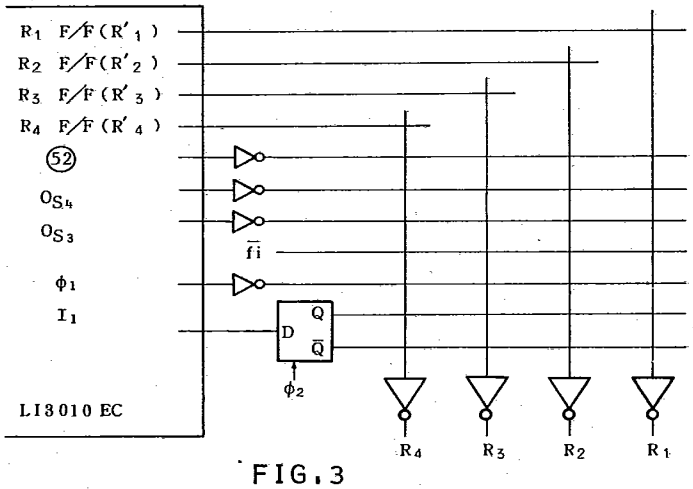


FIG.3

Note:
PC is transferred to synchronize ϕ_1. This cause the outputs I_1 to I_8 from the PROM to synchronize ϕ_1. When the logics are lined up as shown in Fig.3, they are required to synchronize ϕ_2.

5-5. $H_{1\sim2}$ OUTPUTS (PLA 5)

$H_{1\sim3}$ output and O ij output control signals Ⓐ, Ⓑ and Ⓒ are obtained by the combination of $B_{P_{1\sim4}}$, f_7, f_8, ⑤② and T. The LI3010EC requires these to be externally lined up.

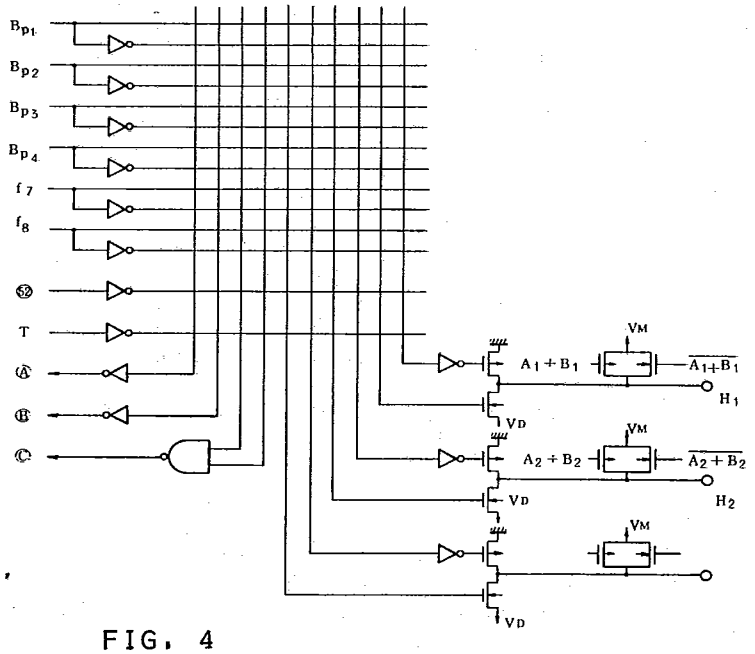


FIG. 4

6. SYSTEM CONFIGURATION

Fig.5 indicates a minimum system configuration required for the LI3010EC when used as evaluator of the SM-4.

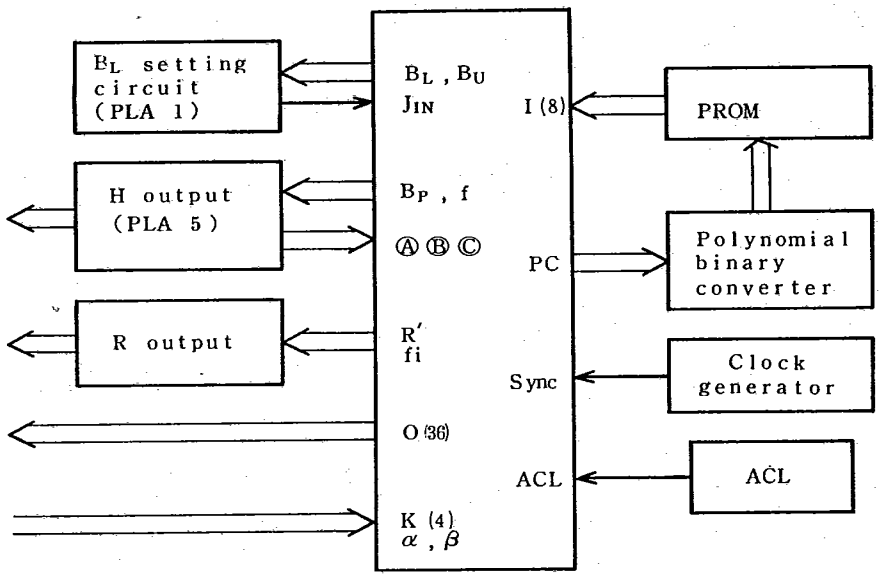


FIG.5

7. ELECTRICAL SPECIFICATIONS AND PACKAGE SPECIFICATIONS

≪ Absolute Maximum Rate ≫

Item	Symbol	Rate	Unit
Terminal voltage *	V_D	+0.3 to -3.5	V
	V_D	+0.3 to -5.5	V
	V_{IN_1}**	+0.3 to V_D-0.3	V
	V_{IN_2}***	+0.3 to V_C-0.3	V
Operation temperature	T opr	0 to +40	°C
Storage temperature	T stg.	-20 to +70	°C

* Maximum voltage applicable to the ground terminal.

** Applicable terminals: DIO(4), K(4), α,β, ACL, CTRL and PI

*** Applicable terminals: Ⓐ Ⓑ Ⓒ, J_{IN}, I(8), HLD, STP and Sync.

≪ Electrical Character ≫ V_D = -3V±5%, V_C=-5V±5%, Ta=25°C

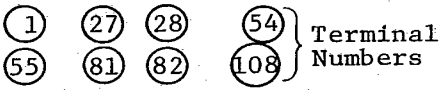
Item	Symbol	Condition	Rate MIN	Rate TYP	Rate MAX	Unit	Note
Input-Voltage	V_{IH1}		-0.6			V	1
	V_{IL1}				V_D+0.6	V	
	V_{IH2}		-0.3				2
	V_{IL2}				V_D+0.3	V	
	V_{IH3}		-0.6				3
	V_{IL3}				V_C+0.6	V	
Output-Voltage	V_{OH1}	I_O=50μA to V_D	-0.5			V	4
	V_{OL1}	I_O= 5μA to GND			V_D+0.5	V	
	V_{OH2}	I_O=50μA to V_D	-0.5			V	5
	V_{OL2}	I_O=30μA to GND			V_D+0.5	V	
	V_{OH3}	I_O=100μA to V_C	-0.6			V	6
	V_{OL3}	R_L=50KΩ to V_C			V_C+0.6	V	

Notes:
1. Applicable terminals: K(4), α,β, PI, CTRL
2. Applicable terminal : ACL
3. Applicable terminals: Ⓐ Ⓑ Ⓒ, J_{IN}, I(8), HLD, STP, Sync.
4. Applicable terminal: O(32)
5. Applicable terminal: DIO(4)
6. Applicable terminals: P_L(6), P_U(4), C_A, C_X, (52), R'(4), B_P(4), f(5), φ'(2)
   All terminals are open drain.

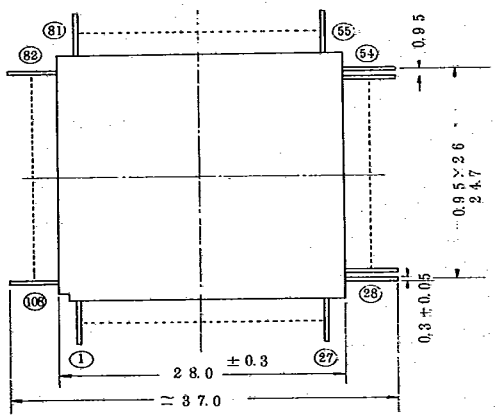
EVALUATION CHIP TERMINAL CABLE

No.	Terminal Name	I/O	No.	Terminal Name	I/O	No.	Terminal Name	I/O	No.	Terminal Name	I/O
1	Ⓐ	I	28	P_{U4}	O	55	f_{13}	O	82	V_D	I
2	Ⓑ	I	29	C_A	O	56	f_8	O	83	B_{M1}	O
3	Ⓒ	I	30	C_X	O	57	f_7	O	84	B_{M2}	O
4	J_{IN}	I	31	DIO_4	I/O	58	ϕ_1'	O	85	B_{M3}	O
5	I_1	I	32	DIO_3	I/O	59	ϕ_2'	O	86	B_{M4}	O
6	I_2	I	33	DIO_2	I/O	60	ACL	I	87	B_{L1}	O
7	I_3	I	34	DIO_1	I/O	61	O_{S4}	O	88	B_{L2}	O
8	I_4	I	35	K_1	I	62	O_{S3}	O	89	B_{L3}	O
9	I_5	I	36	α	I	63	O_{S2}	O	90	B_{L4}	O
10	I_6	I	37	β	I	64	O_{S1}	O	91	O_{15}	O
11	I_7	I	38	K_2	I	65	O_{11}	O	92	O_{25}	O
12	I_8	I	39	K_3	I	66	O_{21}	O	93	O_{35}	O
13	HLD	I	40	K_4	I	67	O_{31}	O	94	O_{45}	O
14	STP	I	41	GND	I	68	O_{41}	O	95	O_{16}	O
15	CTRL	I	42	(52)	O	69	O_{12}	O	96	O_{26}	O
16	PI	I	43	R_1'	O	70	O_{22}	O	97	O_{36}	O
17	J	O	44	R_2'	O	71	O_{32}	O	98	O_{46}	O
18	T	O	45	R_3'	O	72	O_{42}	O	99	O_{17}	O
19	P_{L1}	O	46	R_4'	O	73	O_{13}	O	100	O_{27}	O
20	P_{L2}	O	47	B_{P1}	O	74	O_{23}	O	101	O_{37}	O
21	P_{L3}	O	48	B_{P2}	O	75	O_{33}	O	102	O_{47}	O
22	P_{L4}	O	49	B_{P3}	O	76	O_{43}	O	103	O_{18}	O
23	P_{L5}	O	50	B_{P4}	O	77	O_{14}	O	104	O_{28}	O
24	P_{L6}	O	51	Sync.	I	78	O_{24}	O	105	O_{38}	O
25	P_{U1}	O	52	f_1	O	79	O_{34}	O	106	O_{48}	O
26	P_{U2}	O	53	f_4	O	80	NC		107	BA	I
27	P_{U3}	O	54	NC		81	O_{44}	O	108	V_C	I

≪ 108 Pin Quad Package ≫



UNIT: mm



Notes:

1) Precautions in Program Generator

Be sure to enter the SSRF instruction (5F) in 15 page 0 step at the start address for the Auto Clear. When restarting (0 page 0 step) from the system clock stop, stack registers SL and SU are inconstant, requiring their setting by the SSR instruction or TR1 instruction.

2) Difference between the LI3010EC and SM4

The LI3010EC is identical both in internal logic and input/output circuit to the SM-4. As described earlier, however, $R_{1\sim4}$ outputs and $H_{1\sim3}$ outputs are required to be lined up by an external circuit. The SM-4 has a built-in oscillating circuit with OSC-out and OSC-in terminals provided. The LI3010EC requires an oscillating circuit to be externally provided. Fig. 6 shows the example of an oscillating circuit.

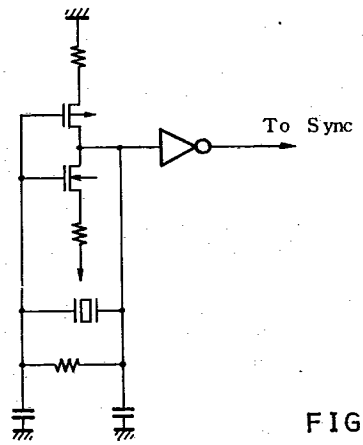


FIG. 6

3) 5V to 3V Level Shifter

The internal logic for the LI3010EC operates on V_D (-3V) in a similar manner to the SM-4. However, the output from the V_C (-5V) is transferred to $I_{1\sim8}$, Ⓐ Ⓑ Ⓒ Sync, STP and HLD inputs, which

are then level-shifted inside the LI3010EC.

4) Program counters P_{L_1} to P_{L_6} of the SM-4 count up in accordance with the polynomial code. This requires the program sequentially written from the start address to write program data in the PROM addresses in accordance with the polynomial code. For this, it is convenient to convert the polynomial code to a binary code. Addresses are assigned in the polynomial code sequence of 00, 32, 48 and so on for programming done so that outputs to the addresses are 00, 01, 02 and so on. Data to be written on PROM is shown on the following page.

FROM ADDRESS TRANSFORM

Address	Output	Address	Output
0 0	0 0	2 0	0 1
0 1	3 E	2 1	1 9
0 2	3 D	2 2	2 E
0 3	1 8	2 3	2 1
0 4	2 D	2 4	3 1
0 5	3 C	2 5	2 A
0 6	1 7	2 6	3 5
0 7	2 0	2 7	0 D
0 8	3 0	2 8	1 B
0 9	2 C	2 9	3 7
0 A	3 B	2 A	3 9
0 B	2 9	2 B	1 3
0 C	3 4	2 C	2 4
0 D	1 6	2 D	2 7
0 E	1 F	2 E	1 1
0 F	0 C	2 F	0 7
1 0	1 A	3 0	0 2
1 1	2 F	3 1	2 2
1 2	2 B	3 2	3 2
1 3	3 6	3 3	0 E
1 4	3 8	3 4	1 C
1 5	3 A	3 5	1 4
1 6	2 8	3 6	2 5
1 7	1 2	3 7	0 8
1 8	2 3	3 8	0 3
1 9	3 3	3 9	0 F
1 A	1 5	3 A	1 D
1 B	2 6	3 B	0 9
1 C	1 0	3 C	0 4
1 D	1 E	3 D	0 A
1 E	0 B	3 E	0 5
1 F	0 6	3 F	0 0