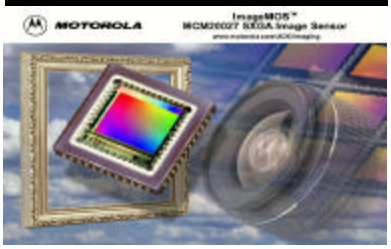
MCM20027
1.3 Megapixel

Advance Information

Color SXGA Digital Image Sensor
1280 x 1024 pixel progressive scan solid state image sensor with integrated CDS/PGA/ADC, digital programming, control, timing, and pixel correction features



Features:

- SXGA resolution, active CMOS image sensor with square pixel unit cells
- 6.0µm pitch pixels with patented pinned photodiode architecture
- Bayer-RGB color filter array with optional micro lenses
- High sensitivity, quantum efficiency, and charge conversion efficiency
- Low fixed pattern noise / Wide dynamic range
- Antiblooming and continuous variable speed shutter
- Single master clock operation
- Digitally programmable via I^2C interface
- Integrated on-chip timing/logic circuitry
- CDS sample and hold for suppression of low frequency and correlated reset noise
- 20X programmable variable gain to optimize dynamic range and facilitate white balance and iris adjustment
- 10-bit, pipelined algorithmic RSD ADC (DNL $\pm$0.5 LSB, INL $\pm$1.0 LSB)
- Automatic column offset correction for noise suppression
- Pixel addressability to support 'Window of Interest' windowing, resolution, and subsampling
- Encoded data stream
- 10 fps full SXGA at 13.5MHz Master Clock Rate
- Single 3.3V power supply
- 48 pin CLCC package

Part Number	Description	Package
MCM20027IBBL	Color RGB sensor with Lenslets	48 Pin CLCC
MCM20027IBMN	Monochrome sensor without Lenslets	48 Pin CLCC

The MCM20027 is a fully integrated, high performance CMOS image sensor with features such as integrated timing, control, and analog signal processing for digital imaging applications. The part provides designers a complete imaging solution with a monolithic image capture and processing engine thus making it a true "camera on a chip". System benefits enable design of smaller, portable, low cost and low power systems. Thereby making the product suitable for a variety of consumer applications including still/full motion imaging, security/surveillance, and automotive among others.

The imaging pixels are based on active CMOS pixels using pinned photodiodes that are realized using Motorola's sub-micron ImageMOS^{TM} technology. A maximum frame rate of 10 FPS at full resolution can be achieved, further the frame rate is completely adjustable without adjusting the system clock. Each pixel on the sensor is individually addressable allowing the user to control "Window of Interest" (WOI) panning and zooming. Control of sub-sampling, resolution, exposure, gain, and other image processing features is accomplished via a two pin I^2C interface. The sensor is run by supplying a single Master Clock. The sensor output is 10 digital bits providing wide dynamic range images.

ELECTRO STATIC DISCHARGE WARNING:
This device is sensitive to electrostatic discharge (ESD).ESD immunity meets Human Body Model (HBM) $\leq$ 1500 V and Machine Model (MM) $\leq$ 150 V Additional ESD data upon request. When handling this part, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its immediate performance and/or reduce the parts expected lifetime..

This document contains information on a new product.Specifications and information herein are subject to change without notice.

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Specifications

Image Size: 7.7mm x 6.1mm (9.82mm Diagonal, 1/2" Optic)

Resolution:1280 x 1024 pixels, available digital zoom and region of interest (ROI) windowing

Pixel Size: 6µm x 6µm

Monochrome Sensitivity: 1.8 V/Lux-sec

Min. Detectable Light Level: 3 Lux at 10FPS/F2 lens

Scan Modes: Progressive

Shutter Modes: Continuous Frame and Single Frame Rolling Shutter modes available

Readout Rate: 13.5MSPS

Frame Rate: 0-10 Full frames (1280x1024) per second

Max Master Clock Frequency: 13.5MHz

System Dynamic Range: 50dB

On Chip programmable gain: -9.5dB to 26dB

On Chip Image Correction: Column Fixed Pattern Correction

Analog to Digital Converter: 10-bit, RSD ADC (DNL +/-0.5 LSB, INL +/-1.0 LSB)

Power Dissipation: 250mW RMS, operating @13.5Mhz

Package: 48 pin ceramic LCC

Temperature Operating Range: 0-40^{o}C

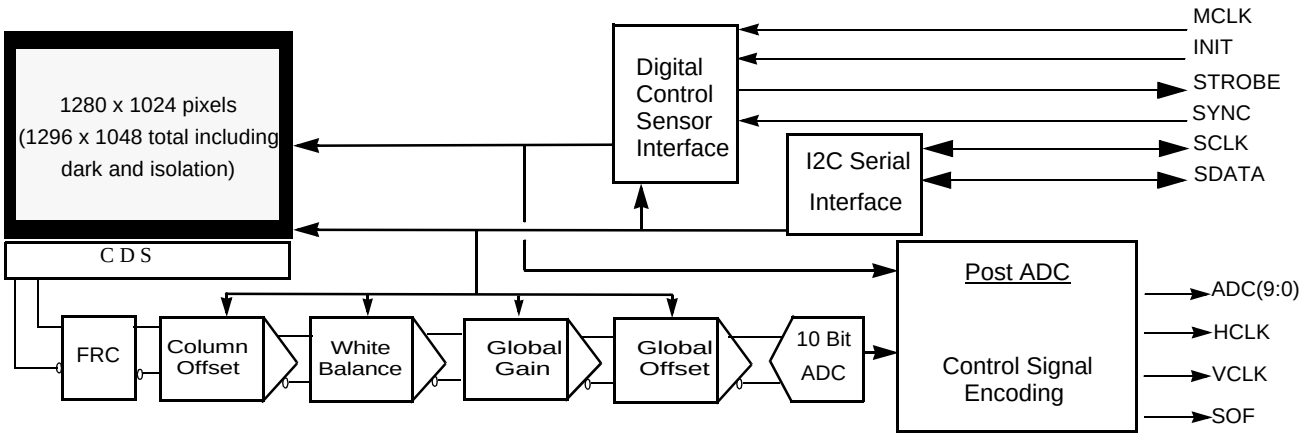
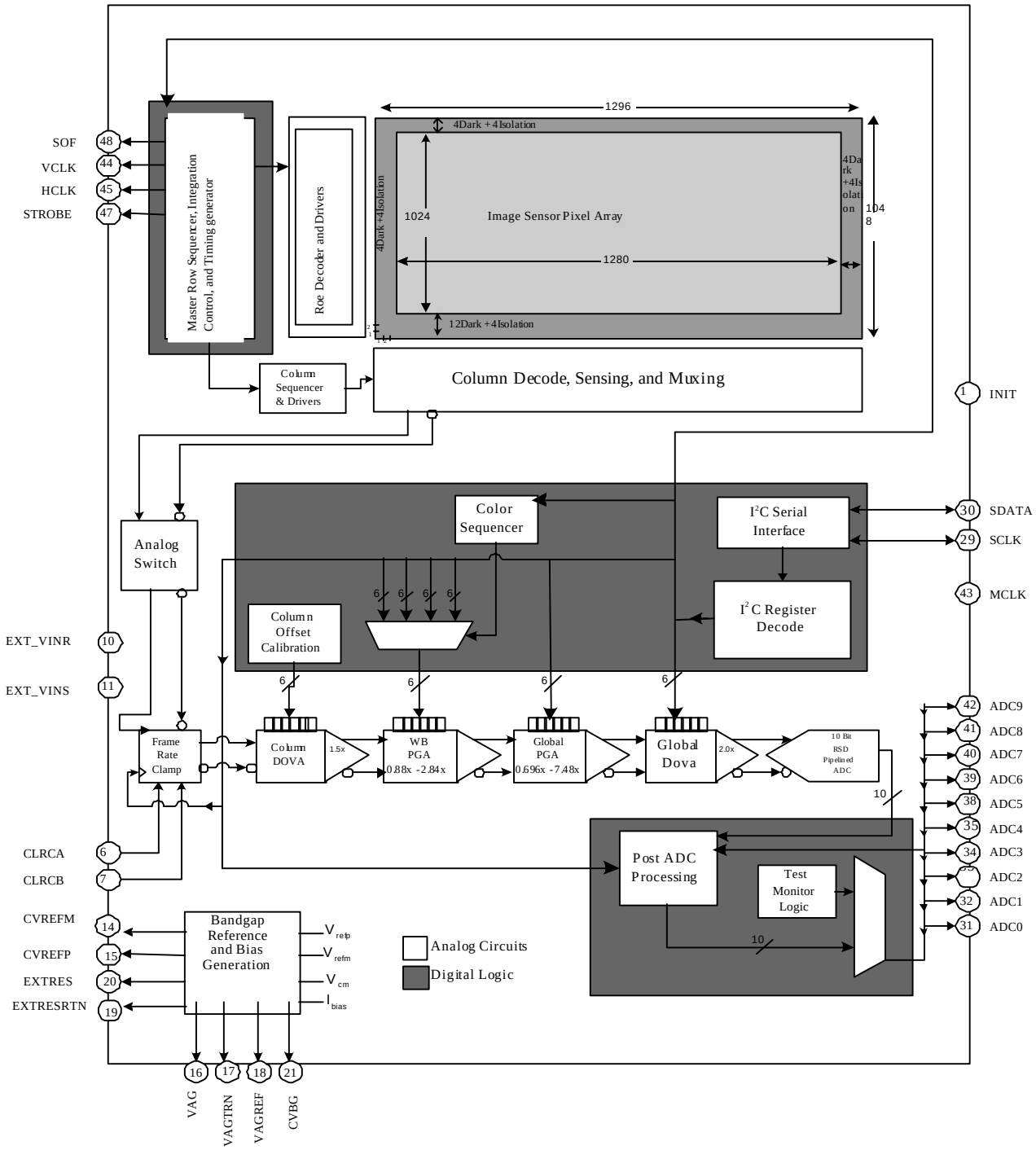


Figure 1. MCM20027 Simplified Block Diagram



See "MCM20027 Pin Definitions" on page 67 for more information

Figure 2. MCM20027 Detailed Block Diagram

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Reference Documentation

No	Description	Name of Document	Release Date	Contact/Location of Info
1	Digital Camera Reference Design utilizing the MCM20027	Roadrunner Application Note	May 4 2001	http://www.motorola.com/adc/imaging
2	Information on MCM20027 Optics	Optic Application note	Feb 7 2001	http://www.motorola.com/adc/imaging
3	Information on Strobe Timing	Strobe Timing Application Note	May 30 2001	http://www.motorola.com/adc/imaging

Table 1. Reference Documentation

1.0 MCM20027 Overview

The MCM20027 is a solid state CMOS Active CMOS Imager (ACI[TM]) that integrates the functionality of a complete analog image acquisition, digitizer, and digital signal processing system on a single chip. The image sensor comprises a format pixel array with 1280x1024 active elements. The image size is fully programmable to user defined windows of interest. The pixels are on a 6.0µm pitch. High sensitivity and low noise are a characteristic of the pinned "shared diffusion" photodiode architecture utilized in the pixels. Standard microlenses further enhance the sensitivity. The sensor is available with Bayer patterned Color Filter Arrays (CFAs) for color output or as a monochrome imager.

Integrated timing and programming controls allow video or still image capture modes.Frame rates are programmable while keeping Master Clock frequency constant. User programmable row and column start/stop allow windowing to a minimum 1x1 pixel window (see "Active Window of Interest Control" on page 12). Windowing can also be performed by subsampling in multiple pixel increments to allow digital zoom (see "Active Window Sub-sampling Control" on page 12).

The analog video output of the pixel array is processed by an on chip analog signal processing pipeline. Correlated Double Sampling (see "Correlated Double Sampling (CDS)" on page 15) eliminates the sensor reset noise without the need to capture and subtract a reset frame per live video frame. The Frame Rate Clamp (FRC) enables real time optical black level calibration and offset correction (see "Frame Rate Clamp (FRC)" on page 15). The programmable analog gain consists of exposure or global gain to map the signal swing to the ADC input range, and white balance gain to perform color white balance in the analog domain. The ASP signal chain consists of :

(1) Column op-amp(1.5X fixed gain)

(2) Column DOVA (1.5X fixed gain)

(3) White Balance PGA (0.88-2.82X)

(4) Global PGA (0.67X - 5.92X)

(5) Global DOVA (2.0X fixed gain)

These Digitally Programmable Amplifiers (DPGAs) allow real time color gain correction for Auto White Balance (see "White Balance Control PGA" on page 16) as well as global gain adjustment (see "Exposure Global Gain PGA" on page 16); offset calibration (see "Programmable Per-Column Offset" on page 16 and "Global Digital Offset Voltage Adjust (DOVA)" on page 19) can be done on a per column basis and globally. This per-column offset correction can be applied by using stored values in the on chip registers. A 10-bit Redundant Signed Digit (RSD) ADC converts the analog data to a 10-bit digital word stream. The fully differential analog signal processing pipeline serves to improve noise immunity, signal to noise ratio, and system dynamic range.

The sensor uses an industry standard two line I^2C complaint serial interface. (see page 26). The MCM20027 operates with a single 3.3V power supply (see "Electrical Characteristics" on page 53) with no additional biases and requires only a single Master Clock for operation upto 13.5MHz. It is housed in a 48 pin ceramic LCC package (see "MCM20027 Packaging Information" on page 69).

The MCM20027 is designed taking into consideration interfacing requirements to standard video encoders. In addition to the 10 bit bayer encoded data stream, the sensor outputs the valid frame, line and pixel sync signals needed for encoding. The sensor interfaces with a variety of commercially available video image processors to allow encoding into various standard video formats.

The MCM20027 is an elegant and extremely flexible single chip solution that simplifies a system designer's tasks of image sensing, processing, digital conversion, and digital signal processing to a high performance, low cost, low power IC. One that supports among others a wide range of low power, portable consumer digital imaging applications.

2.0 MCM20027 Architecture

2.1 Pixel Architecture

The MCM20027 ImageMOS[TM] (1) sensor comprises of a 1280 x 1024 active pixel array and supports progressive scan mode.

The MCM20027 utilizes the Kodak patented "Shared Floating Diffusion" pixel design [3]. This design enables two adjacent Row pixels' photodiodes to share the same floating diffusion transistor. (see Figure 2, on page 8).

1. ImageMOS is a Motorola trademark
2. Patents held jointly by Motorola and Kodak
3. Kodak Patent pending

The basic operation of the pixel relies on the photoelectric effect where due to its physical properties silicon is able to detect photons of light. The photons generate electron-hole pairs in direct proportion to the intensity and wavelength of the incident illumination. The application of an appropriate bias allows the user to collect the electrons and meter the charge in the form of a useful parameter such as voltage.

The pixel architecture also requires all pixels in a row to have common Reset , Transfer 1 and 2, Floating diffusion and Row Select gate controls. In addition all pixels have common supply (V_{DD}) and ground (V_{SS}) connections. An optimized cell architecture provides enhancements such as noise reduction, fill factor maximizations, and antiblooming. The use of pinned photodiodes (2) and proprietary transfer gate devices in the photoelements enables enhanced sensitivity in the entire visual spectral range and a lag free operation.

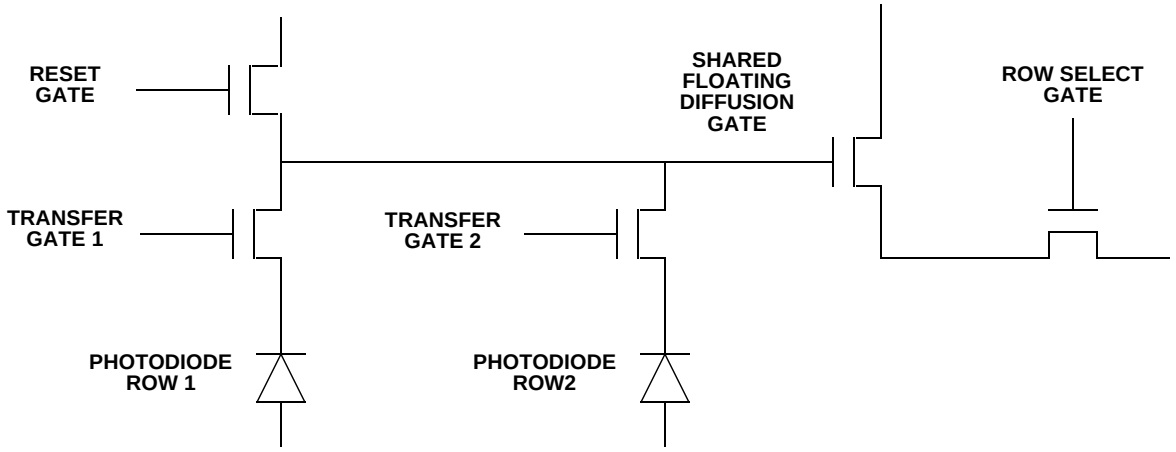
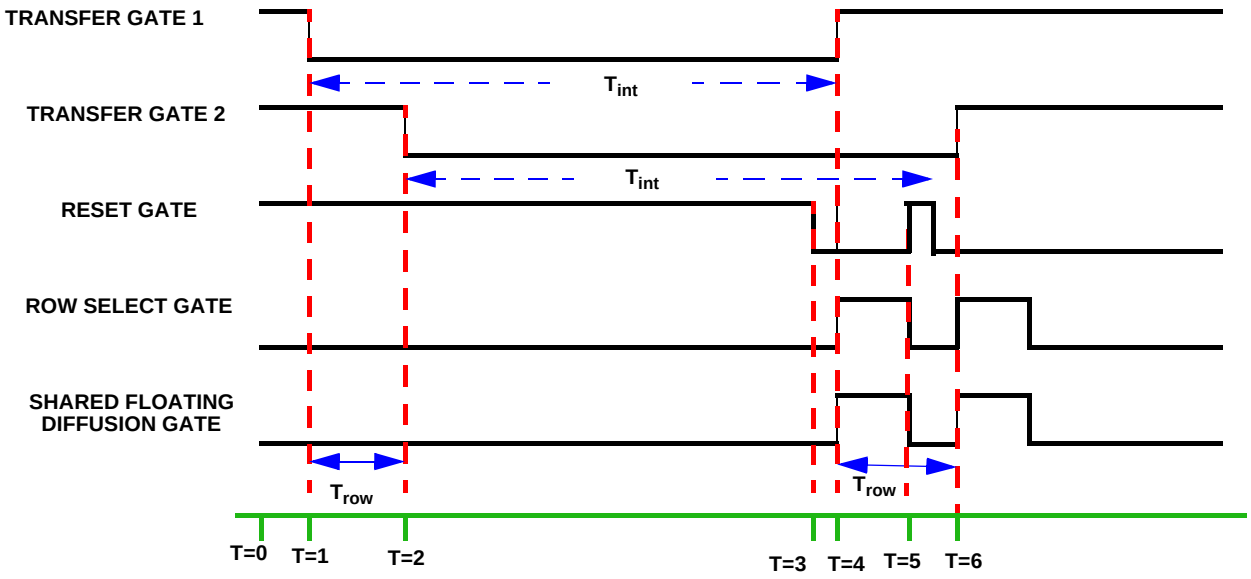


Figure 2. Shared Floating Diffusion Pixel Architecture



How it works?

In brief, initially during Integration @T=0, both Transfer Gates 1 and 2 and the Reset Gate is Open (On-Active High). Transfer Gate 1 then Closes (Off) @ T=1, thereby allowing Photodiode 1 to charge its well capacitance. At this time Photodiode 2 is held at Reset level by having Transfer Gate 2 and the Reset Gate open (On). After 1 Row Period [T_{row}], @T=2 ,Transfer Gate 2 closes (Off). This action causes Photodiode 2 to start charging. When the integration (charging) of Photdiode 1 has

neared completion, @ T=3, the Reset Gate closes (Off). The charge off the well capacitance of Photodiode 1 is then transfered to the Shared Floating Diffusion Gate @ T=4 when Transfer Gate 1 opens (On). Also @T=4 the Shared Diffusion gate and the Row Select gate opens (On). This action causes charge from the floating diffusion to be read out as a Voltage value for that pixel on Row 1. @T=5 the Row Select gate and the Floating diffusion close (Off) while the Reset gate opens (On). This is occurs in preparation of readout of Row 2.

When the integration (charging) of Photodiode 2 has neared completion, the Reset Gate closes (Off) again. The charge off the Well Capacitance of Photodiode 2 is then transfered to the Shared Floating Diffusion Gate @ T=6 when Transfer Gate 2 opens (On) and then the same readout procedure as before occurs.

The nominal photoresponse of the MCM20027 is shown in Figure 3

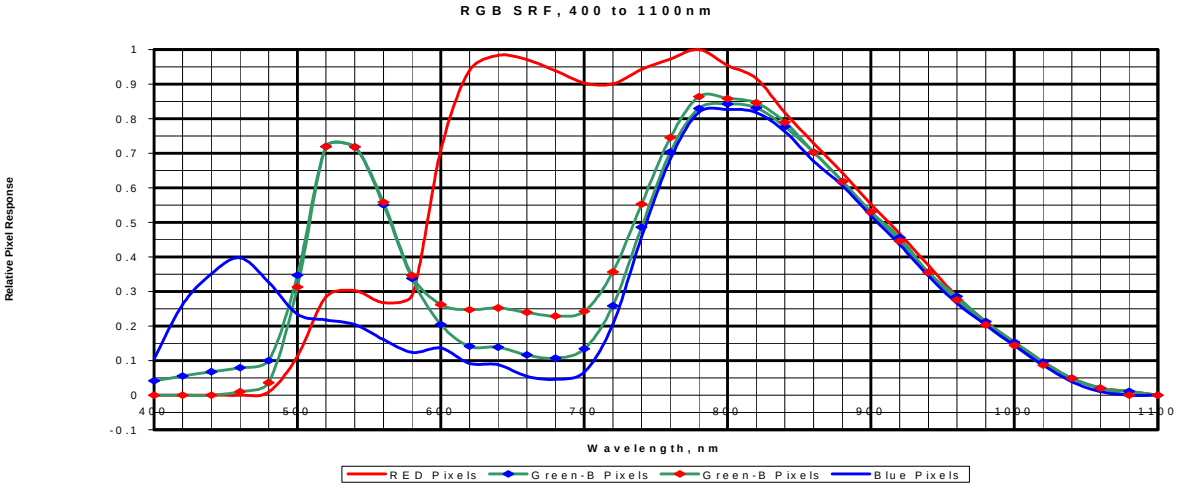


Figure 3. MCM20027 Nominal spectral response

In addition to the imaging pixels, there are additional pixels called dark and dummy pixels at the periphery of the imaging section (see Figure 2). The dark pixels are covered by a light blocking shield rendering the pixels underneath insensitive to photons. These pixels provide the sensor means to measure the dark level offset which is used downstream in the signal processing chain to perform auto black level calibration. The dummy pixels are provided at the array's periphery to eliminate inexact measurements due to light piping into the dark pixels adjacent to active pixels. The output of these pixels should be discarded.

Electronic shuttering, also known as electronic exposure timing in photographic terms, is a standard feature. The pixel integration time can be widely varied from a small fraction of a given frame readout time to the entire frame time.

2.2 Color Separation and Fill Factor Enhancement
The MCM20027 family is offered with the option of monolithic polymer color filter arrays (CFAs). The combination of an extremely planarized process and propriatary color filter technology result in CFAs with superior spectral and transmission properties. The standard option is a primary (RGB) "Bayer" pattern (see Figure 4), however, facility to produce customized CFAs including complementary (CMYG) mosaics also exists.

Applications requiring higher sensitivity can benefit from the optional micro-lens arrays shown in Figure 5. The lenslet arrays can improve the fill factor (aperture ratio) of the sensor by 1.5-2x depending on the F number of the main lens used in the camera system. Microlenses yield greatest benefits when the main lens has a high F number. As a caution, telecentric optical design is a requirement due to the limited optical acceptance angle of the lenslit. The optical acceptance angle is approximately 15 degrees (see figure 5a). Due to the lenslits being placed in the same area/position over all the photodiodes on the sensor, hence, care should be taken when taking into consideration the telecentric design for especially the outermost pixels.The fill factor of the pixels without microlenses is 32%. With Microlens the fill factor improves to approximately 45% to 50%.

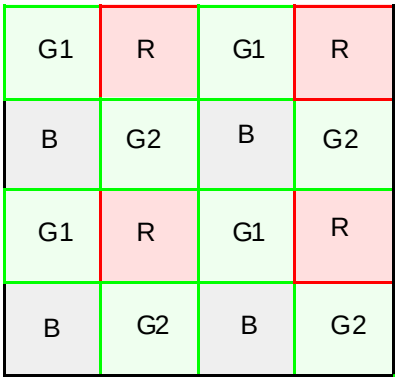


Figure 4. On-chip Bayer CFA

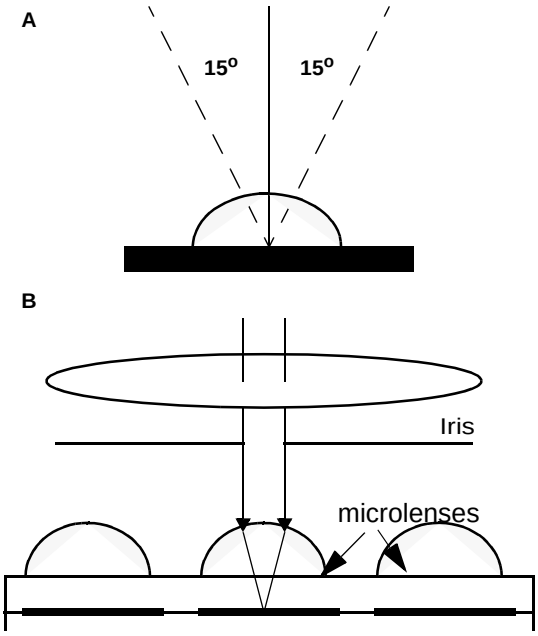


Figure 5. a) 15 degrees acceptance angle b)Improvement in pixel sensitivity results from focusing incident light on photo sensitive portions of the pixel by using microlenses

3.0 Frame Capture Modes

There exists two frame capture modes:

1) Continuous Frame Rolling Shutter mode (CFRS)

2) Single Frame Rolling Shutter mode (SFRS)

The sensor can be put into either one of the aforementioned modes by writing either “1” or “0” to Bit 6 of Capture Mode Control Register, (Table 29), on page 48.

3.1 Continuous Frame Rolling Shutter capture (CFRS) [Default]

The default mode of image capture is the “Continuous Frame Rolling Shutter” capture mode (CFRS). This mode will yield frame rates up to 10fps at 13.5 MHz MCLK. In this mode the image integration and row readout take place in parallel. While a row of pixels is being read out, another row(s) are being integrated. Readout of each row follows the Integration of that row. Therefore the Integration of the rows are staggered out due to the Readout of sequential rows occurring one after the other (see “Integration Time in CFRS mode:” on page 13).

In CFRS, after one frame has completed integrating, the first row of the second frame automatically begins integrating. The readout of the rows also follow the same routine. The waveforms depicting the CFRS output data stream refer to Figure 6, on page 11 and Figure 7, on page 12.

3.1.1 CFRS Video Encoded Data stream

The Pixel Data Stream Signal Control Register, (Table 53), on page 62 allows the user to select how the output pixel data stream in Continuous Frame Rolling Shutter mode is encoded/formatted. In default mode, internally generated signals SOF, VCLK, HCLK etc. drive the integration and readout of the pixel data frames but only the valid pixel data is readout of the sensor. When a “1” is written to bit 5 of the Pixel Data Stream Signal Control Register, (Table 53), on page 62, it causes the output pixel data to be encoded with SOF, VCLK and End Of Frame signals. It accomplishes this by attaching the pixel data with certain predefined signal data. The Video Encoded Signal Definitions, (Table 2), on page 10 defines the data that represents the SOF, VCLK and End of Frame signals.

Signal	Description	Data
SOF	Start of Row readout (i.e.. Readout of Row 1)	3FF3FF3FF3FF
VCLK	Start of Row readout of Rows 2+	3FF3FF000000
End Of Frame	Readout of last Row complete	000000000000

Table 2. Video Encoded Signal Definitions

3.2 Single Frame Rolling Shutter capture mode (SFRS)

This mode of capture refers to non-interlaced or sequential row by row scanning of the entire sensor in a single pass for the purpose of capturing a single frame. The start of Integration in this mode is triggered by the SYNC signal. Similar to the CFRS capture mode, Readout of each row follows the Integration of that row. Therefore the Integration of the rows are staggered out as well due to the Readout of the sequential rows occurring one after the other (see "Integration Time in SFRS mode" on page 14). This process continues until all Rows have been integrated and readout. Once readout of the entire frame is complete, the sensor awaits a new SYNC signal before it starts integration and readout of another frame.

The waveforms depicting the SFRS output data stream refer to Figure 8, on page 12

NOTE!! The faster the clock speed , the closer the sequential Integration start times are.

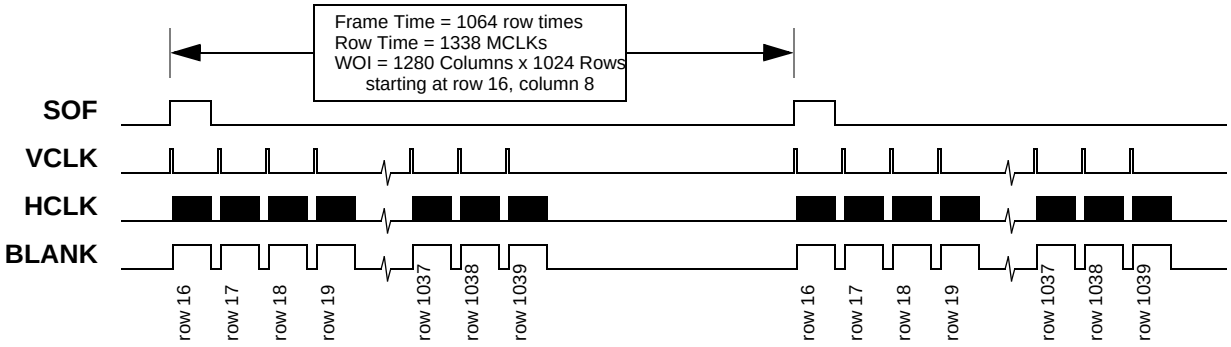


Figure 6. CFRS Default Frame Waveform

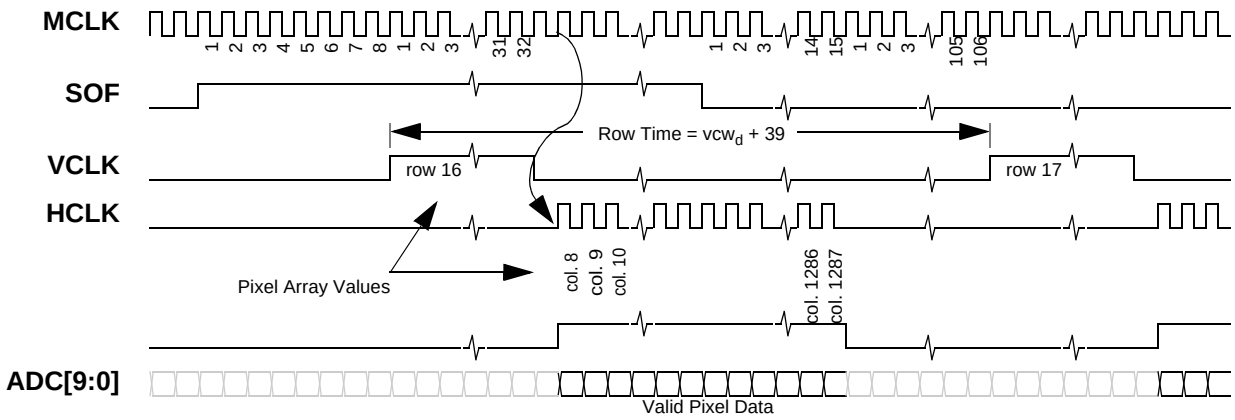


Figure 7. CFRS Default Line Waveform

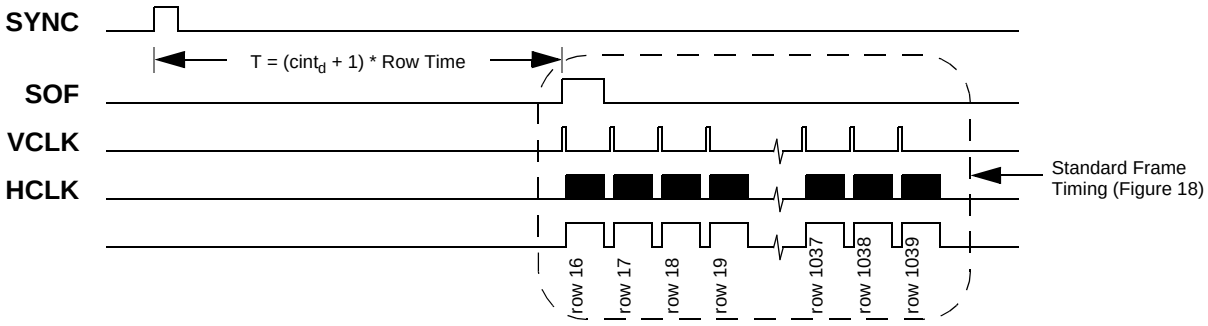


Figure 8. SFRS Waveform

4.0 Active Window of Interest Control

The pixel data to be read out of the device is defined as a 'Window of Interest' (WOI). The window of interest can be defined anywhere on the pixel array at any size. The user provides the upper-left pixel location and the size in both row and column depth to define the WOI. The WOI is defined using the WOI Pointer, WOI Depth, and WOI Width registers, (Table 32 on page 51 through Table 39 on page 53). Please refer to Figure 9 for a pictorial representation of the WOI within the active pixel array.

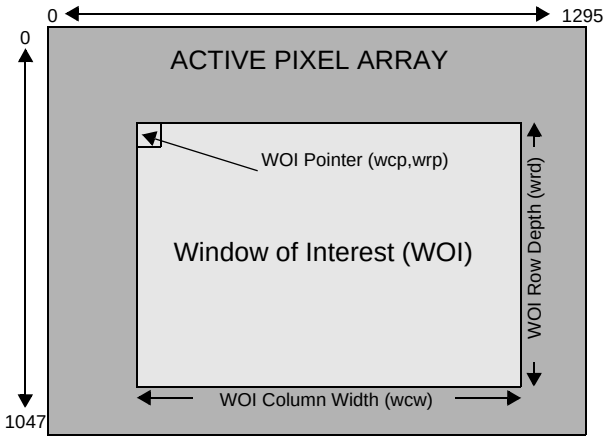


Figure 9. WOI Definition

5.0 Active Window Sub-sampling Control

The user can further control the size of the Active Window that is read out by sub sampling the already defined Active Window Of Interest (See "Active Window of Interest Control" on page 12). Subsampling enables the pixel data to be readout in 1 pixel or 2 pixel increments depending if you are subsampling in either monochrome (1 pixel) or bayer pixel (2 pixel) space in four different sampling rates in each direction: full, 1/2, 1/4, or 1/8. The user controls the subsampling via the Subsample Control Register, (Table 30), on page 49.

An example of Bayer space sub-sampling is shown in Figure 10.

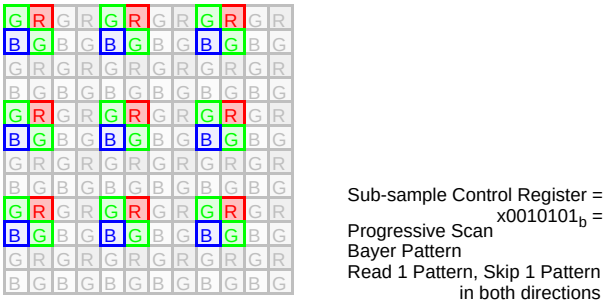


Figure 10. Bayer Space Sub-sampling Example

6.0 Frame Rate and Integration Time Control

In addition to the minimum time required to readout the selected resolution and WOI, the user has the ability to control the frame rates while operating in either Continuous Frame Rolling Shutter capture mode (CFRS) and Single Frame Rolling Shutter (SFRS).

The **frame rate** can be defined as the time required to readout an entire frame of data plus the required boundary timing. This is done by varying the size of a number of parameters identified in later sections, the main one being the Virtual Frame surrounding the WOI.

Please refer to Figure 11 for a pictorial description of the Virtual Frame and its relationship to the WOI

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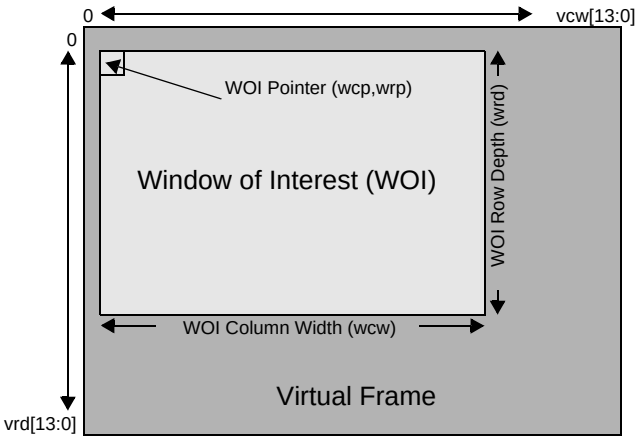


Figure 11. Virtual Frame Definition

6.1 CFRS Frame Time/Rate:

In Continuous Frame Rolling Shutter capture mode, the Frame time is completely defined by the size of the Virtual Frame and can be expressed as:

Frame Time = T_{frame} = (vrd_d + 1) * T_{row}

where **vrd_d** defines the number of rows in the virtual frame. The user controls vrd_d via the Virtual Frame Row Depth registers (Table 42 on page 55 and Table 43 on page 55).

Frame Rate = (Frame time)$^{-1}$

6.2 Integration Time in CFRS mode:

In Continuous Frame Rolling Shutter capture mode, the Integration time is defined as:

Integration Time=T_{int} = ($cint_d$ + 1) * T_{row}

where **$cint_d$** is the number of virtual row times desired for integration time. Therefore, the integration time in CFRS mode can be adjusted in steps of virtual frame row times.The user controls **$cint_d$** via the Integration Time MSB Register, (Table 40), on page 54 and Integration Time LSB Register, (Table 41), on page 55.

Row Time **(T_{row})** is the length of time required to read one row of the virtual frame and can be defined as:

T_{row} = (vcw_d + shs_d + shr_d + 19) * $MCLK_{period}$

where **vcw_d** defines the number of columns in the virtual frame and **shs_d** and **shr_d** are internal timing control registers.

The user controls **vcw_d** via the CFRS Virtual Frame Column Width registers (Table 44 on page 56 and Table 45 on page 56).

The user controls the **shs_d** and **shr_d** values via the Internal Timing Control Register 1 (shs time definition); Table 50 and Table 51, “Internal Timing Control Register 2 (shr time definition),” on page 60.

NOTE!! In Continuous Frame Rolling Shutter (CFRS) capture mode, the Integration time upper limit is bounded by the Frame time (see “CFRS Frame Time/Rate:” on page 13).

i.e.. T_{int} < T_{frame}

6.3 SFRS Frame Time/Rate:

In Single Frame Rolling Shutter capture mode the Frame time is defined as:

Frame time = T_{frame}= Integration time+Readout time

Readout time is the amount of time to readout the data after integration of the row has been completed. It is defined as follows:

Readout time = (vrd_d + 1) * T_{row}

where **vrd_d** defines the number of rows in the virtual frame. The user controls vrd_d via the CFRS Virtual Frame Row Depth registers (Table 42 on page 55 and Table 43 on page 55).

T_{row} = (vcw_d + shs_d + shr_d + 19) * $MCLK_{period}$

For **Integration time** see "Integration Time in SFRS mode" on page 14

6.3.1 Integration Time in SFRS mode

The Integration time in Single Frame Rolling Shutter capture mode is the same as in Rolling Shutter Capture Mode. For further information, see **"Integration Time in CFRS mode:" on page 13**. T**he only difference is that in this mode the Integration time is NOT bounded by the Frame time**

6.4 Example of Frame time/rate and Integration Time in CFRS and SFRS modes

The following illustrates how to determine the Frame time/rate and Integration time in both capture modes:

Assumptions:

1) Active Window of Interest = 1280 x 1024

i.e.. **(wcw_d)**=1279

(**wrd_d**)=1023

2) Virtual Column Width (**vcw_d**)= 1290

3) Virtual Row Depth (**vrd_d**) = 1034

4) Sample & hold time (**shs_d**) = 10

5) Sample & hold time (**shr_d**) = 10

6) Integration Time (**$cint_d$**)= 350

7) MCLK = 13.5 Mhz

NOTE!! vcw_d and $cint_d$ are typically varied frame to frame

Calculations:

Row Time =Trow = (vcwd + shsd + shrd + 19)

= (1290 + 10 + 10 + 19) / 13.5e6

= 98.44µs

Integration Time = (cintd + 1) * Trow

=(350+1)*98.44µs

=34.5ms

Readout time = (vrdd + 1) * Trow

= Frame time in CFRS mode

Frame Time in CFRS mode = (vrd_d + 1) * Trow

T_{frame} =(1034 + 1)* 98.44

= 101.34 ms

Frame Time in SFRS mode =

T_{frame} = Integration time+Readout time

= 34.5ms + 101.34ms

= 135.84ms

Results

Capture Mode	T_{int}	T_{frame}
CFRS	**34.5ms**	**101.34 ms**
SFRS	**34.5ms**	**135.84ms**

NOTE!! CFRS Integration time = 34.5ms because:

T_{int} < T_{frame} = (vrd_d + 1) * T_{row}

(see "Integration Time in CFRS mode:" on page 13)

7.0 Analog Signal Processing Chain Overview

The MCM20027's analog signal processing (ASP) chain incorporates Correlated Double Sampling (CDS), Frame Rate Clamp (FRC), two Digitally Programmable Gain Amplifiers (DPGA), Offset Correction (DOVA), and a 10-bit Analog to Digital Converter (ADC).

To see a pictorial depiction of this chain refer to "Specifications" on page 2

7.1 Correlated Double Sampling (CDS)

The uncertainty associated with the reset action of a capacitive node results in a reset noise which is equal to kTC; C being the capacitance of the node, T the temperature and k the Boltzmann constant. A common way of eliminating this noise source in all image sensors is to use Correlated Double Sampling. The output signal is sampled twice, once for its reset (reference) level and once for the actual video signal. These values are sampled and held while a difference amplifier subtracts the reference level from the signal output. Double sampling of the signal eliminates correlated noise sources (see ."Conceptual block diagram of CDS implementation." on page 15)

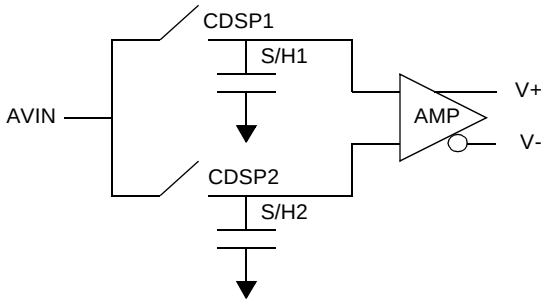


Figure 12. Conceptual block diagram of CDS implementation.

7.2 Frame Rate Clamp (FRC)

The FRC (Figure 13) is designed to provide a feed forward dark level subtract reference level measurement. In the automatic FRC mode, the optical black level reference is re-established each time the image sensor begins a new frame. The MCM20027 uses optical black (dark) pixels to aid in establishing this reference.

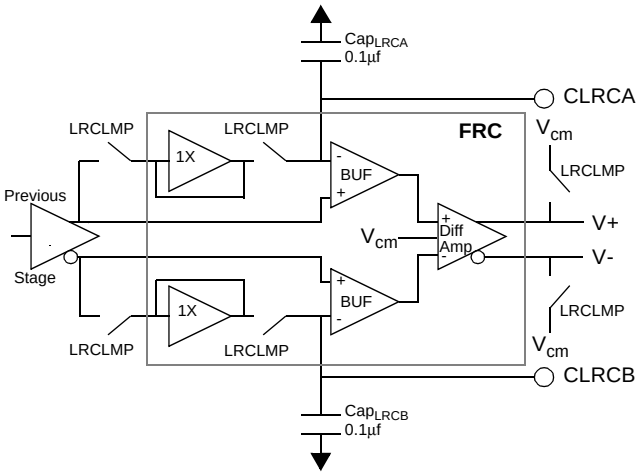


Figure 13. FRC Conceptual Block Diagram

On the MCM20027, dark pixel input signals should be sampled for a minimum of 137µs to allow the two 0.1µF capacitors at the CLRCA and CLRCB pins sufficient time to charge for 10-bit accuracy. This guarantees that the FRC's "droop" will be maintained at ≤750 µV**,** thus assuring the specified ADC 10-bit accuracy at ±0.5 LSB. Therefore, at maximum operational frequency (13.5 MHz), the imager would require a number of frames to establish the dark pixel reference for subsequent active pixel processing. The dark pixel sample period is automatically controlled internally and it is set to skip the first 3 dark rows and then sample the next 2 dark rows. When "dark clamping" is active, each dark pixel is processed and held to establish pixel reference level at the CLRCA and CLRCB pins. During this period, the FRC's differential outputs (V+ and V- on the Diff Amp, Figure 13) are clamped to V_{cm}. Together, these actions help to eliminate the dark level offset, simultaneously establishing the desired zero code at the ADC output.

Care should be exercised in choosing the capacitors for the CLRCA, B pins to reflect different frame rates.

The user can disable this function via the FRC Definition Register; Table 54 and the Power Configuration Register, (Table 19), on page 41 (Check this - should be referring o FRC clamp ON/OFF) which will allow the ASP

chain to drift in offset Per-Column Digital Offset Voltage Adjust (DOVA), and controls the number of rows to clamp on.

7.3 Programmable Per-Column Offset

A programmable per-column offset adjustment is available on the MCM20027. In order to reduce the risk and have the ability to cover any mode of repetitive column Fixed Pattern Noise (FPN), there exists 64 registers that can be programmed with a DC offset that is added to all columns. (Mod64 Column Offset registers; Table 27). Each register is 6 bits, (5 bits plus 1 sign bit), providing+/- 32 register values. The DC register values is added to each of the 64 columns registers to provide the total offset value. This set of 64 values is then repeatedly applied to each bank of 64 in the sensor via the column DOVA stage of the ASP chain.

The Column DOVA DC Register; Table 26, is used to set the initial offset of the pixel output in a range that will facilitate per-column offset data generation for varying operational conditions. In most operational scenarios, this register can be left in its default state of 00_h. This is a pre-image processing gain in comparison to the Global DOVA Register (see section)which is a post image processing chain gain (pre A2D gain)

7.4 Digitally Programmable Gain Amplifiers (DPGA) for White Balance and Exposure Gain

Two DPGAs are available in the analog signal processing chain. These are used to perform white balance and exposure gain functions.

7.4.1 White Balance Control PGA

The sensor produces three primary color outputs, Red, Green and Blue. These are monochrome signals that represent luminance values in each of the primary colors. When added in equal amounts they mix to make neutral color. White balancing is a technique where the gain coefficients of the green(0), red, blue, and green(3) pixels comprising the Bayer pattern (see Figure 14.) are set so as to equalize their outputs for neutral color scenes. Since the sensitivity of the two green pixels in the Bayer pattern may not be equal, an individual color gain register is provided for each component of the Bayer pattern.

Once all color gain registers are loaded with the desired gain coefficients ,according to which gain mode (see "Gain Modes" on page 17) has been set, white balance is then achieved in real time and in analog space. These gain coefficient values are then selected and applied to the pixel output via a high speed path, the delay of which is much shorter than the pixel clock rate. Real time updates can be performed to any of the gain registers. However, latency associated with the I^2C interface should be taken into consideration before changes occur. In most applications, users will be able to assign predefined settings such as daylight, fluorescent, tungsten, and halogen to cover a wide gamut of illumination conditions.

Both DPGA designs use switched capacitors to minimize accumulated offset and improve measurement accuracy and dynamic range. The white balance gain registers are 6-bits and can be programmed to allow gain of 0.696x to 2.74x in varying steps.

The user programs the individual gain coefficients into the MCM20027 via the Color Gain Registers (Table 8 through Table 11). For the default Bayer configuration of the color filter array; Figure 4, the Color Gain Register addresses are as follows: Reg (00h): green pixel of a green-red row; Reg (01h): red pixel; Reg (02h): blue pixel; and Reg (03h): green pixel of a blue-green row.

The MCM20027 is presently available with only a Bayer CFA, however, it is designed to support other novel color configurations. This is accomplished via the Color Tile Configuration Register, (Table 12), on page 37 and the Color Tile Row Definition registers (Table 13 through Table 16).

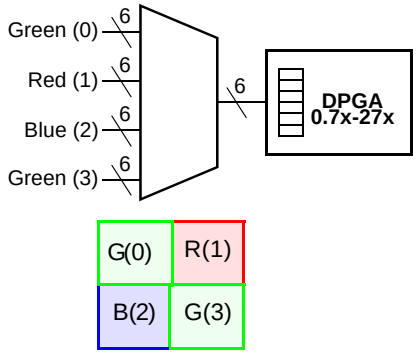


Figure 14. Color Gain Register Selection

7.4.2 Exposure Global Gain PGA

The global gain DPGA provides a 0.67x to 7.5x (approx) programmable gain adjustment for dynamic range. The gain of the amplifier is linearly programmable using a six bit gain coefficients on 2 6-bit PGA gain registers in varying steps depending on which exposure gain mode it is set at i.e. RAW or LIN or LIN2 (PGA Gain Mode, (Table 25), on page 45). The user programs the global gain via the Exposure PGA Global Gain Register A, (Table 23), on page 44.

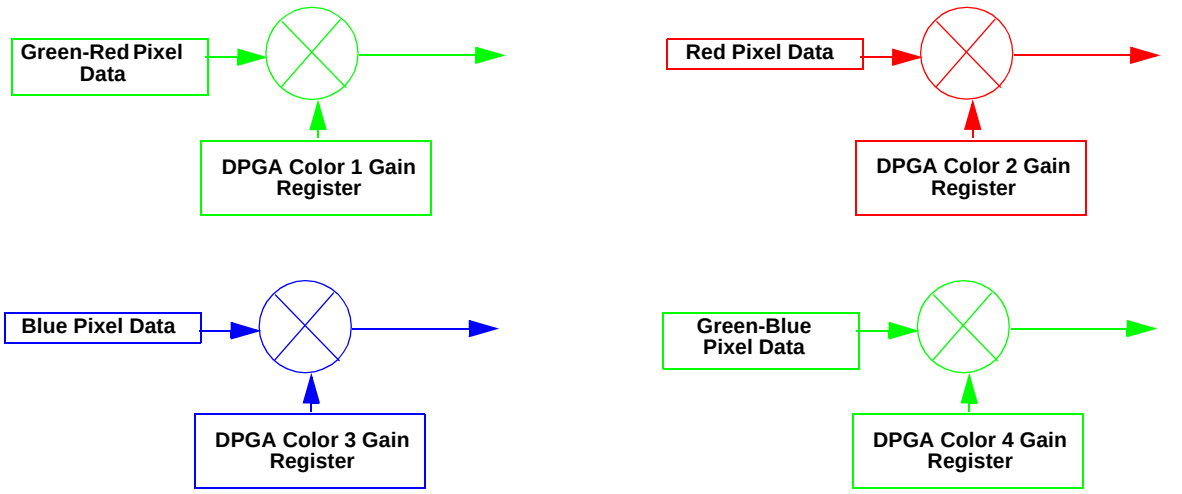
7.4.3 Gain Modes

There exists different gain modes that are available when the sensor is performing White Balance and Exposure gain. The Gain mode utilized for White balance and Exposure gain can be selected by the user writing different values to the register described in Table 25, “PGA Gain Mode,” on page 45.

There are two different Gain modes for White Balance and there are three different Gain modes for the Exposure gain refer to White Balance Gain modes and Gain Formulas; Table 3 and Exposure Gain modes and Gain Formulas; Table 4 for more info.

Register No	Register Name	Variable	Gain Modes	Gain Steps	Gain Formula	Gain Range
00h	DPGA Color 1 Gain Register; Table 8	cg1	RAW	0-32	0.6956 + (0.02174* $cg1_d$)	0.69-1.39
				33-63	1.391+ (0.0434* ($cg1_d$-32)	1.39-2.74
			LINEAR	0-47	0.6956 +(0.0434 x $cg1_d$)	0.69-2.74
01h	DPGA Color 2 Gain Register; Table 9	cg2	RAW	0-32	0.6956 + (0.02174* $cg2_d$)	0.69-1.39
				33-63	1.391+ (0.0434* ($cg2_d$-32)	1.39-2.74
			LINEAR	0-47	0.6956 +(0.0434 x $cg2_d$)	0.69-2.74
02h	DPGA Color 3 Gain Register; Table 10	cg3	RAW	0-32	0.6956 + (0.02174* $cg3_d$)	0.69-1.39
				33-63	1.391+ (0.0434* ($cg3_d$-32)	1.39-2.74
			LINEAR	0-47	0.6956 +(0.0434 x $cg3_d$)	0.69-2.74
03h	DPGA Color 4 Gain Register; Table 11	cg4	RAW	0-32	0.6956 + (0.02174* $cg4_d$)	0.69-1.39
				33-63	1.391+ (0.0434* ($cg4_d$-32)	1.39-2.74
			LINEAR	0-47	0.6956 +(0.0434 x $cg4_d$)	0.69-2.74

Table 3. White Balance Gain modes and Gain Formulas

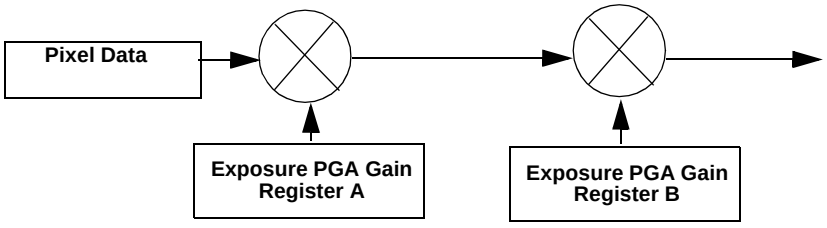


NOTE!! The Diagrams above illustrates how the Color Gain Registers apply the gain onto each individual color pixel data:

Register No	Register Name	Variable	Gain Modes	Gain Steps	Gain Formula	Gain Range
10h	Exposure PGA Global Gain Register A; Table 23	gg1	RAW	0-32	0.6956 + (0.02174* $gg1_d$)	0.69-1.39
				33-63	1.391+ (0.0434* ($gg1_d$-32)	1.39-2.74
			LINEAR	0-47	0.6956 +(0.0434 x $gg1_d$)	0.69-2.74
			LINEAR 2	0-67	0.6956 + (0.0434 * $gg2_d$)	0.69-3.60
21h	Exposure PGA Global Gain Register B; Table 24	gg2	RAW	0-32	0.6956 + (0.02174* $cg2_d$)	0.69-1.39
				33-63	1.391+ (0.0434* ($cg2_d$-32)	1.39-2.74
			LINEAR	0-47	0.6956 +(0.0434 x $cg2_d$)	0.69-2.74
			LINEAR 2	0-67	0.6956 + (0.0434 * $gg2_d$)	0.69-3.60

Table 4. Exposure Gain modes and Gain Formulas

The Diagram below illustrates how the Exposure Gain Registers apply the gain onto the pixel data:



7.5 Global Digital Offset Voltage Adjust (DOVA)

A programmable global offset adjustment is available on the MCM20027. A user defined offset value is loaded via a 6-bit signed magnitude programming code via the Global DOVA Register, (Table 28), on page 47.

Offset correction allows fine-tuning of the signal to remove any additional residual error which may have accumulated in the analog signal path. This function is performed directly before analog to digital conversion and introduces a fixed gain of 2.0X. This feature is useful in applications that need to insert a desired offset to adjust for a known system noise floor relative to AVSS and offsets of amplifiers in the analog chain.

7.6 Analog to Digital Converter (ADC)

The ADC is a fully differential, low power circuit. A pipelined, Redundant Signed Digit (RSD) algorithmic technique is used to yield an ADC with superior characteristics for imaging applications.

Integral Noise Linearity (INL) and Differential Noise Linearity (DNL) performance is specified at $\pm$1.0 and $\pm$0.5, respectively, with no missing codes. The input voltage resolution is 2.44 mV with a full-scale 2.5 V_{pp} input (2.5 $V_{pp}/2^{10}$). The input dynamic range of the ADC is programmed via a Programmable Voltage Reference Generator. The positive reference voltage (VREFP) and negative reference voltages (VREFM) can be programmed from 2.5V to 1.25V and 0V to 1.25V respectively in steps of 5mV via the Reference Voltage Registers (Table 17 and Table 18). This feature is used independently or in conjunction with the DPGAs to maximize the system dynamic range based on incident illumination. The default input range for the ADC is 1.9V for VREFP and 0.6V for VREFM hence allowing a 10 bit digitization of a 1.3V peak to peak signal.

8.0 Sensor External Controls (Additional Operational Conditions)

The MCM20027 includes initialization, standby modes, and external reference voltage outputs to afford the user additional applications flexibility.

8.1 Initialization

The INIT input pin (#42) controls reinitialization of the MCM20027. This serves to assure controlled chip and system startup. Control is asserted via a logic high input. (i.e.. Asserting a Logic high “1” initializes all the Registers, while asserting a Logic low “0” returns the sensor to normal operation). This state must be held a minimum of 1 ms and a 1 ms “wait period” should be allowed before chip processing to ensure that the start-up routines within the MCM20027 have run to completion, and to guarantee that all holding and bypass capacitors, etc. have achieved their required steady state values.

Tasks which are accomplished during startup include: reset of the utility programming registers and initialization to their default values (please refer to previous section for settings), reset of all internal counters and latches, and setup of the analog signal processing chain.

Another method of saving power consumption is to applying an active high signal to the INIT pin (#42) but Note - Doing this will also cause initialization of the chip

.

8.2 Standby Mode

The standby mode option is implemented to allow the user to reduce system power consumption during periods which do not require operation of the MCM20027. This feature allows the user to extend battery life in low power applications.

By utilizing this mode, the user may reduce dynamic power consumption from 250mW RMS nominal @13.5MHz to $\leq$100 uW in the standby mode.

The standby mode is activated by writing a “1” to bit 0 of “Power Configuration Register” on page 41. Writing a “0” restores normal operation.

8.3 Tristate Mode

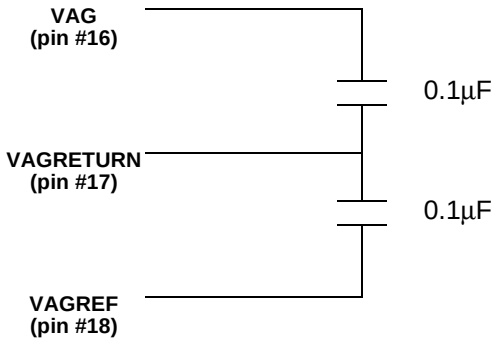
The sensors HCLK, SOF, VCLK, SYNC and STROBE output signals as well as the pixel output data can be tristated via the Tristate Control Register, (Table 21), on page 42.

8.4 References CVREFP, CVREFM

The MCM20027 contains all internally generated references and biases on-chip for system simplification. An internally generated differential bandgap regulator derives all the ADC and other analog signal processing required references. The user should connect 0.1µF capacitors to the CVREFP and CVREFM pins (#15 and #14 respectively) to accurately hold the biases.

8.5 Common Mode References: VAG, VAGREF and VAGRETURN

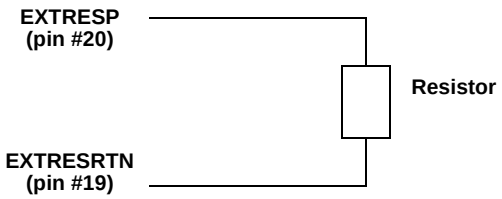
The MCM20027 holds the Common Mode Reference Voltages on the chip to a stable value. In order to achieve this stable value, the VAG (pin #16), VAGREF(pin #18) and VAGRETURN (pin #17) have to be connected to two 0.1µF capacitors in the manner described in the diagram below:



8.6 Internal Bias Current Control

The ASP chain has internally generated bias currents that result in an operating power consumption of nearly 400mW approx. (Accurate value will be given upon sensor testing). By attaching a resistor between pin 20, EXTRES; and Pin19, the user can reduce the power consumption of the device. This feature is enabled by writing a 1_b to bit **res** of the Power Configuration Register. Additional power savings can be achieved at lower clock rates. Note - The External Bias resistor Input pin (EXTRESP - pin #20) should be connected to the

ETRESRTN (pin#19) in the manner described in the diagram below.



9.0 Sensor Output/Input Signals

9.1 Start Of Data Capture (SYNC)

This signal is utilized by the sensor to indicate the start of integration (data capture) in Single Frame Rolling Shutter capture mode (SFRS). For more info refer to Figure 15, on page 22, Figure 8, on page 12 and Figure 16, on page 24. This signal can be generated internally by the sensor or be driven via Pin # 46 of the sensor (see Figure 20, on page 67). To set whether the signal is generated internally or externally, as well as other settings to this signal, refer to Sync and Strobe Control register, (Table 31), on page 50.

9.2 Start Of Row Readout (SOF)

This signal triggers/indicates the start of Row Readout of the frame. This signal is an Output and can be read via Pin # 48 of the sensor (see Figure 20, on page 67). The SOF signal delay as well as its length can be set by the user via SOF Delay Register, (Table 46), on page 57 and SOF & VCLK Signal Length Control Register, (Table 48), on page 57. For timing diagrams depicting the use of the SOF signal refer to Figure 15, on page 22, Figure 6, on page 11, Figure 7, on page 12 ,Figure 8, on page 12 and Figure 16, on page 24.

9.3 Horizontal Data SYNC (VCLK)

This signal triggers the Readout of the sequential rows of the frame. This signal is an Output and can be read via Pin # 44 of the sensor (see Figure 20, on page 67). The VCLK signal delay in relation to SOF, as well as its length can be set by the user via VCLK Delay Register, (Table 47), on page 57 and SOF & VCLK Signal Length Control Register, (Table 48), on page 57. For timing diagrams depicting the use of the VCLK signal refer toFigure 15, on page 22, Figure 6, on page 11, Figure 7, on page 12 ,Figure 8, on page 12 and Figure 16, on page 24.

9.4 Data Valid (HCLK)

This signal triggers/indicates a single active pixel data has been readout (eg Column 5 of Row 10 data has been read out). This signal is an Output and can be read via Pin # 45 of the sensor (see Figure 20, on page 67). The HCLK signal delay can be set by the user via HCLK Delay Register, (Table 52), on page 60. For timing diagrams depicting the use of the HCLK signal refer to Figure 15, on page 22, Figure 6, on page 11, Figure 7, on page 12 ,and Figure 8, on page 12.

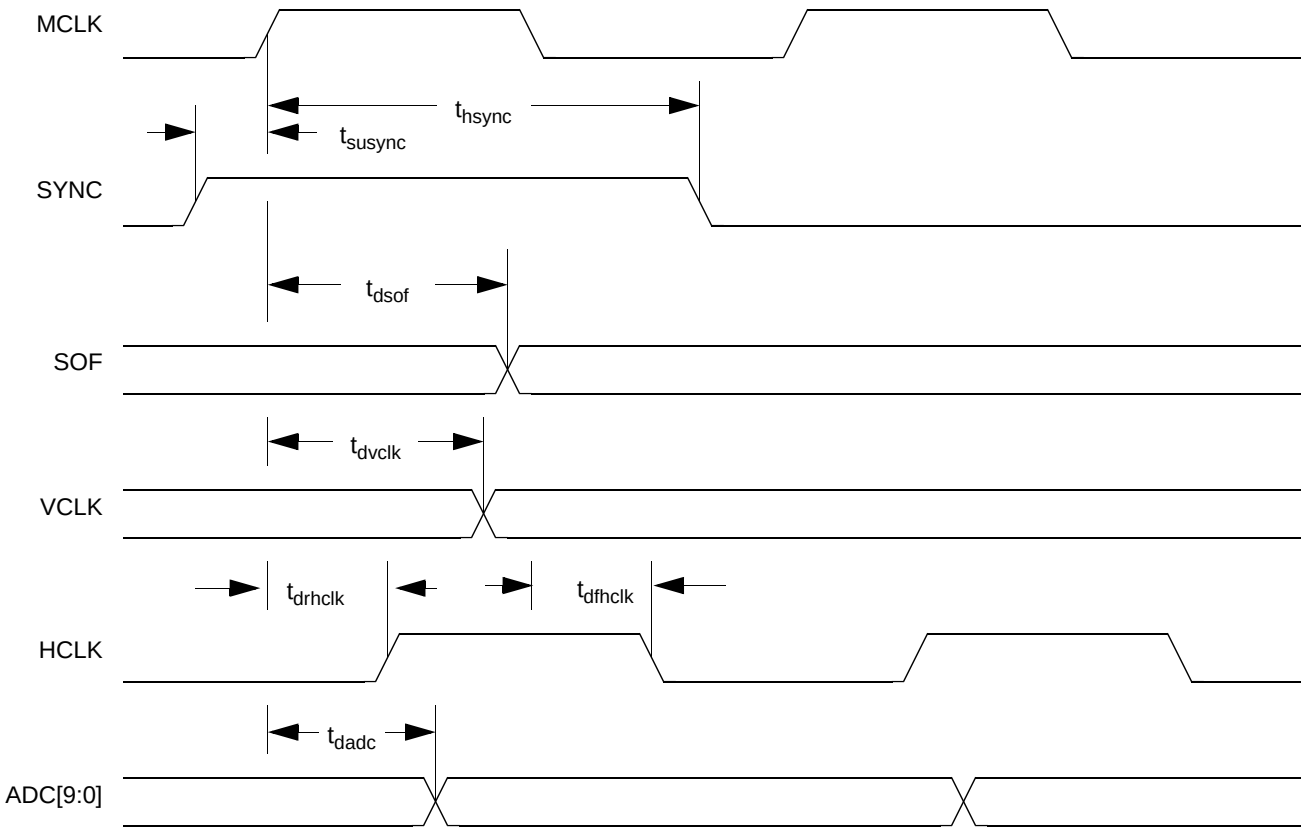


Figure 15. Pixel Data Bus Iinterface Timing Specifications (see Table Below)

PIXEL DATA BUS INTERFACE TIMING SPECIFICATIONS (see Figure 15)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{max}	MCLK maximum frequency	1	11.5	13.5	MHz
t_{hsync}	SYNC hold time w.r.t MCLK	3.5	-	9	ns
t_{susync}	SYNC setup time w.r.t MCLK	3.0	-	8.5	ns
t_{dsof}	MCLK to SOF delay time	8	13	21.5	ns
t_{dvclk}	MCLK to VCLK delay time	8.5	13.5	22	ns
t_{drhclk}	Rising edge of MCLK to rising edge of HCLK delay time	7.5	13	22	ns
t_{dfhclk}	Falling edge of MCLK to falling edge of HCLK delay time	3	5	10.5	ns
t_{dadc}	MCLK to ADC[9:0] delay time	8	13	21.5	ns
t_{strobe}	MCLK to STROBE delay time	8	13	21.5	ns

9.5 Strobe Signal

The Strobe signal is a output pin on the MCM20027 sensor that can be used to activate 'Flash/Strobe illumination modules". It can be activated by writing a "1" to bit 3 of "Sync and Strobe Control register" on page 50 while in SFRS mode. When activated, the Strobe signal goes high (Active) when all Rows are Integrating simultaneously, and ends one Row period ($\mathbf{T_{row)}}$ before the last Row begins to Integrate. (see 3"Frame Rate and Integration Time Control" on page 13). The start of the strobe signal can also be set by the user. In default mode, when the strobe is activated, the signal fires 2 Row Periods ($\mathbf{T_{row}}$) before the first Row begins to Readout and last for a length of 1 $\mathbf{T_{row}}$ .A sample timing diagram for the Strobe signal can be seen in Figure 16, on page 24:

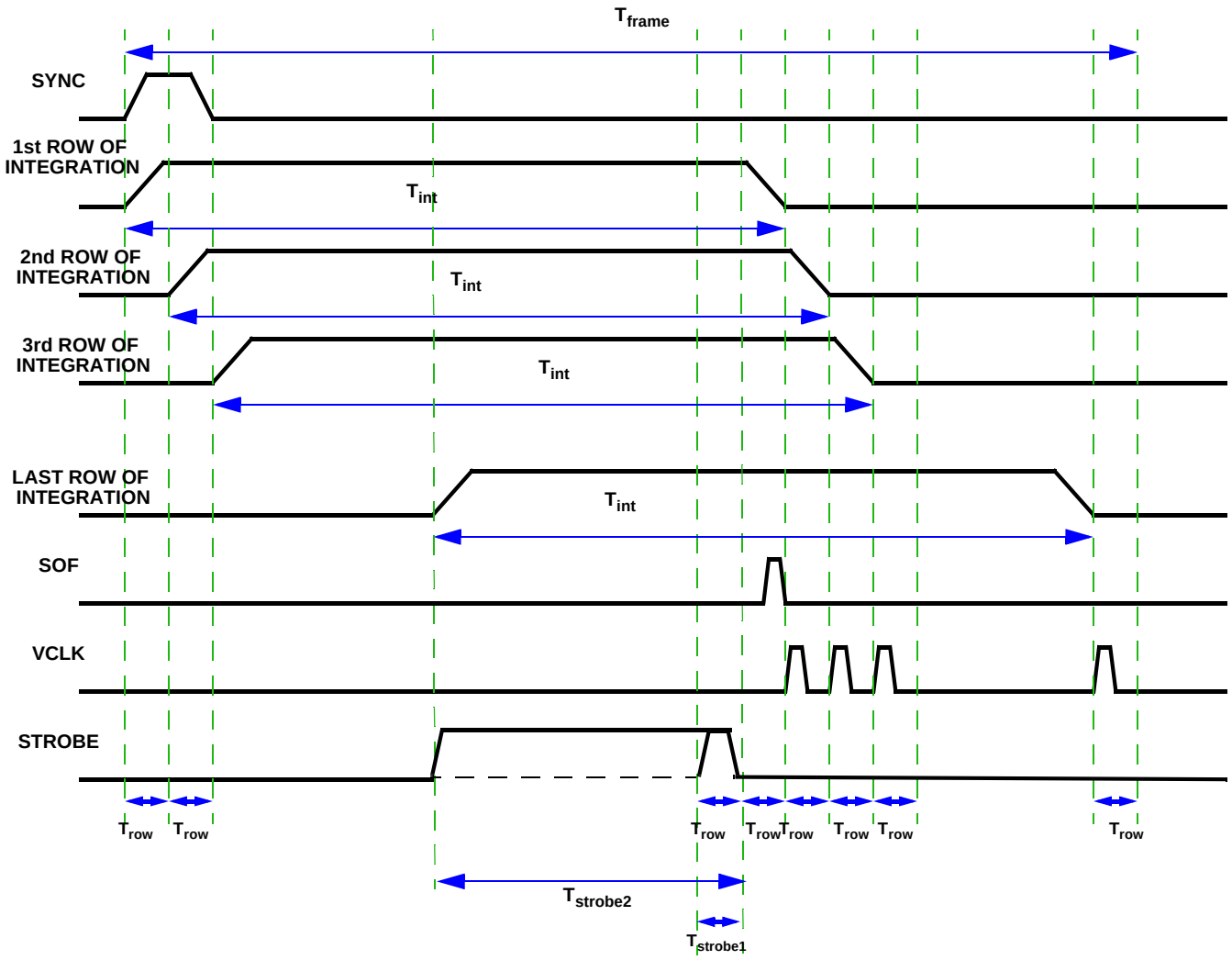


Figure 16. Strobe Timing Diagram in SFRS capture mode

To ensure that Strobe signal fires, the integration time must be large enough to ensure that all rows are integrating simulanteously for at least 2 Row periods ($\mathbf{T_{row}}$)

(see "Frame Rate and Integration Time Control" on page 13)

where $\mathbf{T_{row} = (vcw_d + shs_d + shr_d + 19)}$

To accomplish this - ensure that the Integration time ($\mathbf{cint_d}$) greater than 2 Row periods ($\mathbf{T_{row}}$) larger than the active Window of Interest Row depth.

Min. Integration time = $\mathbf{T_{intmin}=(cint_{min}+1)*T_{row}}$

$\mathbf{cint_{min}=wrd_d+x}$ **where x > 2**

where $\mathbf{wrd_d}$ is the Window Of Interest Row depth.

$\mathbf{T_{strobe1}= T_{row}}$

$\mathbf{T_{strobe2}= T_{intmin} - (wrd_d+1)*T_{row}}$

EXAMPLE: Below you will find an example of how to ensure that the strobe signal will fire and to determine the length of the STROBE signal in default mode:

(Refer to Figure 16, on page 24 for timing analysis)

Goal (For example purpose):

Strobe Signal that lasts for at least 250us, which is the length of a typical strobe/flash event.

Assumptions:

1) Active Window of Interest = 1280 x 1024

ie. $\mathbf{(wcw_d)}$=1279

$\mathbf{(wrd_d)}$=1023

2) Virtual Column Width ($\mathbf{vcw_d}$)= 1290

3) Virtual Row Depth ($\mathbf{vrd_d}$) = 1034

4) Sample & hold time ($\mathbf{shs_d}$) = 10

5) Sample & hold time ($\mathbf{shr_d}$) = 10

6) MCLK = 13 Mhz

Variables:

Integration Time ($\mathbf{cint_{min}}$) is the main variable used to control the time of the Strobe signals.

$\mathbf{T_{intmin}=(cint_{min}+1)*T_{row}}$

Calculations:

Row Time =Trow = (vcwd + shsd + shrd + 19)

= (1290 + 10 + 10 + 19) / 13.5e6

= 98.44µs

$\mathbf{T_{intmin}=(cint_{min}+1)*T_{row}}$

$\mathbf{cint_{min}=wrd_d+x}$ **where x > 2**

Let $\mathbf{cint_{min}= wrd_d+x}$ **where x > 2**

= 1023 + 4 = 1029 **where x=4**

Therefore,

$\mathbf{T_{intmin}}$= 101.39

$\mathbf{T_{strobe1}}$= 98.44µs

$\mathbf{T_{strobe2}= T_{intmin} - (wrd_d+2)*T_{row}}$

= 3 * $\mathbf{T_{row}}$

= 295us

Results:

Signal	Value
$\mathbf{T_{row}}$	98us
$\mathbf{T_{int}}$	101ms
$\mathbf{T_{strobe1}}$	98us
$\mathbf{T_{strobe2}}$	295us
$\mathbf{T_{frame}}$	202ms

NOTE!! Refer to Figure 16, on page 24 for timing analysis

10.0 I²C Serial Interface

The I²C is an industry standard which is also compatible with the Motorola bus (called M-Bus) that is available on many microprocessor products. The I²C contains a serial two-wire half-duplex interface that features bidirectional operation, master or slave modes, and multimaster environment support. The clock frequency on the system is governed by the slowest device on the board. The SDATA and SCLK are the bidirectional data and clock pins, respectively. These pins are open drain and will require a pull-up resistor to VDD of 1.5 kΩ to 10 kΩ (see page 66).

The I²C is used to write the required user system data into the Program Control Registers in the MCM20027. The I²C bus can also read the data in the Program Control Register for verification or test considerations. The MCM20027 is a slave only device that supports a maximum clock rate (SCLK) of 100 kHz while reading or writing only one register address per I²C start/stop cycle. The following sections will be limited to the methods for writing and reading data into the MCM20027 register.

For a complete reference to I²C, see “The I²C Bus from Theory to Practice” by Dominique Paret and Carll-Fenger, published by John Wiley & Sons, ISBN 0471962686.

10.1 MCM20027 I²C Bus Protocol

The MCM20027 uses the I²C bus to write or read one register byte per start/stop I²C cycle as shown in Figure 17 and Figure 18. These figures will be used to describe the various parts of the I²C protocol communications as it applies to the MCM20027.

MCM20027 I²C bus communication is basically composed of following parts: START signal, MCM20027 slave address (0110011_b) transmission followed by a R/$\overline{W}$ bit, an acknowledgment signal from the slave, 8 bit data transfer followed by another acknowledgment signal, STOP signal, Repeated START signal, and clock synchronization.

10.2 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCLK and SDATA lines are at logical “1”), a master may initiate communication by sending a START signal. As shown in Figure 17, a START signal is defined as a high-to-low transition of SDATA while SCLK is high. This signal denotes the beginning of a new data transfer and wakes up all the slaves on the bus.

10.3 Slave Address Transmission

The first byte of a data transfer, immediately after the START signal, is the slave address transmitted by the master. This is a 7-bit calling address followed by a R/$\overline{W}$ bit. The seven-bit address for the MCM20027, starting with the MSB (AD7) is 0110011_b. The transmitted calling address on the SDATA line may only be changed while SCLK is low as shown in Figure 17. The data on the SDATA line is valid on the High to Low signal transition on the SCLK line. The R/W bit following the 7-bit tells the slave the desired direction of data transfer:

- 1 = Read transfer, the slave transitions to a slave transmitter and sends the data to the master
- 0 = Write transfer, the master transmits data to the slave

10.4 Acknowledgment

Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDATA line low at the 9th clock (see Figure 17). If a transmitted slave address is acknowledged, successful slave addressing is said to have been achieved. No two slaves in the system may have the same address. The MCM20027 is configured to be a slave only.

10.5 Data Transfer

Once successful slave addressing is achieved, data transfer can proceed between the master and the selected slave in a direction specified by the R/W bit sent by the calling master. Note that for the first byte after a start signal (in Figure 17 and Figure 18), the R/W bit is always a “0” designating a write transfer. This is required since the next data transfer will contain the register address to be read or written.

All transfers that come after a calling address cycle are referred to as data transfers, even if they carry sub-address information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCLK is low and must be held stable while SCLK is high as shown in Figure 17. There is one clock pulse on SCLK for each data bit, the MSB being transferred first.

Each data byte has to be followed by an acknowledge bit, which is signalled from the receiving device by pulling the SDATA low at the ninth clock. So one complete data byte transfer needs nine clock pulses. If the slave receiver does not acknowledge the master, the SDATA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling.

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDATA line for the master to generate STOP or START signal.

10.6 Stop Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called a Repeated START. A STOP signal is defined as a low-to-high transition of SDATA while SCLK is at logical “1” (see Figure 17).

The master can generate a STOP even if the slave has generated an acknowledge bit at which point the slave must release the bus.

10.7 Repeated START Signal

A Repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in a different mode (transmit/receive mode) without releasing the bus.

As shown in Figure 18, a Repeated START signal is being used during the read cycle and to redirect the data transfer from a write cycle (master transmits the register address to the slave) to a read cycle (slave transmits the data from the designated register to the slave).

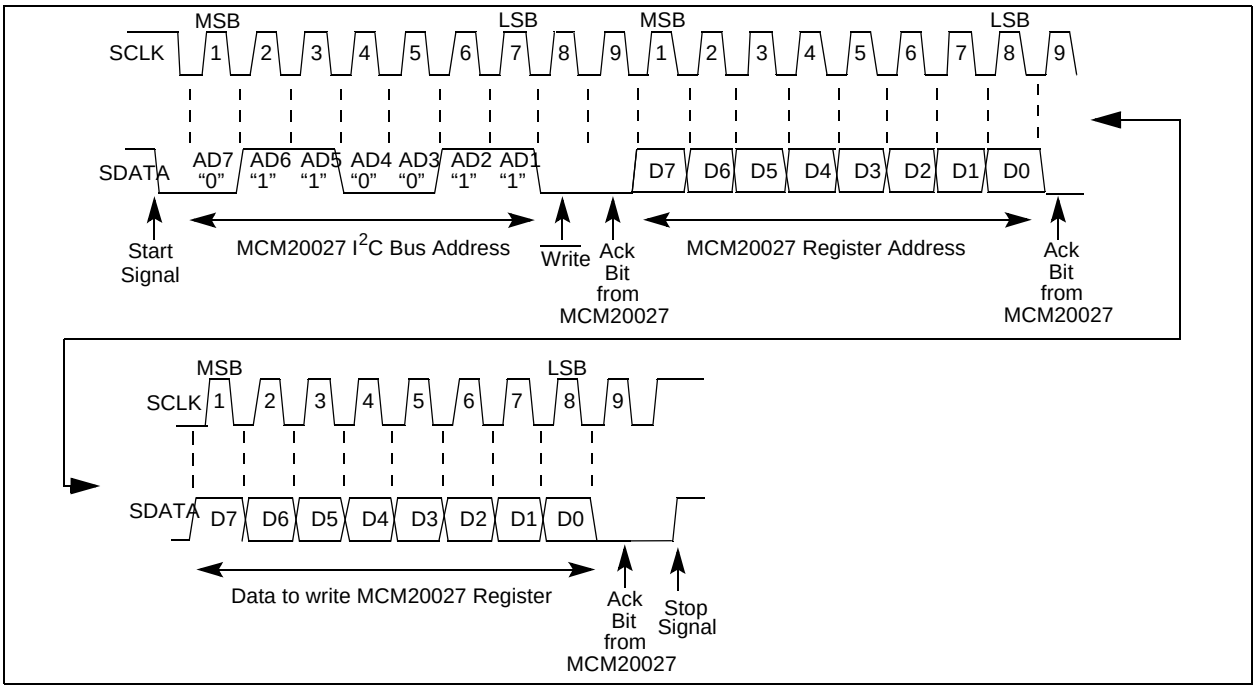


Figure 17. WRITE Cycle using I2C Bus

10.8 I2C Bus Clocking and Synchronization

Open drain outputs are used on the SCLK outputs of all master and slave devices so that the clock can be synchronized and stretched using wire-AND logic. This means that the slowest device will keep the bus from going faster than it is capable of receiving or transmitting data.

After the master has driven SCLK from High to Low, all the slaves drive SCLK Low for the required period that is needed by each slave device and then releases the SCLK bus. If the slave SCLK Low period is greater than the master SCLK Low period, the resulting SCLK bus signal Low period is stretched. Therefore, synchronized clocking occurs since the SCLK is held low by the device with the longest Low period. Also, this method can be used by the slaves to slow down the bit rate of a transfer. The master controls the length of time that the SCLK line is in the High state. The data on the SDATline is valid when the master switches the SCLK line from a High to a Low.

Slave devices may hold the SCLK low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCLK line.

10.9 Register Write

Writing the MCM20027 registers is accomplished with the following I2C transactions (see Figure 17):

- Master transmits a START
- Master transmits the MCM20027 Slave Calling Address with “WRITE” indicated (BYTE=66_h, 102_d, 01100110_b)
- MCM20027 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- Master transmits the MCM20027 Register Address
- MCM20027 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the Register Address
- Master transmits the data to be written into the register at the previously received Register Address
- MCM20027 slave sends acknowledgment by forcing the SDATA Low during the 9th clock after receiving the data to be written into the Register Address
- Master transmits STOP to end the write cycle

10.10 Register Read

Reading the MCM20027 registers is accomplished with the following I2C transactions (see Figure 18):

- Master transmits a START
- Master transmits the MCM20027 Slave Calling Address with “WRITE” indicated (BYTE=66_h, 102_d, 01100110_b)
- MCM20027 slave sends acknowledgment by forcing the SData Low during the 9th clock, if the Calling Address was received
- Master transmits the MCM20027 Register Address
- MCM20027 slave sends acknowledgment by forcing the SData Low during the 9th clock after receiving the Register Address
- Master transmits a Repeated START
- Master transmits the MCM20027 Slave Calling Address with “READ” indicated (BYTE = $67_{h,}$ 103_d, 01100111_b)
- MCM20027 slave sends acknowledgment by forcing the SDATA Low during the 9th clock, if the Calling Address was received
- At this point, the MCM20027 transitions from a “Slave-Receiver” to a “Slave-Transmitter”
- MCM20027 sends the SCLK and the Register Data contained in the Register Address that was previously received from the master; MCM20027 transitions to slave-receiver
- Master does not send an acknowledgment (NAK)
- Master transmits STOP to end the read cycle

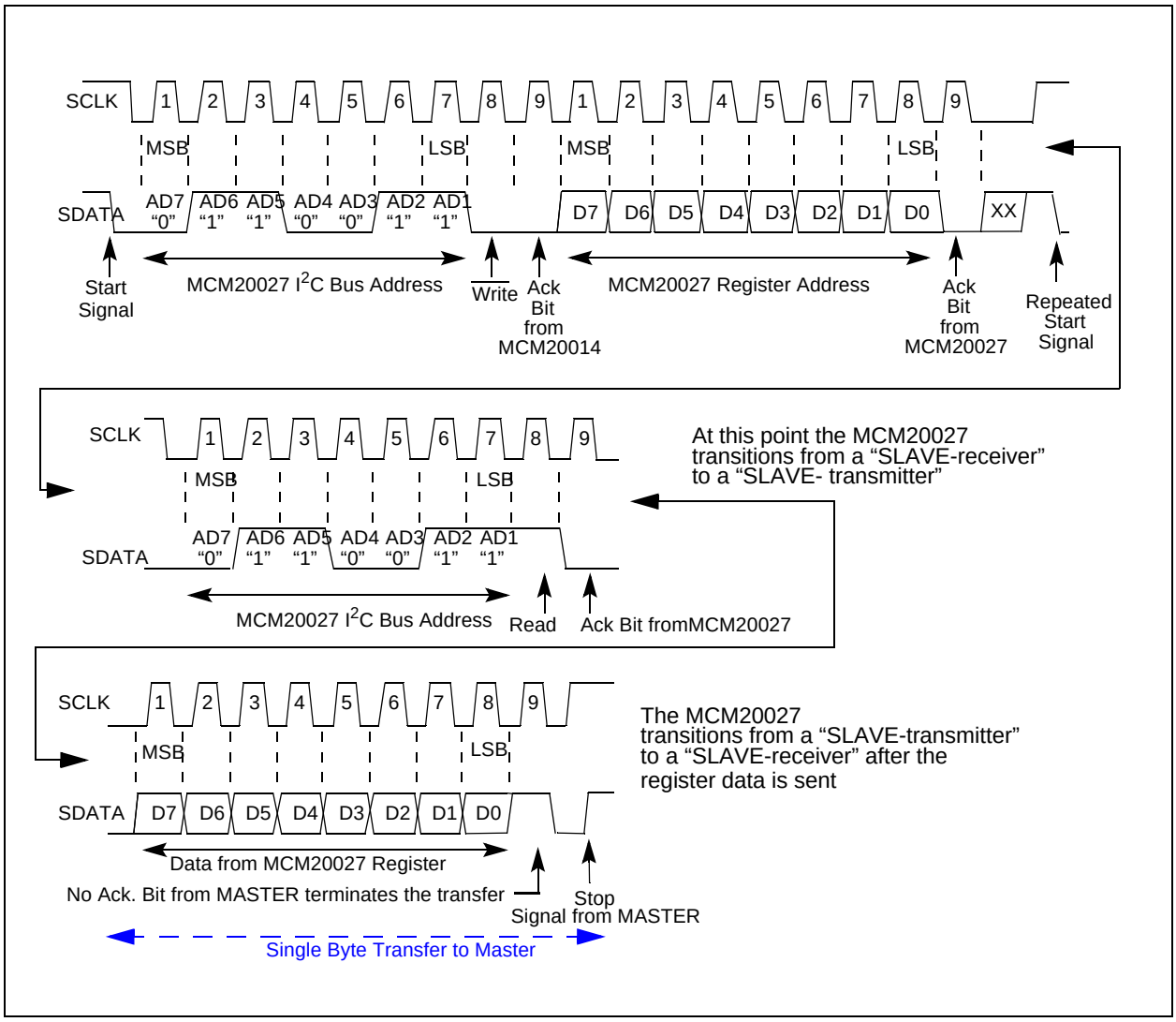


Figure 18. READ Cycle using I²C Bus

I²C SERIAL INTERFACE[6] TIMING SPECIFICATIONS (see Figure 19)				
Symbol	**Characteristic**	**Min**	**Max**	**Unit**
f_{max}	SCLK maximum frequency	50	400	KHz
M1	Start condition SCLK hold time	4	-	T_{MCLK}[7]
M2	SCLK low period	8	-	T_{MCLK}
M3	SCLK/SDATA rise time [from V_{IL} = (0.2)*VDD to V_{IH} = (.8)*VDD]	-	.3	µs[8]
M4	SDATA hold time	4	-	T_{MCLK}[7]
M5	SCLK/SDATA fall time (from Vh = 2.4V to Vl = 0.5V)	-	.3	µs[8]
M6	SCLK high period	4	-	T_{MCLK}
M7	SDATA setup time	4	-	T_{MCLK}[7]
M8	Start / Repeated Start condition SCLK setup time	4	-	T_{MCLK}
M9	Stop condition SCLK setup time	4	-	T_{MCLK}
C_I	Capacitive for each I/O pin	-	10	pF
Cbus	Capacitive bus load for SCLK and SDATA	-	200	pF
Rp	Pull-up Resistor on SCLK and SDATA	1.5	10	kΩ[9]

[6] I²C is a proprietary Phillips interface bus
[7] The unit T_{MCLK} is the period of the input master clock; The frequency of MCLK is assumed 13.5 MHz
[8] The capacitive load is 200 pF
[9] A pull-up resistor to VDD is required on each of the SCLK and SDATA lines; for a maximum bus capacitive load of 200 pf, the minimum value of Rp should be selected in order to meet specifications

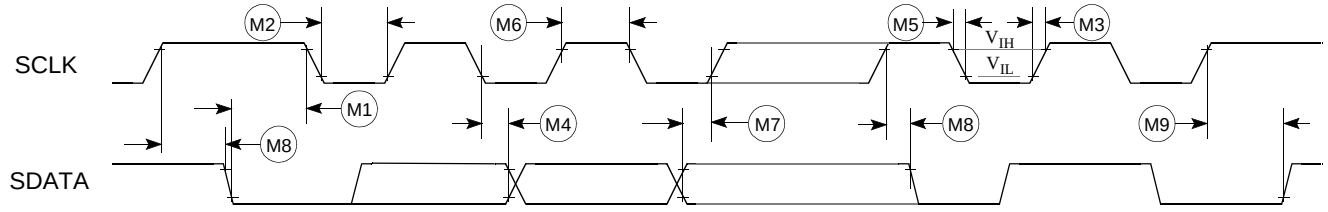


Figure 19. I²C SERIAL INTERFACE[6] TIMING SPECIFICATIONS

11.0 Suggested Software Register Programming Reference

There are number of registers whose default values we have been changed to make the sensor operational with a Digital Still Camera. The registers, there suggested new values (changes) and reason for there change are detailed in Suggested Register Default Value Changes, (Table 5), on page 31

NOTE!! These are only suggested value changes. Depending on the application, there might exist more or less registers whose default values require modifications.

Register No	Register Name	Default Values	New Values	Comment
$0C_h$	Power Configuration Register; Table 19	00_h	08_h	Switching External Resistor On for Lower active power consumption
22_h	PGA Gain Mode; Table 25	00_h	06_h	White Balance switched from Raw to Linear gain mode . Exposure Gain switched from Raw to Linear 2 gain mode
23_h	Global DOVA Register; Table 28	00_h	27_h	Negative Offset for Analog Signal Processing chain
42_h	Sync and Strobe Control register; Table 31	02_h	00_h	Necessary for switch to SFRS capture mode in addition to Capture Mode Control Register
56_h	SOF & VCLK Signal Length Control Register; Table 48	$0E_h$	09_h	new SOF = 64 MCLKs new VCLK = 8 MCLKs
$5F_h$	Internal Timing Control Register 1 (shs time definition); Table 50	$0A_h$	00_h	new shs=64 MCLKs increase sample time to sweep all available charge from pixel
60_h	Internal Timing Control Register 2 (shr time definition); Table 51	$0A_h$	00_h	new shr=64 MCLKs increased reset timesweep all available charge from pixel

Table 5. Suggested Register Default Value Changes

12.0 MCM20027 Utility Programming Registers

12.1 Register Reference Map

The I^2C addressing is broken up into groups of 16 and assigned to a specific digital block. The designated block is responsible for driving the internal control bus, when the assigned range of addresses are present on the internal address bus. The grouping designation and assigned range are listed in Table 6. Each block contains registers which are loaded and read by the digital and analog blocks to provide configuration control via the I^2C serial interface.

Table 7 contains all the I^2C address assignments. The table includes a column indicating whether the register values are shadowed with respect to the sensor interface. If the register is shadowed, the sensor interface will only be updated upon frame boundaries, thereby eliminating intraframe artifacts resulting from register changes.

Address Range	Block Name
00_h - $2F_h$	Analog Register Interface
40_h - $7F_h$	Sensor Interface
80_h - BF_h	Column Offset coeff.

Table 6. I^2C Address Range Assignments

Hex Address	Register Function	Default	Ref. Table	Shadowed?
00_h	DPGA Color 1 Gain Register (Green of Green-Red Row)	$0E_h$	Table 8, page 35	Yes
01_h	DPGA Color 2 Gain Register (Red)	$0E_h$	Table 9, page 35	Yes
02_h	DPGA Color 3 Gain Register (Blue)	$0E_h$	Table 10, page 36	Yes
03_h	DPGA Color 4 Gain Register (Green of Blue-Green Row)	$0E_h$	Table 11, page 36	Yes
04_h	*Unused*			
05_h	Color Tile Configuration Register	05_h	Table 12, page 37	No
06_h	Color Tile Row 1 Definition Register	44_h	Table 13, page 38	No
07_h	Color Tile Row 2 Definition Register	EE_h	Table 14, page 38	No
08_h	Color Tile Row 3 Definition Register	00_h	Table 15, page 39	No
09_h	Color Tile Row 4 Definition Register	00_h	Table 16, page 39	No
$0A_h$	Negative Voltage Reference Code Register	76_h	Table 17, page 40	No
$0B_h$	Positive Voltage Reference Code Register	80_h	Table 18, page 40	No
$0C_h$	Power Configuration Register	00_h	Table 19, page 41	No
$0D_h$	Factory Use Only	*FUO*	FUO	*FUO*
$0E_h$	Reset Control Register	00_h	Table 20, page 42	No
$0F_h$	Device Identification (read only)	50_h		No

Table 7. I^2C Address Assignments

Hex Address	Register Function	Default	Ref. Table	Shadowed?
10_h	Exposure PGA Global Gain Register A	$0E_h$	Table 23, page 44	Yes
11_h	*Unused*			
12h	Tristate Control Register; Table 21	03_h	Table 21, page 42	
13h	Programable Bias Generator Control register	00_h	Table 22, page 43	
14-1F	*Unused*			
20_h	Column DOVA DC Register	00_h	Table 26, page 46	No
21_h	Exposure PGA Global Gain Register B	$0E_h$	Table 24, page 45	Yes
22_h	PGA Gain Mode	00_h	Table 25, page 45	No
23_h	Global DOVA Register	00_h	Table 28, page 47	No
24 - $3F_h$	*Unused*			
40_h	Capture Mode Control Register	$2A_h$	Table 29, page 48	Yes
41_h	Sub-sample Control Register	10_h	Table 30, page 49	Yes
42_h	Sync and Strobe Control register	02_h	Table 31, page 50	Yes
43_h - 44_h	*Unused*			
45_h	WOI Row Pointer MSB Register	00_h	Table 32, page 51	Yes
46_h	WOI Row Pointer LSB Register	10_h	Table 33, page 51	Yes
47_h	WOI Row Depth MSB Register	03_h	Table 34, page 51	Yes
48_h	WOI Row Depth LSB Register	FF_h	Table 35, page 52	Yes
49_h	WOI Column Pointer MSB Register	00_h	Table 36, page 52	Yes
$4A_h$	WOI Column Pointer LSB Register	08_h	Table 37, page 53	Yes
$4B_h$	WOI Column Width MSB Register	04_h	Table 38, page 53	Yes
$4C_h$	WOI Column Width LSB Register	FF_h	Table 39, page 53	Yes
$4D_h$	Factory Use Only			
$4E_h$	Integration Time MSB Register	04_h	Table 40, page 54	Yes
$4F_h$	Integration Time LSB Register	FF_h	Table 41, page 55	Yes
50_h	Virtual Frame Row Depth MSB Register	04_h	Table 42, page 55	Yes
51_h	Virtual Frame Row Depth LSB Register	27_h	Table 43, page 55	Yes

Table 7. I^2C Address Assignments (Continued)

Hex Address	Register Function	Default	Ref. Table	Shadowed?
52_h	Virtual Frame Column Width MSB Register	05_h	Table 44, page 56	Yes
53_h	Virtual Frame Column Width LSB Register	13_h	Table 45, page 56	Yes
54_h	SOF Delay Register	$4C_h$	Table 46, page 57	No
55_h	VCLK Delay Register	02_h	Table 47, page 57	No
56_h	SOF & VCLK Signal Length Control Register	$0E_h$	Table 47, page 57	No
57_h	Greycode and Readout Control Register	04_h	Table 49, page 58	No
58_h - $5E_h$	*Unused*			
$5F_h$	Internal Timing Control Register 1 (shs time definition)	$0A_h$	Table 50, page 59	Yes
60_h	Internal Timing Control Register 2 (shr time definition)	$0A_h$	Table 51, page 60	Yes
61_h-*63_h*	*Factory Use Only*			
64_h	HCLK Delay Register	$5C_h$	Table 52, page 60	Yes
65_h	Pixel Data Stream Signal Control Register	00_h	Table 53, page 62	
66_h	*Factory Use Only*			
67_h	FRC Definition Register	24_h	Table 54, page 63	
68_h	*Factory Use Only*			
69_h - $7F_h$	*Unused*			
80-BF	Mod64 Column Offset registers	00_h	Table 27, page 47	
$C0_h$ -FF $_h$	*Unused*			

Table 7. I^2C Address Assignments (Continued)

13.0 Detailed Register Block Assignments

This section describes in further detail the functional operation of the various MCM20027 programmable registers. The registers are subdivided into various blocks for ease of addressability and use (see Table 6).

In each table where a suffix code is used; h = hex, b = binary, and d = decimal.

13.1 Analog Register Interface Block

The address range for this block is 00_h to BF_h.

13.1.1 Analog Color Configuration

The four Color Gain Registers, Color Tile Configuration Register, and four Color Tile Row definitions define how white balance is achieved on the device. Six-bit gain codes can be selected for four separate colors: Table 8, Table 9, Table 10, and Table 11. Gain for each individual color register is programmable given the gain function defined in the table. The gain function used depends on what Gain mode (White balance gain mode) the sensor is set (PGA Gain Mode; Table 25).The user programs these registers to account for changing light conditions to assure a white balanced output. The default value in each register is provides for a unity gain. In addition, the default CFA pattern color is listed in the title of each register.

Address 00_h	**DPGA Color 1 Gain Code Green of Green-Red Row**						**Default $0E_h$**
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg1[5]	cg1[4]	cg1[3]	cg1[2]	cg1[1]	cg1[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Gain	PGA Gain Mode Raw Gain Mode [$cg1_d$= 0-32_d] ---> Gain = 0.6956 + (0.02174* $cg1_d$) Raw Gain Mode [$cg1_d$= 33-63_d] --> Gain = 1.391+ (0.0434* ($cg1_d$-32) (Range 0.696 - 2.736) Linear Gain Mode -----> Gain = 0.6956 +(0.0434 x $cg1_d$) (Range 0.696 - 2.736)					001110_b

Table 8. DPGA Color 1 Gain Register

Address 01_h	**DPGA Color 2 Gain Code Red**						**Default $0E_h$**
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg2[5]	cg2[4]	cg2[3]	cg2[2]	cg2[1]	cg2[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx

Table 9. DPGA Color 2 Gain Register

Address 01_h	**DPGA Color 2 Gain Code Red**						**Default $0E_h$**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**cg2[5]**	**cg2[4]**	**cg2[3]**	**cg2[2]**	**cg2[1]**	**cg2[0]**
5 - 0	Gain	PGA Gain Mode Raw Gain Mode [$cg2_d$= 0-32_d] ---> Gain = 0.6956 + (0.02174* $cg2_d$) Raw Gain Mode [$cg2_d$= 33-63_d] --> Gain = 1.391+ (0.0434* ($cg2_d$-32) (Range 0.696 - 2.736) Linear Gain Mode -----> Gain = 0.6956 +(0.0434 x $cg2_d$) (Range 0.696 - 2.736)					001110_b

Table 9. DPGA Color 2 Gain Register

Address 02_h	**DPGA Color 3 Gain Code Blue**						**Default $0E_h$**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**cg3[5]**	**cg3[4]**	**cg3[3]**	**cg3[2]**	**cg3[1]**	**cg3[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Gain	PGA Gain Mode Raw Gain Mode [$cg3_d$= 0-32_d] ---> Gain = 0.6956 + (0.02174* $cg3_d$) Raw Gain Mode [$cg3_d$= 33-63_d] --> Gain = 1.391+ (0.0434* ($cg3_d$-32) (Range 0.696 - 2.736) Linear Gain Mode -----> Gain = 0.6956 +(0.0434 x $cg3_d$) (Range 0.696 - 2.736)					001110_b

Table 10. DPGA Color 3 Gain Register

Address 03_h	**DPGA Color 4 Gain Code Green of Blue-Green Row**						**Default $0E_h$**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**cg4[5]**	**cg4[4]**	**cg4[3]**	**cg4[2]**	**cg4[1]**	**cg4[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx

Table 11. DPGA Color 4 Gain Register

Address 03_h	DPGA Color 4 Gain Code Green of Blue-Green Row						Default $0E_h$
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cg4[5]	cg4[4]	cg4[3]	cg4[2]	cg4[1]	cg4[0]
5 - 0	Gain	PGA Gain Mode Raw Gain Mode [$cg4_d$= 0-32_d] ---> Gain = 0.6956 + (0.02174* $cg4_d$) Raw Gain Mode [$cg4_d$= 33-63_d] --> Gain = 1.391+ (0.0434* ($cg4_d$-32) (Range 0.696 - 2.736) Linear Gain Mode -----> Gain = 0.6956 +(0.0434 x $cg4_d$) (Range 0.696 - 2.736)					001110_b

Table 11. DPGA Color 4 Gain Register

The Color Tile Configuration Register; Table 12, defines the maximum number of lines and the maximum number of colors per line. A maximum of four row and four column definitions are permitted. The Color Tile Configuration Register defaults to two lines and two colors per line. The user should leave this register in default unless a unique CFA option has been ordered.

This register can be configured to any pattern combination of 1, 2, or 4 rows and 1, 2, or 4 columns.

Address 05_h	Color Tile Configuration						Default 05_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	nc[1]	nc[0]	nr[1]	nr[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 4	Unused	Unused					xxxx
3 - 2	Columns	00_b = 1 Column in tile. 01_b = 2 Columns in tile. $1x_b$ = 4 Columns in tile.					01_b
1 - 0	Rows	00_b = 1 Row in tile. 01_b = 2 Rows in tile. $1x_b$ = 4 Rows in tile.					01_b

Table 12. Color Tile Configuration Register

The Color Tile Row Definition registers; Table 13, Table 14, Table 15, and Table 16 define the sequence of colors for each respective line. Each byte wide line definition allows a maximum of four unique color definitions using 2 bits per color in a given line. Gain programming for each color was described earlier in this section. The default line definitions are colors 00_b, 01_b, 00_b, 01_b for row 1 and 10_b, 11_b, 10_b, 11_b for row 2 which supports a Bayer pattern as defined in section 2.2. The user should leave these registers in default unless a unique CFA option has been ordered.

For the default Bayer configuration of the color filter array; Figure 4, the Color Gain Register addresses are as follows: Reg (01_h): green pixel of a green-red row; Reg (00_h): red pixel; Reg (03_h): blue pixel; and Reg (02_h):green pixel of a blue-green row. The predefined

gain values programmed in the respective registers are applied to pixel outputs as they are being read.

Address 06_h	**Color Tile Row 1 Definition Green - Red Row**						**Default 44_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
r1c4[1]	**r1c4[0]**	**r1c3[1]**	**r1c3[0]**	**r1c2[1]**	**r1c2[0]**	**r1c1[1]**	**r1c1[0]**

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Color 4	Fourth Color in Row 1(Green)	01_b
5 - 4	Color 3	Third Color in Row 1 (Red)	00_b
3 - 2	Color 2	Second Color in Row 1 (Green)	01_b
1 - 0	Color 1	First Color in Row 1 (Red)	00_b

Table 13. Color Tile Row 1 Definition Register

Address 07_h	**Color Tile Row 2 Definition Blue - Green Row**						**Default EE_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
r2c4[1]	**r2c4[0]**	**r2c3[1]**	**r2c3[0]**	**r2c2[1]**	**r2c2[0]**	**r2c1[1]**	**r2c1[0]**

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Color 4	Fourth Color in Row 2 (Blue)	11_b
5 - 4	Color 3	Third Color in Row 2 (Green)	10_b
3 - 2	Color 2	Second Color in Row 2 (Blue)	11_b
1 - 0	Color 1	First Color in Row 2 (Green)	10_b

Table 14. Color Tile Row 2 Definition Register

Address 08_h	Color Tile Row 3 Definition Unused						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
r3c4[1]	r3c4[0]	r3c3[1]	r3c3[0]	r3c2[1]	r3c2[0]	r3c1[1]	r3c1[0]

Bit Number	Function	Description	Reset State
7 - 6	Color 4	Fourth Color in Row 3	00_b
5 - 4	Color 3	Third Color in Row 3	00_b
3 - 2	Color 2	Second Color in Row 3	00_b
1 - 0	Color 1	First Color in Row 3	00_b

Table 15. Color Tile Row 3 Definition Register

Address 09_h	Color Tile Row 4 Definition Unused						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
r4c4[1]	r4c4[0]	r4c3[1]	r4c3[0]	r4c2[1]	r4c2[0]	r4c1[1]	r4c1[0]

Bit Number	Function	Description	Reset State
7 - 6	Color 4	Fourth Color in Row 4	00_b
5 - 4	Color 3	Third Color in Row 4	00_b
3 - 2	Color 2	Second Color in Row 4	00_b
1 - 0	Color 1	First Color in Row 4	00_b

Table 16. Color Tile Row 4 Definition Register

13.1.2 Reference Voltage Adjust Registers

The analog register block allows programming the input voltage range of the analog to digital converter to match the saturation voltage of the pixel array. The voltage reference generator can be programmed via two registers; **nrv** (0 to 1.25V) Table 17, **prv** (2.5V to 1.25V) Table 18, in 5mV steps. A 00_h value in the **prv** register represents a reference output voltage of 2.5V. A 00_h value in the **nrv** register represents output voltage of 0V. The default settings for the two registers produce a 1.9V reference on **prv** and 0.6V on **nrv** outputs. When adjusting

these values, the user should keep the voltage range centered around 1.25V.

Address $0A_h$	**Voltage Reference "Negative" Code**						**Default 76_h**
msb (7)	6	5	4	3	2	1	lsb (0)
nrv[7]	**nrv[6]**	**nrv[5]**	**nrv[4]**	**nrv[3]**	**nrv[2]**	**nrv[1]**	**nrv[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Reference	Voltage = 0.0 + (5mV * nrc_d)					01110110_b (0.6V)

Table 17. Negative Voltage Reference Code Register

Address $0B_h$	**Voltage Reference "Positive" Code**						**Default 80_h**
msb (7)	6	5	4	3	2	1	lsb (0)
prv[7]	**prv[6]**	**prv[5]**	**prv[4]**	**prv[3]**	**prv[2]**	**prv[1]**	**prv[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Reference	Voltage = 2.5 - (5mV * prv_d)					10000000_b (1.9V)

Table 18. Positive Voltage Reference Code Register

13.1.3 Analog Control Registers

The Analog Register Block also contains a Power Configuration Register; Table 19, and a Reset Control Register; Table 20.

The Power Configuration Register controls the internal analog functionality that directly effect power consumption of the device. An external precision resistor pin is available on the MCM20027 that may be used to more accurately regulate the internal current sources. This serves to minimize variations in power consumption that are caused by variations in internal resistor values as well as offer a method to reduce the power consumption of the device. The default for this control uses the internally provided resistor which is nominally 12.5kΩ. This feature is enabled by setting the **res** bit of the Power Configuration Register and placing a resistor between the pin; EXTRES, and ground. Figure 11 depicts the power savings that can be achieved with an external resistor at a specific clock rate. Power is further reduced at lower clock rates.

The **pbg** bit of the Power Configuration Register; Table 19, is used to enable/disable the "Programmable Bias Generator". When this bit is enabled, the user can vary the power consumption of the White Balance PGA (PGAWB), Exposure gain PGA A (PGAEXPa), Exposure gain PGA B (PGEXPb), Frame Rate Clamp (FRC), Column Offset DOVA (COL_DOVA), Global offset DOVA (DOVE) and/or the Analog to Digital converter (A2D) between half an full current (power) consumption. in the Programable Bias Generator Control register; Table 22.

When this bit is disabled, it will use the power configured by the internal or external resistor (bit 3).

The MCM20027 is put into a standby mode via the I^2C interface by setting the **sby** bit of the Power Configuration Register.

Address $0C_h$	**Power Configuration**						**Default 00_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**x**	**pbg**	**res**	**ssc**	**sc**	**sby**

Bit Number	**Function**	**Description**	**Reset State**
7-5	Unused	Unused	x
4	Prog Bias Gen	0_b = Prog Bias Gen Disabled 1_b = Prog Bias Gen Enabled	0
3	Int/Ext Resistor	0_b = Internal Resistor 1_b = External Resistor	0_b
2	Select Software Clamp	0_b = Select internal Clamp 1_b = Select software Clamp	0_b
1	Software Clamp	0_b = Clamp Off 1_b = Clamp On (if ssc = 1)	0_b
0	Software Standby	0_b = Soft Standby inactive 1_b = Soft Standby active	0_b

Table 19. Power Configuration Register

Additional control of the MCM20027 can be had using the Reset Control Register; Reset Control Register; Table 20.

Setting the **sir** bit of this register will reset all the non programmable Sensor interface registers to a known reset state.

Setting the **par** bit of this register will reset all the Sensors non programmable Post ADC registers to a known reset state.

Setting the **asp** bit of this register will reset all the sensors registers in the ASP processing chain to a known reset state.

Setting the **ssr** bit of this register will reset all the non-user programmable registers to a known reset state. This is useful in situations when control of the MCM20027 has been lost due to system interrupts and the device needs only to be restarted using the earlier user programmed values.

Setting the **sit** bit allows the user to completely reset the MCM20027 to the default state via the serial control Interface. For both reset bits, **ssr** and **sit**, the user must return those bits to 0 to enable continued operation

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Address $0E_h$	Reset Control						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	asr	par	sir	ssr	sit

Bit Number	Function	Description	Reset State
7 - 5	Unused	Unused	xxx
4	ASP (A2D) Reset	0_b = Normal Mode 1_b = Reset registers in the A2D to 0	0_b
3	Post ADC Reset	0_b = Normal Mode 1_b = Reset non-programmable Post ADC Registers to Reset state.	0_b
2	Sensor Interface Reset	0_b = Normal Mode 1_b = Reset non-programmable Sensor Interface resgisters to Reset state.	0_b
1	State Reset	0_b = Normal Mode 1_b = Reset all non-programmable registers to the Reset state	0_b
0	Soft Reset	0_b = Normal Mode 1_b = Reset all registers. (Same functions as setting the INIT pin)	0_b

Table 20. Reset Control Register

The Tristate Control Register; Table 21 is used to set signals into Tristate mode. When the **tsctl** bit is reset (i.e.. “0”) the HCLK, SOF, VCLK, SYNC and STROBE output signals are set to Tristate mode. When the **tspix** bit is reset (i.e. “0”) the pixel output data is set to Tristate mode.

Address 12_h	Tristate Control B						Default 03_h
msb (7)	6	5	4	3	2	1	lsb (0)
FUO	FUO	FUO	FUO	FUO	FUO	tsctl	tspix

Bit Number	Function	Description	Reset State
7 - 3	FUO	Factory Use Only	000000_b
1	tsctl	0 - Outputs in Tristate 1 - Outputs driving	1_b

Table 21. Tristate Control Register

Address 12_h	Tristate Control B						Default 03_h
msb (7)	6	5	4	3	2	1	lsb (0)
FUO	FUO	FUO	FUO	FUO	FUO	tsctl	tspix
0	tspix	0 - Outputs in Tristate 1 - Outputs driving					1_b

Table 21. Tristate Control Register

The Programable Bias Generator Control register; Table 22 can be used by the user to vary the power consumption of the White Balance PGA (PGAWB), Exposure gain PGA A (PGAEXPa), Exposure gain PGA B (PGEXPb), Frame Rate Clamp (FRC), Column Offset DOVA (COL_DOVA), Global offset DOVA (DOVE) and/or the Analog to Digital converter (A2D) between half an full current (power) consumption.

In order for this Register to be used, the **pbg** bit of the Power Configuration Register; Table 19 has to be enabled.

Address 13_h	Programable Bias Generator Control						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	adp	gdp	egb	ega	wbp	cdp	fcp

Bit Number	Function	Description	Reset State
7	Unused	Unused	x_b
6	A to D Converter (A2D)	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]	0_b
5	Global Dova	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]	0_b
4	PGA Exp. Gain B	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]	0_b
3	PGA Exp. Gain A	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]	0_b
2	PGA White Balance	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]	0_b
1	Col_Dova	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]	0_b

Table 22. Programable Bias Generator Control register

Address 13_h	Programable Bias Generator Control						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	adp	gdp	egb	ega	wbp	cdp	fcp
0	Frame Rate Clamp	1_b = Full Current (Power) consumption [80/100] 0_b = Half Current (Power) consumption [40/50]					0_b

Table 22. Programable Bias Generator Control register

13.2 Gain Calibration Block

The Exposure PGA Global Gain Register A; Table 23 and the Exposure PGA Global Gain Register B; Table 24, allows the user to set a global gain via two 6 bit register which are applied universally to all the pixel outputs. This enables the user to account for varying light conditions.The Gain range depends on what the Exposure Gain Mode (PGA Gain Mode; Table 25)is set. If The Exposure gain mode is set at either Raw or Linear, then Exposure PGA Global Gain Register A; Table 23 and Exposure PGA Global Gain Register B; Table 24 are both utilized. But if it is set at Linear 2 gain mode, then only Exposure PGA Global Gain Register A; Table 23 is used.

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Address 10_h	Exposure PGA Global Gain A						Default $0E_h$
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	gg1[5]	gg1[4]	gg1[3]	gg1[2]	gg1[1]	gg1[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Gain	PGA Gain Mode Raw Gain Mode [$gg1_d$= 0-32_d] ---> Gain = 0.6956 + (0.02174* $gg1_d$) Raw Gain Mode [$gg1_d$= 33-63_d] --> Gain = 1.391+ (0.0434* ($gg1_d$-32) (Range 0.696 - 2.736) Linear Gain Mode -----> Gain = 0.6956 + (0.0434 * $gg1_d$) (Range 0.696 - 2.736) Linear 2 Gain Mode ----> Gain = 0.484 +(0.12 x $gg1_d$) (Range 0.484 - 7.488)					001110

Table 23. Exposure PGA Global Gain Register A

Address 21_h	**Exposure PGA Global Gain B**						**Default $0E_h$**
msb (7)	6	5	4	3	2	1	lsb (0)
x	**x**	**gg2[5]**	**gg2[4]**	**gg2[3]**	**gg2[2]**	**gg2[1]**	**gg2[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx_b
5 - 0	Gain	PGA Gain Mode Raw Gain Mode [$gg2_d$= 0-32_d] ---> Gain = 0.6956 + (0.02174* $gg2_d$) Raw Gain Mode [$gg2_d$= 33-63_d] --> Gain = 1.391+ (0.0434* ($gg2_d$-32) (Range 0.696 - 2.736) Linear Gain Mode -----> Gain = 0.6956 + (0.0434 * $gg2_d$) (Range 0.696 - 2.736)						001110

Table 24. Exposure PGA Global Gain Register B

The PGA Gain Mode; Table 25, is the register where the PGA Gain modes for the White Balance and Exposure gains can be selected. There are two different Gain modes for White Balance and there are three different Gain modes for the Exposure gain.

White Balance Gain modes:

1) Raw gain mode - 32 steps @ 0.02174/step

- 32 steps @ 0.04340/step

2) Linear gain mode - 48 steps @ 0.04340/step

Exposure Gain Modes:

1) Raw gain mode - 32 steps @ 0.02174/step

- 32 steps @ 0.04340/step

i.e. PGA Global Gain A Register= Raw gain mode

PGA Global Gain B Register= Raw gain mode

2) Linear gain mode - 48 steps @ 0.04340/step

i.e. PGA Global Gain A Register= Linear gain mode

PGAGlobal Gain B Register= Linear gain mode

3) Linear 2 gain mode - 64 steps @ ~ 0.12/step

i.e. PGA Global Gain A Register= Linear 2 gain mode

PGA Global Gain B Register= Not used

The **wbm** bit sets the White Balance mode. While the **egm**[d] bit sets the Exposure gain mode

Address 22_h	**PGA Gain Mode**						**Default 00_h**
msb (7)	6	5	4	3	2	1	lsb (0)
x	**x**	**x**	**x**	**x**	**wbm**	**egm[1]**	**egm[0]**
Bit Number	**Function**	**Description**					**Reset State**

Table 25. PGA Gain Mode

Address 22_h	PGA Gain Mode						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	wbm	egm[1]	egm[0]
7 - 3	Unused	Unused					xxxx
2	White Balance Gain Mode	0_b = Raw gain mode 1_b = Linear gain mode					0_b
1 - 0	Exposure Gain Mode	00_b = Raw gain mode 01_b = Linear gain mode $1x_b$ = Linear 2 gain mode					00b

Table 25. PGA Gain Mode

13.3 Offset Calibration Block

Offset adjustments for the MCM20027 are done in separate sections of the ASP to facilitate FPN removal and final image black level set.

The Column DOVA DC Register; Table 26, is used to set the initial offset of the pixel output in a range that will facilitate per-column offset data generation for varying operational conditions. In most operational scenarios, this register can be left in its default state of 00_h. This is a pre-image processing gain in comparison to the Global DOVA Register which is a post image processing chain gain (pre A2D gain).

This register can also be used to apply a global offset adjust. In this case, the user must take into account the Color Gain and Global Gain registers to determine the resulting offset at the output.

Address 20_h	Column DOVA DC						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	cdd[5]	cdd[4]	cdd[3]	cdd[2]	cdd[1]	cdd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5	Sign	0_b = Positive Offset 1_b = Negative Offset					0_b
4 - 0	Column DC Offset	Offset = 2.6 * cdd_d (64 steps @ 2.6mV /Step)					00000_b

Table 26. Column DOVA DC Register

The Mod64 Column Offset registers; Table 27 are used in conjunction with the Column DOVA DC Register; Table 26 to reduce/eliminate fixed pattern noise (FPN). There are 64 registers that can be programmed with individual offset values. They will be applied to all the columns on a single image frame on a Modular 64 basis.i.e. Register 80_h Column offset will be applied to Column 0 , Register 81_h Column offset will be applied to Column 1, Register BF_h Column offset will be applied to Column 63, Register 80_h Column offset will be applied to Column 0..etc..

Address 80-BF$_h$	**Mod64 Column Offset**						**Default 00$_h$**
msb (7)	6	5	4	3	2	1	lsb (0)
x	**x**	**mdd[5]**	**mdd[4]**	**mdd[3]**	**mdd[2]**	**mdd[1]**	**mdd[0]**

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
4 - 0	Mod 64 Column DC Offset	Offset = 2.6 * mdd_d (64 steps @ 2.6mV /Step)	00000_b

Table 27. Mod64 Column Offset registers

The Global DOVA Register; Table 28 performs a final offset adjustment in analog space prior to the ADC. The 6-bit register uses its MSB to indicate positive or negative offset. Each bit value changes the offset value by 4 LSB code levels hence giving an offset range of +/-124 LSB. As an example, to program an offset of +92 LSB, the binary representation of $+23_d$ i.e. 010111_b should be loaded.

Address 23$_h$	**Global DOVA**						**Default 00$_h$**
msb (7)	6	5	4	3	2	1	lsb (0)
x	**x**	**gd[5]**	**gd[4]**	**gd[3]**	**gd[2]**	**gd[1]**	**gd[0]**

Bit Number	**Function**	**Description**	**Reset State**
7 - 6	Unused	Unused	xx
5	Sign	0_b = Positive Offset 1_b = Negative Offset	0_b
4 - 0	Offset	Offset = 12 * gd_d (64 steps @ 12mV /Step)	00000_b

Table 28. Global DOVA Register

13.4 Sensor Interface Block

13.4.1 Sensor Output Control

The sensor output control registers define how the window of interest is captured and what data is output from the MCM20027.

The Capture Mode Control Register; Table 29, defines how the data is captured and how the data is to be provided at the output..

Setting the **cms** bit will stop the current output data stream at the end of the current frame. Unsetting this bit (**cms** = 0_b) will resume the output of the frame stream. The MCM20027 is in CFRS in default. The user may use this bit to capture data in the CFRS mode and/or SFRS while using the SYNC pin. The SYNC pin triggers a single frame of data to be output from the device in the

SFRS mode. Please refer to Figure 14, on page 20 for a timing diagram of this mode.

The **sp** bit is used to define whether SOF is active high or low. SOF is active high in default.

The **ve** bit is used to determine whether VCLK is output at the beginning of all the rows including virtual frame rows or for the WOI rows only. The default is WOI only.

The **vp** bit is used to define whether VCLK is active high or low. VCLK is active high in default.

The **he** bit is used to determine whether HCLK is output continuously or for the WOI pixels only. The default is WOI only.

The **hp** bit is used to define whether HCLK is active high or low. HCLK is active high in default.

The **hm** bit is used to define HCLK is toggled or whetherwhether it is continuously output.

Address 40_h	**Capture Mode Control**						**Default $2A_h$**
msb (7)	6	5	4	3	2	1	lsb (0)
FUO	**cms**	**sp**	**ve**	**vp**	**he**	**hp**	**hm**

Bit Number	**Function**	**Description**	**Reset State**
7	FUO	Factory Use Only	0_b
6	Capture Mode	0_b = Continuos Frame Rolling Shutter 1_b = Single Frame Rolling Shutter	0_b
5	SOF Phase	1_b = SOF active high 0_b = SOF active low	1_b
4	VCLK Enable	1_b = All virtual frame rows 0_b = Window of Interest rows only	0_b
3	VCLK Phase	1_b = Active high 0_b = Active low	1_b
2	HCLK Enable	1_b = Continuous 0_b = Window of Interest Pixels only	0_b
1	HCLK Phase	1_b = Active high 0_b = Active low	1_b
0	HCLK Mode	1_b = Continuous - envelope 0_b = Toggles - like MCLK	0_b

Table 29. Capture Mode Control Register

The Sub-sample Control Register; Table 30, is used to define what pixels of the WOI are read and the method they are read.

Using the **cm** bit, the user can sample the pixel array in either monochrome or Bayer pattern color space. This means that when sampling the rows or columns, the set of pixels read will be gathered as individual pixels (monochrome) or in color tiles of pixels (Bayer pattern). The pixels will be read in monochrome mode in default.

The row sub sampling rate is defined by **rf**[1:0] while the column sub sampling rate is defined by **cf**[1:0]. The pixel array is fully sampled in default.

Address 41_h	Sub-sample Control						Default 10_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	FUO	FUO	cm	rf[1]	rf[0]	cf[1]	cf[0]

Bit Number	Function	Description	Reset State
7	Unused	Unused	x
6-5	FUO	Factory Use Only	FUO
4	Color Mode	1_b = Bayer Pattern Sampling 0_b = Monochrome Pattern Sampling	1_b
3 - 2	Row Frequency	11_b = read one row pattern, skip 7 (1/8 sampled) 10_b = read one row pattern, skip 3 (1/4 sampled) 01_b = read one row pattern, skip one (1/2 sampled) 00_b = full sampling	00_b
1 - 0	Column Frequency	11_b = read one column pattern, skip 7 (1/8 sampled) 10_b = read one column pattern, skip 3 (1/4 sampled) 01_b = read one column pattern, skip one (1/2 sampled) 00_b = full sampling	00_b

Table 30. Sub-sample Control Register

The Sync and Strobe Control register; Table 31 is used to control the sync and strobe signals.

The **sr** bit when enabled causes the SYNC signal to go high for exactly one clock cycle, and then returns to a low. It remains low until the **sr** bit is enabled again.

The **sa** bit when enabled causes the SYNC signal high until this bit is disabled. This causes continuous frame processing.

The **se** bit when enabled will allow for an external signal to drive the SYNC signal via the SYNC pin on the chip.

The **sae** bit when enabled will enable the STROBE signal to be generated automatically by the sensor.This will only work in SFRS (Single Frame Rolling Shutter). The STROBE signal is goes high when all the Rows in the Frame are integrating together.

The **saw** bit allows the user to select how long the STROBE signal is going to be on. If the bit is set to 1 (Setting 1), causes the STROBE Signal to be on from the time all the Rows are integrating to 1 Row time (T_{ROW}) before Read-Out of the first Row commences. If the bit is set to 0 (Setting 0), causes the STROBE signal to on for a duration of 1 Row time (T_{ROW}) from the time all Rows are integrating

The **sso** bit ,when enabled, forces the STROBE signal and thereby the STROBE Pin high until it is reset back to 0. When this bit is set high - the **sae** and **saw** bit settings become negligible.

NOTE! Please refer to Figure 15, on page 14 for Strobe Signal timing diagram.

Address 42_h	SYNC and STROBE Control						Default 02_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	sso	saw	sae	se	sa	sr

Bit Number	Function	Description	Reset State
7-6	Unused	Unused	xx
5	Strobe Enable	1_b = Strobe On 0_b = Disabled	0_b
4	Strobe Auto Width Definition	1_b = Maximum time (Entire time during which all active rows are inte grating) 0_b = 1 line	0_b
3	Strobe Auto Enabled	1_b = Enabled during integration 0_b = Disabled	0_b
2	Exernal SYNC Enabled	1_b = Enabled 0_b = Disabled	0_b
1	SYNC Always	1_b = Enabled 0_b = Disabled	1_b
0	SYNC Request	1_b = Enabled (Self clearing - will always read “0”) 0_b = Disabled	0_b

Table 31. Sync and Strobe Control register

13.4.2 Programmable “Window of Interest”

The WOI is defined by a set of registers that indicate the upper-left starting point for the window and another set of registers that define the size of the window. Please refer to Figure 9, on page 12 for a pictorial representation of the WOI within the active pixel array.

The WOI Row Pointer; **wrp**[10:0] (Table 32 and Table 33), and the WOI Column Pointer; **wcp**[10:0] (Table 36 and Table 37), mark the upper-left starting point for the WOI.

The WOI Row Pointer; **wrp**[10:0], has a range of 0_d to 1047_d whereas the WOI Column Pointer; **wcp**[10:0] has a usable range of 0_d to 1295_d. The pointer can be placed anywhere within the active pixel array.

The WOI Row Depth; **wrd**[10:0] (Table 32 and Table 33), and the WOI Column Depth; **wcd**[10:0] (Table 36 and Table 37), indicate the size of the WOI.

The WOI Row Depth; **wrd**[10:0], has a range of 0_d to 1047_d whereas the WOI Column Depth; **wcd**[10:0], has a range of 0_d to 1295_d.

The user should be careful to create a WOI that contains active pixels only. There is no logic in the sensor

interface to prevent the user from defining an WOI that addresses non-existent pixels.

Address 45_h	**WOI Row Pointer MSB**						**Default 00_h**
msb (7)	6	5	4	3	2	1	lsb (0)
x	**x**	**x**	**x**	**x**	**wrp[10]**	**wrp[9]**	**wrp[8]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 3	Unused	Unused					xxxxx
2 - 0	WOI Row Pointer	In conjunction with the WOI Row Pointer LSB Register (Table 33), forms the 11-bit WOI Row Pointer wrp[10:0]					000_b

Table 32. WOI Row Pointer MSB Register

Address 46_h	**WOI Row Pointer LSB**						**Default 10_h**
msb (7)	6	5	4	3	2	1	lsb (0)
wrp[7]	**wrp[6]**	**wrp[5]**	**wrp[4]**	**wrp[3]**	**wrp[2]**	**wrp[1]**	**wrp[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Row Pointer MSB Register (Table 32), forms the 11-bit WOI Row Pointer wrp[10:0]					00010000_b (row 16)

Table 33. WOI Row Pointer LSB Register

Address 47_h	**WOI Row Depth MSB**						**Default 03_h**
msb (7)	6	5	4	3	2	1	lsb (0)
x	**x**	**x**	**x**	**x**	**wrd[10]**	**wrd[9]**	**wrd[8]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 3	Unused	Unused					xxxxx

Table 34. WOI Row Depth MSB Register

Address 47_h	WOI Row Depth MSB						Default 03_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	wrd[10]	wrd[9]	wrd[8]
2-0	WOI Row Depth	In conjunction with the WOI Row Depth LSB Register (Table 35), forms the 11-bit WOI Row Depth wrd[10:0].					011_b

Table 34. WOI Row Depth MSB Register

Address 48_h	WOI Row Depth LSB						Default FF_h
msb (7)	6	5	4	3	2	1	lsb (0)
wrd[7]	wrd[6]	wrd[5]	wrd[4]	wrd[3]	wrd[2]	wrd[1]	wrd[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Row Depth MSB Register (Table 34), forms the 11-bit WOI Row Depth wrd[10:0]. Desired = $wrd_d + 1$.					11111111_b (1024 rows)

Table 35. WOI Row Depth LSB Register

Address 49_h	WOI Column Pointer MSB						Default 00_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	wcp[10]	wcp[9]	wcp[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 3	Unused	Unused					xxxxx
2 - 0	WOI Col. Pointer	In conjunction with the WOI Column Pointer LSB Register (Table 37), forms the 11-bit WOI Column Pointer wcp[10:0]					000_b

Table 36. WOI Column Pointer MSB Register

Address $4A_h$	WOI Column Pointer LSB						Default 08_h
msb (7)	6	5	4	3	2	1	lsb (0)
wcp[7]	wcp[6]	wcp5]	wcp[4]	wcp[3]	wcp[2]	wcp[1]	wcp[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Col. Pointer	In conjunction with the WOI Column Pointer MSB Register (Table 36), forms the 11-bit WOI Column Pointer wcp[10:0]					00001000_b (col. 8)

Table 37. WOI Column Pointer LSB Register

Address $4B_h$	WOI Column Width MSB						Default 04_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	x	wcw[10]	wcw[9]	wcw[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 3	Unused	Unused					xxxxx
2 - 0	WOI Col. Width	In conjunction with the WOI Column Width LSB Register (Table 39), forms the 11-bit WOI Column Width wcw[10:0].					100_b

Table 38. WOI Column Width MSB Register

Address $4C_h$	WOI Column Width LSB						Default FF_h
msb (7)	6	5	4	3	2	1	lsb (0)
wcw[7]	wcw[6]	wcw[5]	wcw[4]	wcw[3]	wcw[2]	wcw[1]	wcw[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	WOI Row Pointer	In conjunction with the WOI Column Width MSB Register (Table 38), forms the 11-bit WOI Column Width wcw[10:0]. Desired = $wcw_d + 1$.					11111111_b (1280 col.)

Table 39. WOI Column Width LSB Register

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13.4.3 Integration Time Control

The Integration Time registers; Table 41, Table 40, and Table 41, control the integration time for the pixel array. Integration time for CFRS and SFRS; **cint**[13:0], is measured in Virtual Row times. Please refer to Figure 11 for a pictorial description of the Virtual Frame and its relationship to the WOI.

NOTE!! The **upd bit** of the Integration Time MSB Register; Table 40 is used to indicate a change to **cint**[13:0]. Since multiple I2C writes may be needed to complete desired frame to frame integration time changes, the **upd** bit signals that all desired programming has been completed, and to apply these changes to the next frame captured. This prevents undesirable changes in integration time that may result from I2C writes that span the “End of Frame” boundary. This **upd** bit has to be toggled from its previous state in order for the new value of **cint**[13:0] to be accepted/updated by the sensor and take effect. i.e. If its previous state is “0”, when writing a new **cint** value, first write cint[7:0] to the Integration Time LSB Register; Table 41, then write both **cint** [13:8] and “1” to the **upd** bit to the Integration Time MSB Register; Table 40.

A virtual frame is the mechanism by which the user controls the integration time and frame time for the output data stream. By adding additional rows or columns as ‘blanking’ to the WOI to form the Virtual Frame, the user can control the amount of blanking in both horizontal and vertical space.(Table 42, “Virtual Frame Row Depth MSB Register,” on page 55 Table 43, “Virtual Frame Row Depth LSB Register,” on page 55Table 44, “Virtual Frame Column Width MSB Register,” on page 56Table 45, “Virtual Frame Column Width LSB Register,” on page 56)

The user should be careful to create a Virtual Frame that is larger than the WOI. There is no logic in the sensor interface to prevent the user from defining a Virtual Frame smaller than the WOI. Therefore, pixel data may be lost.

The Virtual Frame must be at least 1 row and 6 columns larger than the WOI.

The Virtual Frame completely defines the integration time in CFRS. Any changes to the WOI or how the WOI is sampled has no effect on integration time.

Address $4E_h$	**Integration Time MSB**						**Default 04_h**
msb (7)	6	5	4	3	2	1	lsb (0)
FUO	**upd**	**cint[13]**	**cint[12]**	**cint[11]**	**cint[10]**	**cint[9]**	**cint[8]**

Bit Number	**Function**	**Description**	**Reset State**
7	FUO	Factory Use Only	
6	Integration Time Update Switch	This bit has to change from its previous state everytime a new value is written to **Integration Time ISB and the Integration Time LSB**.	0
5 - 0	Integration Time	In conjunction with the Integration Time LSB (Table 41) Register, forms the 14-bit Integration Time cint[13:0].	000100_b

Table 40. Integration Time MSB Register

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Address $4F_h$	**Integration Time LSB**						**Default FF_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
cint[7]	**cint[6]**	**cint[5]**	**cint[4]**	**cint[3]**	**cint[2]**	**cint[1]**	**cint[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Integration Time	In conjunction with the Integration Time ISB (Table 40) Register, forms the 14-bit Integration Time cint[13:0]. Integration Time = $(cint_d + 1) * T_{row}$					11111111_b **CFRS and SFRS**: 1280 Rows)

Table 41. Integration Time LSB Register

Address 50_h	**Virtual Frame Row Depth MSB**						**Default 04_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**vrd[13]**	**vrd[12]**	**vrd[11]**	**vrd[10]**	**vrd[9]**	**vrd[8]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Virtual Row Depth	In conjunction with the CFRS and SFRS Virtual Frame Row Depth LSB (Table 43) Register, forms the 14-bit Virtual Frame Row Depth vrd[13:0].					000100_b

Table 42. Virtual Frame Row Depth MSB Register

Address 51_h	**Virtual Frame Row Depth LSB**						**Default 27_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
vrd[7]	**vrd[6]**	**vrd[5]**	**vrd[4]**	**vrd[3]**	**vrd[2]**	**vrd[1]**	**vrd[0]**
Bit Number	**Function**	**Description**					**Reset State**

Table 43. Virtual Frame Row Depth LSB Register

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Address 51_h	Virtual Frame Row Depth LSB						Default 27_h
msb (7)	6	5	4	3	2	1	lsb (0)
vrd[7]	vrd[6]	vrd[5]	vrd[4]	vrd[3]	vrd[2]	vrd[1]	vrd[0]
7 - 0	Virtual Row Depth	In conjunction with the CFRS and SFRS Virtual Frame Row Depth MSB (Table 42) Register, forms the 14-bit Virtual Frame Row Depth vrd[13:0]. WOI is always top-left justified in Virtual Frame. vrd_d minimum = wrd_d + 1						00100111_b (1064 rows)

Table 43. Virtual Frame Row Depth LSB Register

Address 52_h	Virtual Frame Column Width MSB						Default 05_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	vcw[13]	vcw[12]	vcw[11]	vcw[10]	vcw[9]	vcw[8]
Bit Number	**Function**	**Description**					**Reset State**
7 - 6	Unused	Unused					xx
5 - 0	Virtual Column Width	In conjunction with the CFRS and SFRS Virtual Frame Column Width LSB (Table 45) Register, forms the 14-bit Virtual Frame Column Width vcw[13:0].					000101_b

Table 44. Virtual Frame Column Width MSB Register

Address 53_h	Virtual Frame Column Width LSB						Default 13_h
msb (7)	6	5	4	3	2	1	lsb (0)
vcw[7]	vcw[6]	vcw[5]	vcw[4]	vcw[3]	vcw[2]	vcw[1]	vcw[0]
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	Virtual Column Width	In conjunction with the CFRS and SFRS Virtual Frame Column Width MSB (Table 44) Register, forms the 14-bit Virtual Frame Column Width vcw[13:0]. WOI is always top-left justified in Virtual Frame. vcw_d minimum = wcw_d + 11						00010011_b (1300 col.)

Table 45. Virtual Frame Column Width LSB Register

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The SOF Delay Register; Table 46 and VCLK Delay Register; Table 47 are used to determine the time (clock) delay for the start of the two signals respectively. The SOF Delay is measured as the time after the start of the change of row address (Change of row address is a parameter that cannot be easily identified by the common user). The VCLK Delay is defined as the time after the SOF signal is first initialized. The SOF & VCLK Signal Length Control Register, Table 48 , is used to define the size of the SOF and VCLK signals. In default, SOF is one row wide while VLCK is 64 MCLKs wide

Address 54_h	**SOF Delay**						**Default $4C_h$**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
sofd[7]	**sofd[6]**	**sof[d5]**	**sofd[4]**	**sofd[3]**	**sofd[2]**	**sofd[1]**	**sofd[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	SOF Delay	Delay= sofd[d] x 0.5 MCLKs (Note - Delay is relative to Internal Pixel Transfer Control)					1001100b

Table 46. SOF Delay Register

Address 55_h	**VCLK Delay**						**Default 02_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
vckd[7]	**vckd[6]**	**vckd[5]**	**vckd[4]**	**vckd[3]**	**vckd[2]**	**vckd[1]**	**vckd[0]**
Bit Number	**Function**	**Description**					**Reset State**
7 - 0	VCLK Delay	Delay = vckd[d] x 0.5 MCLKs (Note - Delay is relative to Start Of Frame {SOF} signal)					00000010_b

Table 47. VCLK Delay Register

Address 56_h	**SOF and VCLK Signal Length Control**						**Default E_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**x**	**x**	**x**	**sofc[3]**	**sofc[2]**	**vckc[1]**	**vckc[0]**
Bit Number	**Function**	**Description**					**Reset State**
3 - 2	SOF Control	sof[3:2] = 00_b = 1 MCLK Wide sof[3:2] = 01_b = 8 MCLKs Wide sof[3:2] = 10_b = 64 MCLKs Wide sof[3:2] = 11_b = Full Row Wide					11_b

Table 48. SOF & VCLK Signal Length Control Register

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Address 56_h	SOF and VCLK Signal Length Control						Default E_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	sofc[3]	sofc[2]	vckc[1]	vckc[0]
1 - 0	VCLK Control	vck[1:0] = 00_b = 1 MCLK Wide vck[1:0] = 01_b = 8 MCLKs Wide vck[1:0] = 10_b = 64 MCLKs Wide vck[1:0] = 11_b = Full Row Wide					10_b

Table 48. SOF & VCLK Signal Length Control Register

The Greycode and Readout Control Register; Table 49 allows the user to choose if the column and row addresses are to utilize Greycode address format or not. It also allows the user to select the user to select the direction of the row and column readout.

The **rrc** when enabled causes the column data to be readout in the reverse direction as compared to the normal readout direction.

The **rrr** when enabled causes the row data to be readout in the reverse direction as compared to the normal readout direction.

The **gcc** bit when enabled causes the column addresses to be Greycoded.

The **gcr** bit when enabled causes the column addresses to be Greycoded.

Address 57_h	Greycode and Readout Control						Default 04_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	gcr	gcc	rrr	rrc
Bit Number	**Function**	**Description**					**Reset State**
7-4	Unused	Unused					
3	Row Greycode Address	1_b = Greycode addressing Enabled 0_b = Binary Addressing					0_b
2	Column Greycode Address Enable	1_b = Greycode addressing Enabled 0_b = Binary Addressing					1_b

Table 49. Greycode and Readout Control Register

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Address 57_h	Greycode and Readout Control						Default 04_h
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	x	x	gcr	gcc	rrr	rrc
1	Row Read-out	1_b = Reverse Readout (Top to Bottom) 0_b = Normal Readout (Bottom to Top)					0_b
0	Column Readout	1_b = Reverse Readout (Right to Left) 0_b = Normal Readout (Left to Right					0_b

Table 49. Greycode and Readout Control Register

The Internal Timing Control Register 1 (shs time definition); Table 50 and ,Internal Timing Control Register 2 (shr time definition); Table 51 are used to define the size of internal timing pulse widths. In default, both **shs** and **shr** are 6 MCLK's wide. A maximum of 64 MCLK's can be programmed for the shs delay and another 64 MCLK's for the shr delay, for a total 0f 128 MCLK's. Note! writing 00h to either of these Registers will write a maximum timing delay of 64 MCLK's. i.e. 00 = 64 MCLK

Address $5F_h$	Internal Timing Control						Default $0A_h$
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	shs[5]	shs[4]	shs[3]	shs[2]	shs[1]	shs[0]
Bit Number	**Function**	**Description**					**Reset State**
7-6	Unused	Unused					xx
5 - 0	shs	shs[5:0] = 000000_b = 64 MCLKs Wide shs[5:0] = 000001_b = 1_d MCLKs Wide shs[5:0] = 000010_b = 2_d MCLKs Wide shs[5:0] = 000011_b = 3_d MCLKs Wide | | shs[5:0] = 111111_b = 63_d MCLKs Wide					001010b

Table 50. Internal Timing Control Register 1 (shs time definition)

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Address 60_h	Internal Timing Control						Default $0A_h$
msb (7)	6	5	4	3	2	1	lsb (0)
x	x	shr[5]	shr[4]	shr[3]	shr[2]	shr[1]	shr[0]

Bit Number	Function	Description	Reset State
7-6	Unused	Unused	xx
5 - 0	shr	shr[5:0] = 000000_b = 64 MCLKs Wide shr[5:0] = 000001_b = 1_d MCLKs Wide shr[5:0] = 000010_b = 2_d MCLKs Wide shr[5:0] = 000011_b = 3_d MCLKs Wide | | shr[5:0] = 111111_b = 63_d MCLKs Wide	001010b

Table 51. Internal Timing Control Register 2 (shr time definition)

The HCLK Delay Register; Table 52 allows the user to program the delay for the start of the HCLK signal. The delay is calculated in accordance to the result of inserting the value of the register into the following formula:

Delay = ((hckd[d]-4)x 0.5) - 16 MCLKs

Address 64_h	HCLK Control						Default $5C_h$
msb (7)	6	5	4	3	2	1	lsb (0)
x	FUO	FUO	FUO	FUO	hckd[2]	hckd[1]	hckd[0]

Bit Number	Function	Description	Reset State
7	Unused	Unused	x
6 - 3	FUO	Factory Use Only	

Table 52. HCLK Delay Register

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Address 64_h	HCLK Control						Default $5C_h$
msb (7)	6	5	4	3	2	1	lsb (0)
x	FUO	FUO	FUO	FUO	hckd[2]	hckd[1]	hckd[0]
2 - 0	HCLK Delay	Delay = ((hckd[d]-4)x 0.5) - 16 MCLKs					100_b

Table 52. HCLK Delay Register

The Pixel Data Stream Control Register allows the user to select how the output pixel data stream is encoded/formatted.

The **vcb** bit allows the user to force all the Blanking data coming out of the A2D to be 0.

The **vcg** bit allows the user to choose between encoded pixel data output stream or non-encoded pixel data output stream.

The **vcc** bit allows the user to clip the output active pixel data to lie between 001 and 3FE

The default mode (**Normal Mode)** has the SOF, HCLK, VCLK etc. signals being utilised to indicate the start of data and the end of data. (Figure 2, on page 7 and Figure 14, on page 20)

Register Value = $\mathbf{00_h}$

Another mode, **Video Mode** is a mode where the SOF and Row start/end signals are encoded (contained) in the Active Pixel data stream. In addition, all data that is not a SOF, Row start/end, or Active pixel data are forced to 0. i.e. all Blanking data from the A2D are forced to 0. The following sequence identifies the signals below: (see Figure , on page 30)

a) SOF (1st Row of Pixel Data) - “3FF x 4)

b) Start of all other Rows - “3FF x 2” then “000 x 2”

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Register Value = **70**

Address 65_h	**Pixel Data Stream Signal Control Register**						**Default 00_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**vcb**	**vsg**	**vcc**	**FUO**	**FUO**	**FUO**	**FUO**
Bit Number	**Function**	**Description**					**Reset State**
7	Unused	Unused					x
6	Vcode Blanking	1_b = All blanking data will be forced to 0 0_b = Blanking of Data					0_b
5	Vcode Sync Generation	1_b = Prefixes 3FF x 4 to beginning of active pixel data to indicate start of Row 1(SOF signal). Prefixes 3FF x 2 and then 000 x 2 to indicate start of all following Rows of data (VCLK) [Encoded data stream] 0_b = Use of SOF, HCLK etc. signals for sync generation (No coded data stream)					0_b
4	Vcode Clipping	1_b = Will clip output data stream to values 001_b to $3FE_b$ 0_b = No clipping of output data stream					0_b
3 - 0	FUO	Factory Use Only					0000_b

Table 53. Pixel Data Stream Signal Control Register

The FRC Definition Register; Table 54 allows the user to define the size of the dark rows to use as Clamping rows.

The frcs bit identifies the starting position of the Clamping rows. i.e. If 4d is written to this register, the first clamped dark row would be the 4th row.

The frcd bit identifies the FRC row depth. Allows the user to select the number of dark rows to clamp on.

NOTE! Since there exists ONLY 11 dark rows the addition of FRC Row Depth + FRC Row Start should not be greater than 11, otherwise light rows would be clamped in the process.

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Address 67_h	**FRC Definition**						**Default 24_h**
msb (7)	**6**	**5**	**4**	**3**	**2**	**1**	**lsb (0)**
x	**FUO**	**frcd[1]**	**frcd[0]**	**frcs[3]**	**frcs[2]**	**frcs[1]**	**frcs[0]**

Bit Number	**Function**	**Description**	**Reset State**
7	Unused	Unused	x
6	FUO	Factory Use Only	
5 - 4	FRC Row Depth	Defines the number of Clamping Rows. **NOTE!! The addition of FRC Row Depth + FRC Row Start should not be greater than 11_d.**	10_b
3 - 0	FRC Row Start	Defines the first Clamping row. Defines the FRC starting point.	0100

Table 54. FRC Definition Register

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14.0 Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS[1] (Voltages Referenced to VSS)			
Symbol	**Parameter**	**Value**	**Unit**
V_{DD}	DC Supply Voltage	-0.5 to 3.8	V
V_{in}	DC Input Voltage	0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	±50	mA
I	DC Current Drain, V_{DD} and V_{SS} Pins	±100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	°C

[1] Maximum Ratings are those values beyond which damage to the device may occur.

$V_{SS} = AV_{SS} = DV_{SS} = V_{SSO}$ ($DV_{SS} = V_{SS}$ of Digital circuit, $AV_{SS} = V_{SS}$ of Analog Circuit)
$V_{DD} = AV_{DD} = DV_{DD} = V_{DDO}$ ($DV_{DD} = V_{DD}$ of Digital circuit, $AV_{DD} = V_{DD}$ of Analog Circuit)

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality; voltage referenced to VSS)				
Symbol	Parameter	Min.	Max	Unit
V_{DD}	DC Supply Voltage, V_{DD} = 3.3V (Nominal)	3.0	3.6	V
T_A	Commercial Operating Temperature	0	40	°C
T_J	Junction Temperature	0	55	°C

Notes:
- All parameters are characterized for DC conditions after thermal equilibrium has been established.
- Unused inputs must always be tied to an appropriate logic level, e.g., either V_{SS} or V_{DD}.
- This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that

normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this high impedance circuit.
- For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V ± 0.3V; V_{DD} referenced to V_{SS}; T_a = 0°C to 40°C)					
			T_A = 0°C to 40°C		
Symbol	Characteristic	Condition	Min.	Max	Unit
V_{IH}	Input High Voltage		2.0	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{in}	Input Leakage Current, No Pull-up Resistor	$V_{in} = V_{DD}$ or V_{SS}	-5	5	µA

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I_{OH}	Output High Current	V_{DD} = Min., V_{OH} Min. = 0.8 * V_{DD}	-3		mA
I_{OL}	Output Low Current	V_{DD} = Min., V_{OL} Max = 0.4 V	3		mA
V_{OH}	Output High Voltage	V_{DD} = Min., I_{OH} = -100µA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = Min., I_{OL} = 100µA		0.2	V
I_{OZ}	3-State Output Leakage Current	Output = High Impedance, V_{out} = V_{DD} or V_{SS}	-10	10	µA
I_{DD}	Maximum Standby Supply Current	I_{out} = 0mA, V_{in} = V_{DD} or V_{SS}	0	15.0	mA

POWER DISSIPATION (VDD = 3.0V, VDD referenced to VSS; At = 25°C)

Symbol	Parameter	Condition	Typ	Unit
P_{STDBY}	Standby Power	INIT Pin Logic High	100	uW
P_{AVG}	Average Power	13.5 MHz Operation	250	mW

MCM20027 MONOCHROME CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS

Symbol	Parameter	Typ	Unit	Notes
E_{sat}	Saturation Exposure	0.14	µJ/cm^2	1
QE	Peak Quantum Efficiency (@550nm)	18	%	2
PRNU	Photoresponse Non-uniformity	12	% pk-pk	3

Notes:
1.For λ = 550 nm wavelength.
2.Refer to typical values from Figure 3, MCM20027 nominal spectral response.
3.For a 100 x 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal.

MCM20027 COLOR CMOS IMAGE SENSOR ELECTRO-OPTICAL CHARACTERISTICS

Symbol	Parameter	Typ	Unit	Notes
E_{sat}	Saturation Exposure	0.3	µJ/cm^2	1
QE_r	Red Peak Quantum Efficiency @ λ = 650 nm	12	%	2
QE_g	Green Peak Quantum Efficiency @ λ = 550 nm	11	%	2
QE_b	Blue Peak Quantum Efficiency @ λ = 450 nm	8	%	2

Notes:
1.For λ = 550 nm wavelength.
2.Refer to typical values from Figure 3, MCM20027 nominal spectral response.

CMOS IMAGE SENSOR CHARACTERISTICS

Symbol	Parameter	Typ	Unit	Notes
	Sensitivity	1.8	V/lux-sec	
I_d	Photodiode Dark Current	0.2	nA/cm^2	
DSNU	Dark Signal Non-Uniformity (Entire Field)	0.4	% rms	
CTE	Pixel Charge Transfer Efficiency	0.9995	%	1
f_H	Horizontal Imager Frequency	11.5	MHz	4
X_{ab}	Blooming Margin - shuttered light	200		2,3

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Notes:
1. Transfer efficiency of photosite
2. X_{ab} represents the increase above the saturation-irradiance level (H_{sat}) that the device can be exposed to before blooming of the pixel will occur.
3. No column streaking
4. At 30fps VGA

GENERAL				
Symbol	Parameter	Typ	Unit	Notes
$n_{e^- total}$	Total System (equivalent) Noise Floor	70	e^- rms	1
DR	System Dynamic Range	50	dB	

Notes:
1.Includes amplifier noise, dark pattern noise and dark current shot noise at 13.5 MHz data rates.

ANALOG SIGNAL PROCESSOR CHARACTERISTICS

Analog to Digital Converter (ADC)					
Symbol	Parameter	Min	Typ	Max	Units
	Resolution		10		bits
V_{IN}	Input Dynamic Range[8]		2.5		Vpp
INL	Integral Non-Linearity		±1.0		LSB
DNL	Differential Non-Linearity		±0.5		LSB
f_{max}	ADC Clock Rate			13.5	MHz

Notes:
[8] Effective differential signal dynamic range
9. INL & DNL test limits are adjusted to compensate for the effects of the LRC, DOVA and DPGA stages between teh EXT_VINS input and the input of the ADC.

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15.0 MCM20027 Pin Definitions

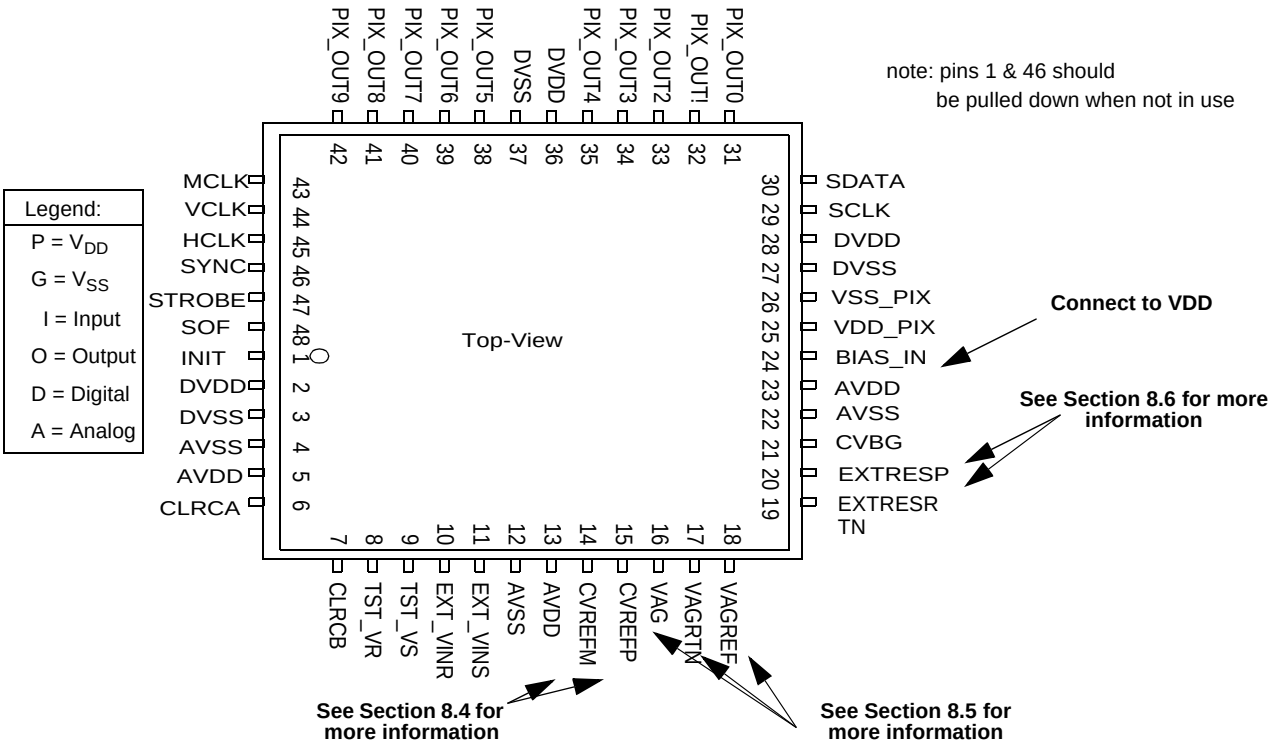

Figure 20. MCM20027 Pin Definitions

Pin No.	Pin Name	Description	Pin Type	Power
1	INIT	Sensor Initialize	I	
2	DVDD	Digital Power	P	D
3	DVSS	Digital Ground	G	D
4	AVSS	Analog Ground	G	A
5	AVDD	Analog Power	P	A
6	CLRCA	Line Rate Clamp Output	O	
7	CLRCB	Line Rate Clamp Output	O	
8	TST_VR	Analog test reference Output	O	
9	TST_VS	Analog test signal Output	O	
10	EXT_VINR	Analog test reference Input	I	
11	EXT_VINS	Analog test signal Input	I	
12	AVSS	Analog Ground	G	A
13	AVDD	Analog Power	P	A
14	CVREFM	Bias Reference Bottom Output	O	
15	CVREFP	Bias Reference Top Output	O	
16	VAG	Common Mode Cap Input	I	
17	VAGRETN	Common Mode Cap Return		A
18	VAGREF	Common Mode Caps Input	I	
19	EXTRESRTN	EXTRES Return		A
20	EXTRES	External Bias Resistor Input	I	
21	CVBG	Bandgap Voltage Testpoint		
22	AVSS	Analog Ground	G	A
23	AVDD	Analog Power	P	A
24	BIAS_IN	Pixel row 1046/7 inj Bias in	I	

Pin No.	Pin Name	Description	Pin Type	Power
25	VDD_PIX	Pixel power		
26	VSS_PIX	Pixel ground		
27	DVSS	Digital Ground	G	D
28	DVDD	Digital Power	P	D
29	SCLK	I2C Serial Clock	I/O	
30	SDATA	I2C Serial Data	I/O	
31	PIX_OUT0	Output bit 0 = 1 Weight	O	
32	PIX_OUT1	Output bit 1 = 2 Weight	O	
33	PIX_OUT2	Output bit 2 = 4 Weight	O	
34	PIX_OUT3	Output bit 3 = 8 Weight	O	
35	PIX_OUT4	Output bit 4 = 16 Weight	O	
36	DVDD	Digital Power	P	D
37	DVSS	Digital Ground	G	D
38	PIX_OUT5	Output bit 5 = 32 Weight	O	
39	PIX_OUT6	Output bit 6 = 64 Weight	O	
40	PIX_OUT7	Output bit 7 = 128 Weight	O	
41	PIX_OUT8	Output bit 8 = 256 Weight	O	
42	PIX_OUT9	Output bit 9 = 512 Weight	O	
43	MCLK	Master Clock	I	
44	VCLK	Line Sync	O	
45	HCLK	Pixel Sync	O	
46	SYNC	Sensor Sync Signal	I	
47	STROBE	Strobe signal	O	
48	SOF	Start Of Frame	O	

Table 55. MCM20027 Pin Definitions

I	**INPUT**
P	**POWER**
G	**GROUND**
O	**OUTPUT**
D	**DIGITAL**
A	**ANALOG**
I/O	**BIDIRECTIONAL**

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16.0 MCM20027 Packaging Information

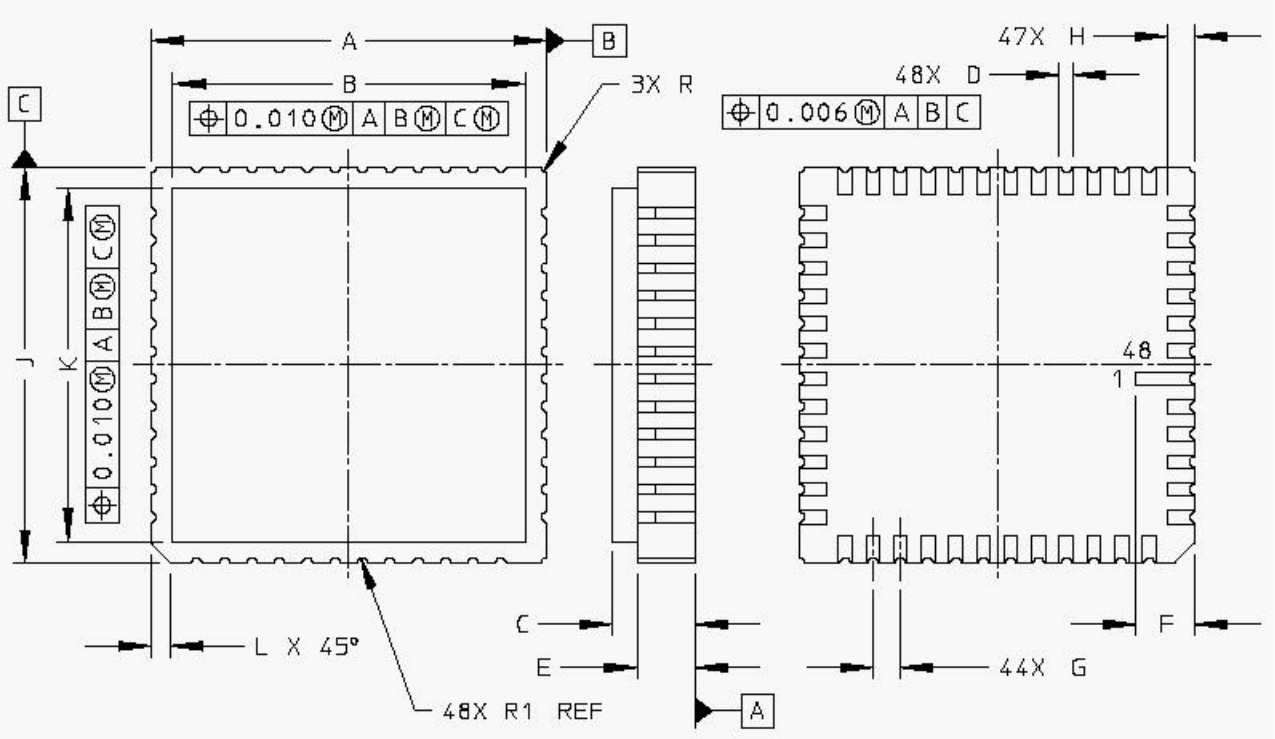

Figure 21. 48 Terminal ceramic leadless chip carrier (bottom view)

Dim	Min(Inches)	Max(Inches)
A	0.555	0.572
B	0.525	0.545
C	---	0.09362
D	0.016	0.024
E	0.054	0.068
F	0.075	0.095
G	0.040 BSC	
H	0.033	0.047
J	0.555	0.572
K	0.525	0.545
R	0.0075 (Radius)	
R1	0.0075 (Radius)	

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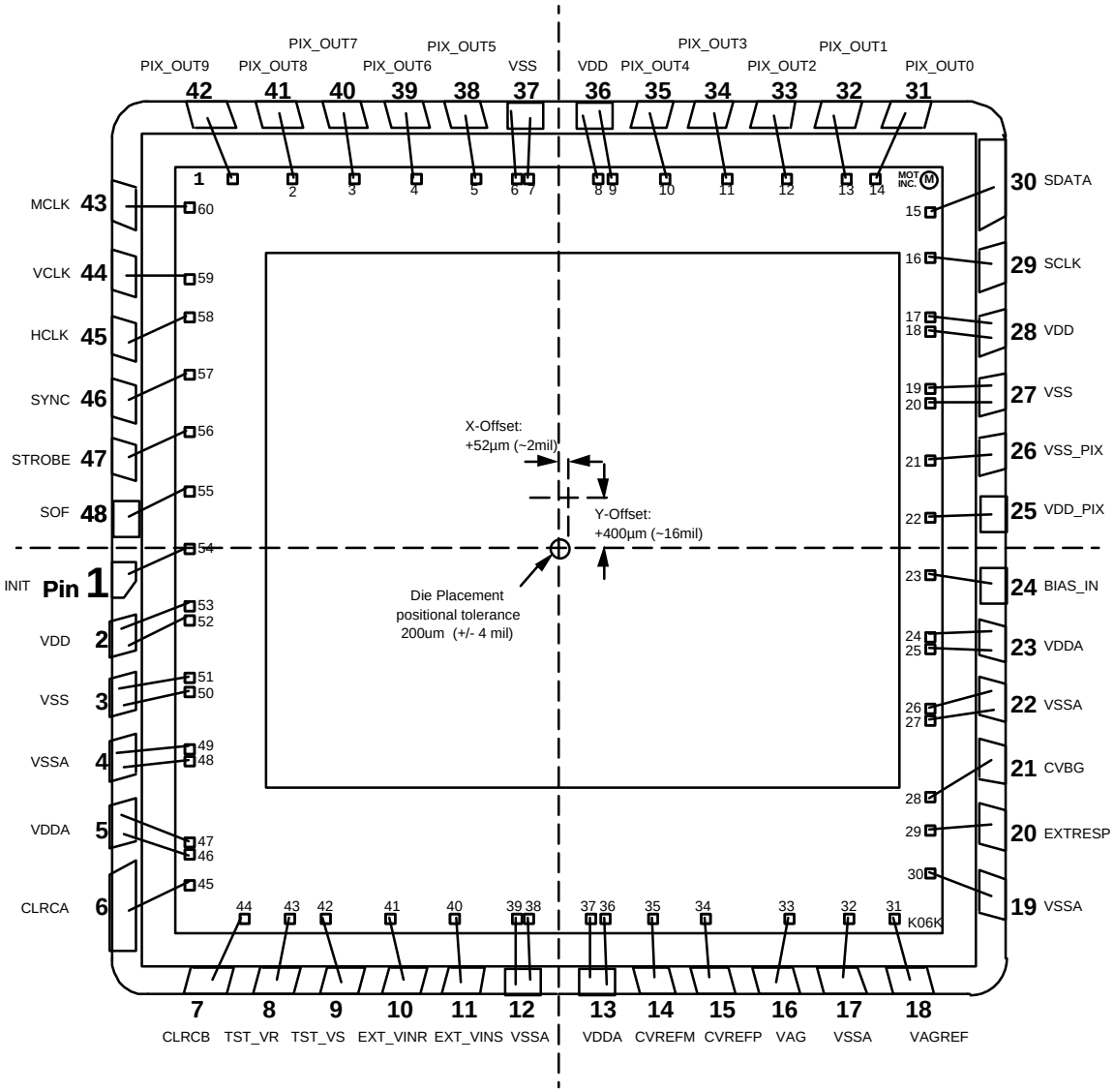

Figure 23. Center of the focal plane array with respect to the die cavity (top view)

Notes:

1. Dimensions are in inches.
2. Interpret dimensions and tolerances per ASME Y14.5-1994

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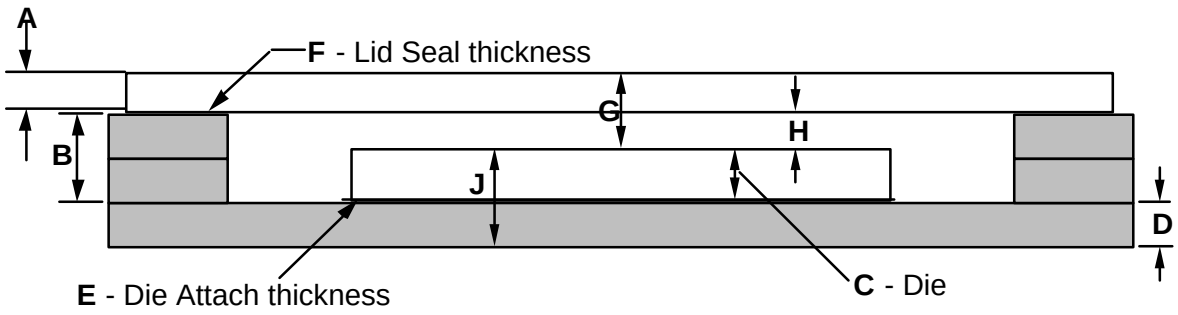

		Metric (mm)			English (inches)		
Dimension	**Description**	**Nominal**	min	max	**Nominal**	min	max
A	Glass (Thickness)	0.55000	0.50000	0.60000	0.02165	0.01969	0.02362
B	Cavity (Depth)	1.11760	0.99060	1.24460	0.04400	0.03900	0.04900
C	Die - Si (Thickness)	0.72500	0.70500	0.74500	0.02854	0.02776	0.02933
D	Bottom Layer (Thickness)	0.43180	0.38100	0.48260	0.01700	0.01500	0.01900
E	Die Attach - bondline (Thickness)	0.02540	0.01270	0.07620	0.00100	0.00050	0.00300
F	Glass Attach - bondline (Thickness)	0.02540	0.00635	0.05080	0.00100	0.00025	0.00200
G	Imager to Lid - outer surface (d)	0.94260	0.67575	1.17770	0.03711	0.02660	0.04637
H	Imager to Lid - inner surface (d)	0.39260	0.17575	0.57770	0.01546	0.00692	0.02274
J	Imager to seating plane - of pkg	1.18220	1.09870	1.30380	0.04654	0.04326	0.05133
	Pkg (Th - total)	2.12480	1.87795	2.37800	0.08365	0.07393	0.09362
	Base (Th)	1.54940	1.70180	1.39700	0.06100	0.06700	0.05500

Note: The package sketch is representative and does not necessarily reflect exact scale and relative feature sizes.

Reference Notes:
1mil = 25.4um
1mm = 39.37mil

Figure 22. 48 Terminal ceramic leadless chip carrier (z-direction view)

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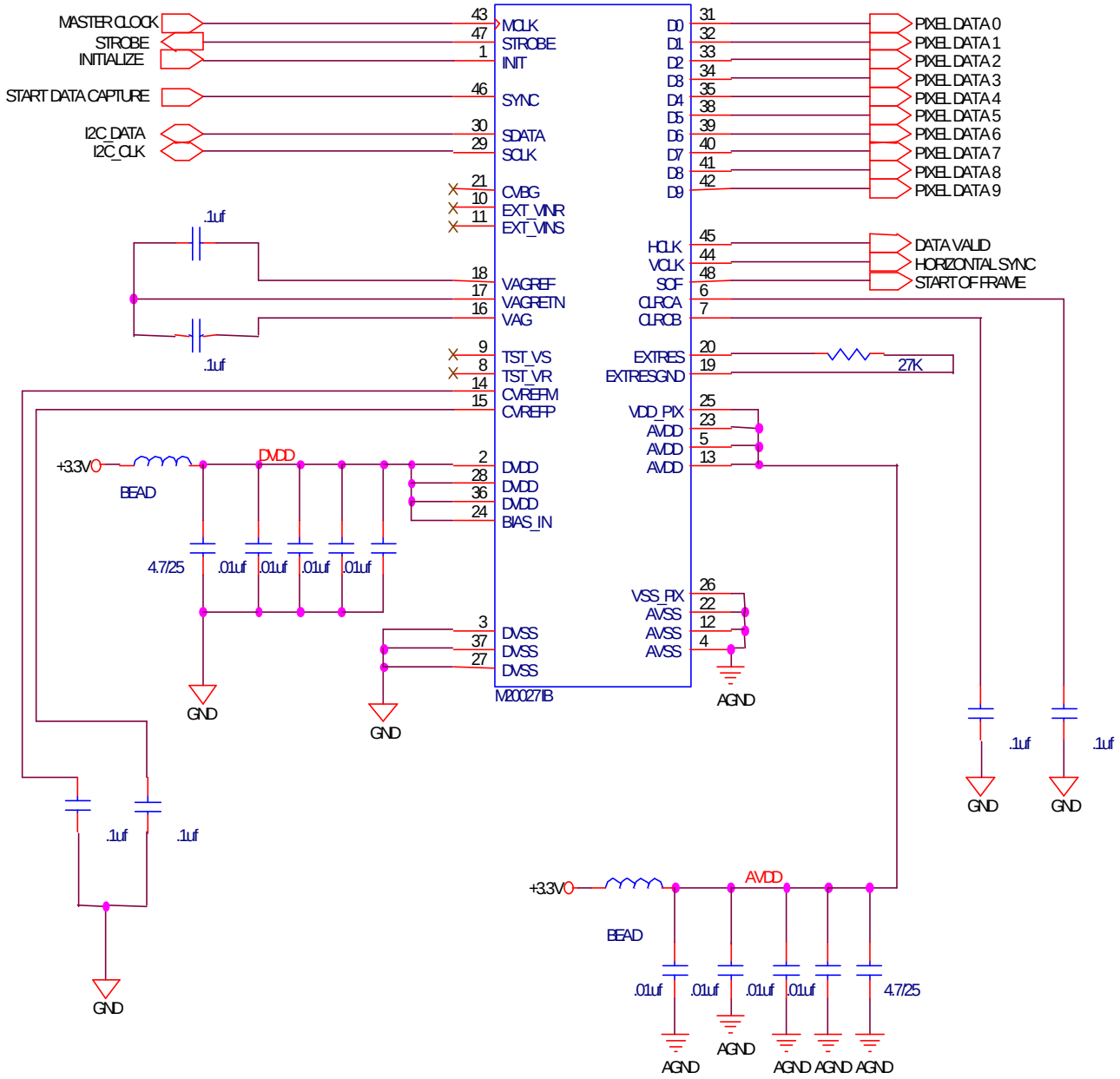
17.0 MCM20027 Typical Connection

Below you will find a schematic illustrating a typical connection of an MCM20027 CMOS sensor. One can use this as a reference when connecting the sensor with another external device such as an image processor, SDRAM etc.This schematic also illustrates the connection of the required passives on the sensor.



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ELECTRO STATIC DISCHARGE WARNING:
This device is sensitive to electrostatic discharge (ESD).ESD immunity meets Human Body Model (HBM) ≤ 1500 V and Machine Model (MM) ≤ 150 V Additional ESD data upon request. When handling this part, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its immediate performance and/or reduce the parts expected lifetime..

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