HM628128BI Series

131,072-word × 8-bit High speed CMOS Static RAM

HITACHI

ADE-203-363A(Z)
Rev. 1.0
Apr. 28, 1995

The Hitachi HM628128BI is a CMOS static RAM organized 131,072-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS shrink process technology. It offers low power standby power dissipation, therefore, it is suitable for battery back-up systems. The device, packaged in a 525-mil SOP or a 600-mil plastic DIP is available.

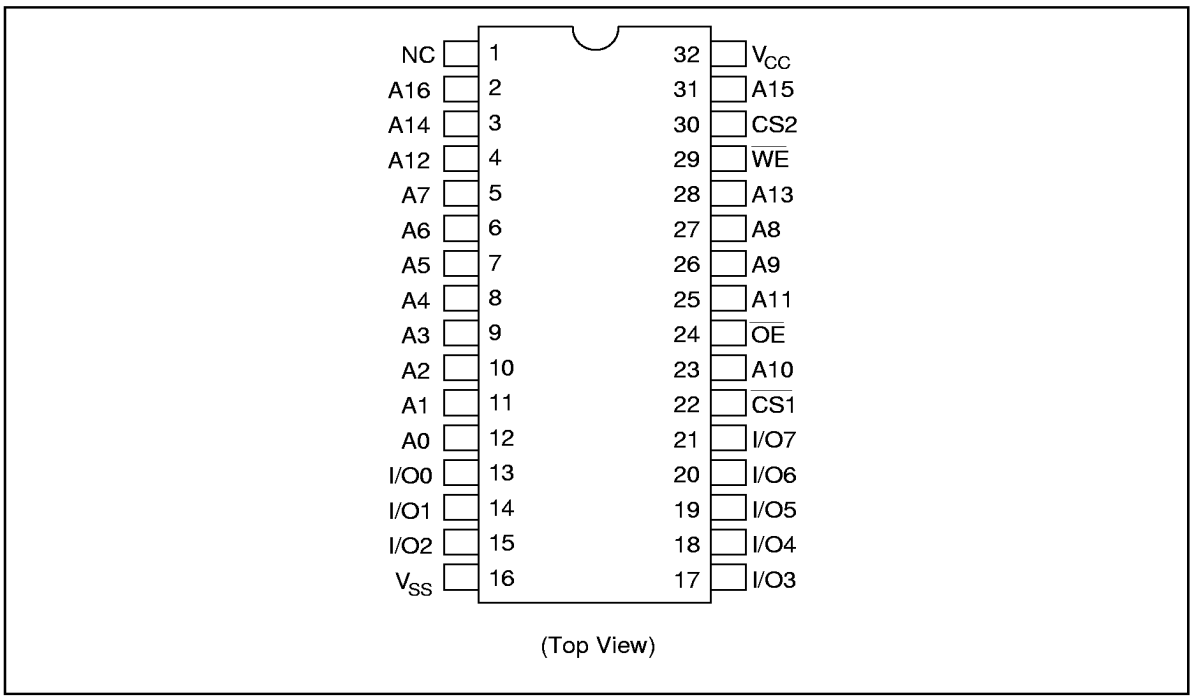
Features

- High speed
  Fast access time: 85/100 ns (max)
- Low power
  standby: 10 µW (typ)
  Operation: 50 mW/MHz (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- Directly TTL compatible
  All inputs and outputs
- Capability of battery back up operation
- 2 chip selection for battery back up
- Operating temperature range
- –40 to +85°C

Ordering Information

Part No.	Access time	Data Retention Current	Package
HM628128BLPI-8	85 ns	50 µA	600-mil 32-pin plastic DIP (DP-32)
HM628128BLPI-10	100 ns	50 µA	
HM628128BLFPI-8	85 ns	50 µA	525-mil 32-pin plastic SOP (FP-32D)
HM628128BLFPI-10	100 ns	50 µA	

Pin Arrangement

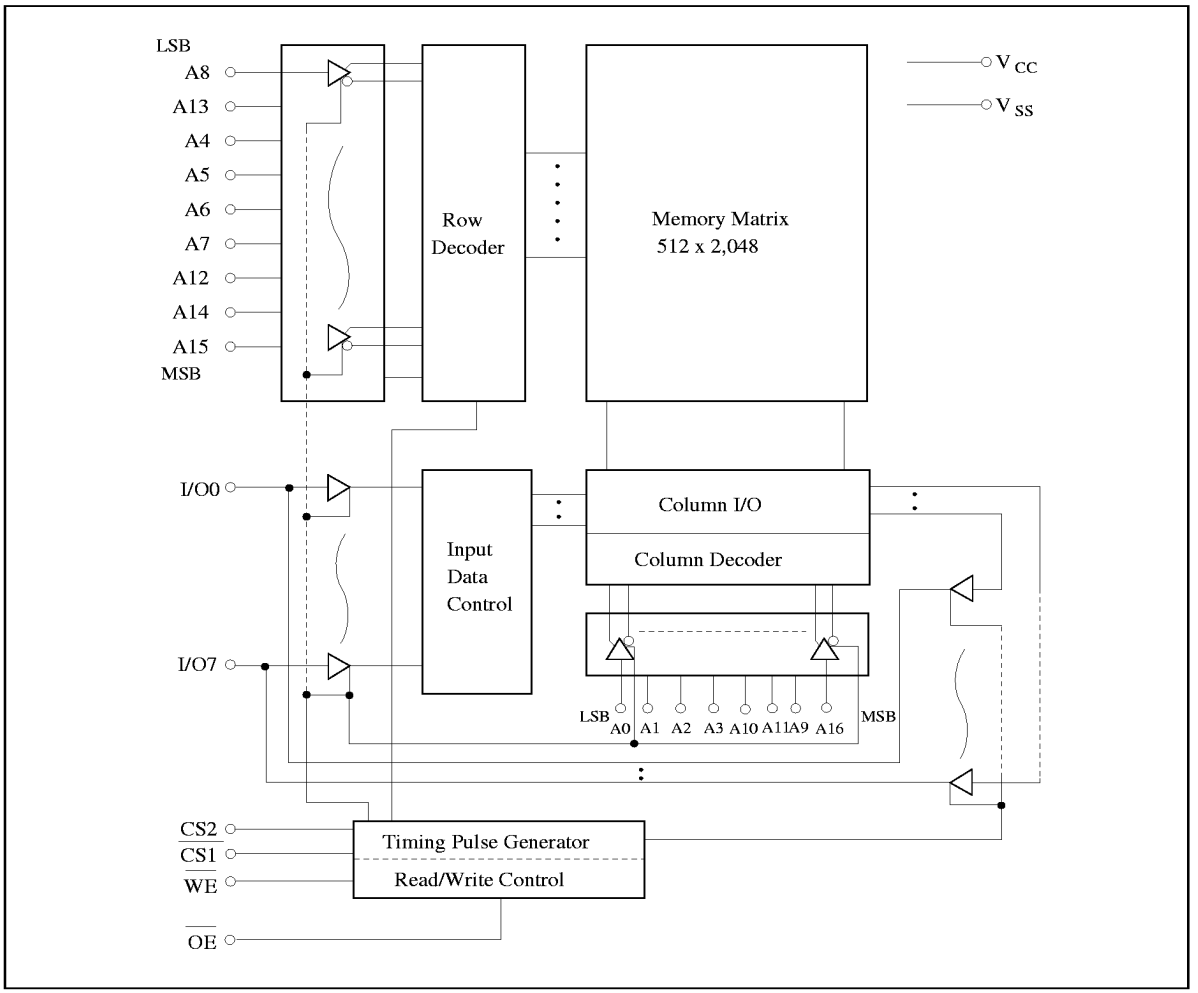


(Top View)

Pin Description

Pin name	Function
A0 to A16	Address
I/O0 to I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{cc}	Power supply
V_{ss}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5[*1] to V_{CC}+0.3[*2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–40 to +85	°C

Notes: 1. –3.0 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 7.0 V.

Function Table

WE	CS1	CS2	OE	Mode	V_{CC} current	I/O pin	Ref. cycle
X	H	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
X	X	L	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X:H or L

Recommended DC Operating Conditions (Ta = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage (logic 1)	V_{IH}	2.4	—	V_{CC} + 0.3	V
Input low voltage (logic 0)	V_{IL}	–0.3[*1]	—	0.6	V

Note9 1. –3.0 V for pulse half-width ≤ 30ns

DC Characteristics (Ta = –40 to +85°C, V_{CC} = 5V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current : DC	I_{CC}	—	15	30	mA	$\overline{CS1}$ = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL} $I_{I/O}$ = 0mA
Operating power supply current	I_{CC1}	—	35	70	mA	Min.cycle, duty = 100 %, $\overline{CS1}$=V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
	I_{CC2}	—	10	25	mA	Cycle time = 1 µs, duty = 100 % $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V CS2 ≥ V_{CC} – 0.2 V, Others = V_{IH}/V_{IL} V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby V_{CC} current : DC	I_{SB}	—	1	2	mA	CS2 = V_{IL} or CS2 = V_{IH}, $\overline{CS1}$ =V_{IH}
Standby V_{CC} current (1): DC	I_{SB1}	—	2	100	µA	0V≤ Vin ≤ V_{CC} , (1) 0V≤ CS2 ≤ 0.2V or (2) CS2 ≥ V_{CC} – 0.2V , $\overline{CS1}$ ≥ V_{CC} – 0.2V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL}= 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH}= –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25ÞC and not guaranteed.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin*1	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$*1	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100 % tested.

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 5 V ±10%, unless otherwise noted.)

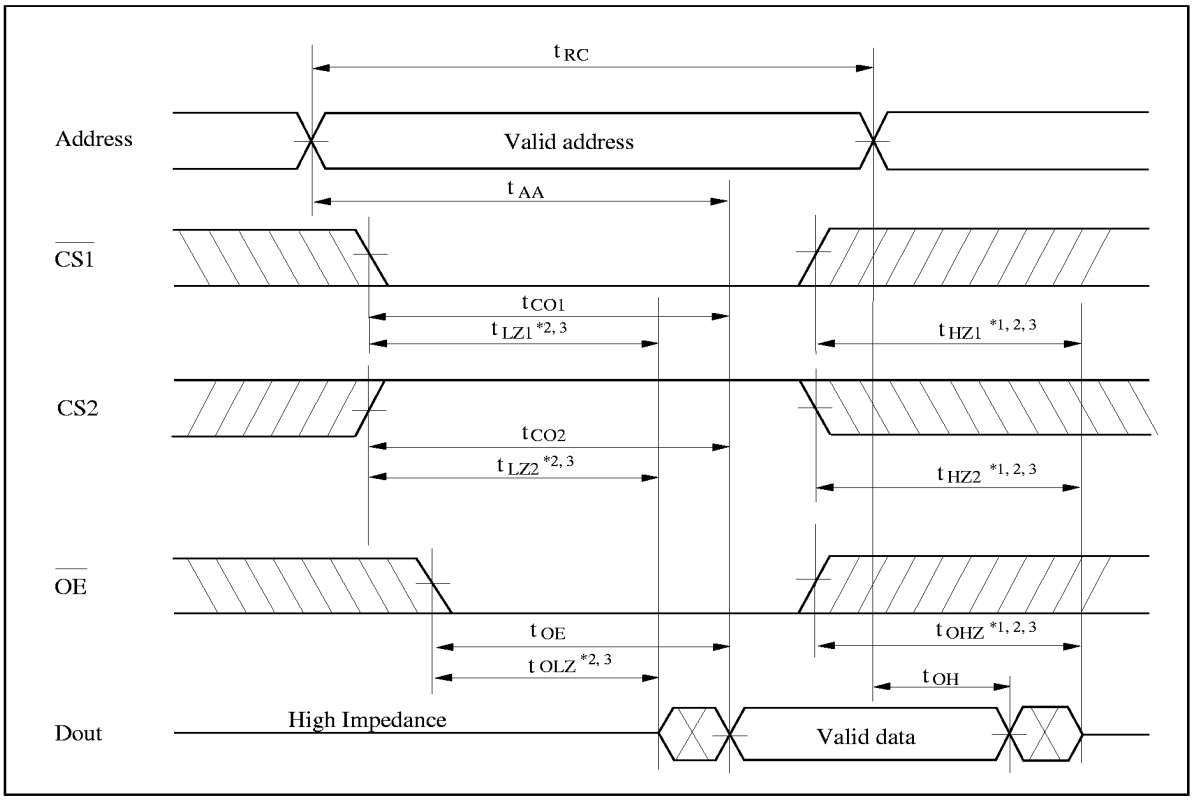
Test Conditions

- Input pulse levels : 0.5 V to 2.5 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels : 1.5 V
- Output load : 1 TTL Gate and C_L (100pF) (Including scope and jig)

Read Cycle

		HM628128BI					
		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	85	—	100	—	ns	
Address access time	t_{AA}	—	85	—	100	ns	
Chip selection to output valid	t_{CO1}	—	85	—	100	ns	
	t_{CO2}	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	45	—	50	ns	
Chip selection to output in low-Z	t_{LZ1}	10	—	10	—	ns	2, 3
	t_{LZ2}	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	30	0	35	ns	1, 2, 3
	t_{HZ2}	0	30	0	35	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	ns	

Read Cycle Timing[*4]



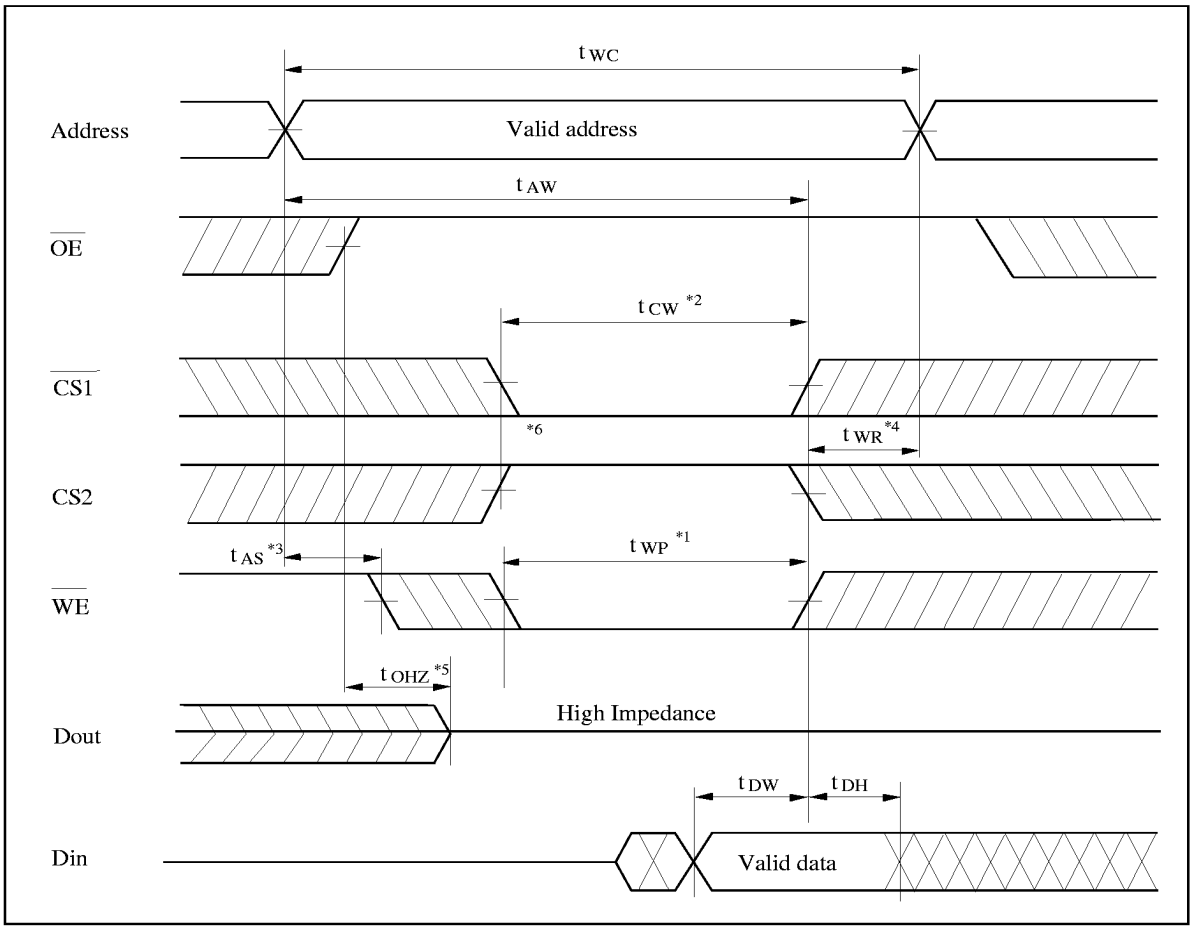
Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. This parameter is sampled and not 100 % tested.
4. $\overline{WE}$ is high for read cycle.

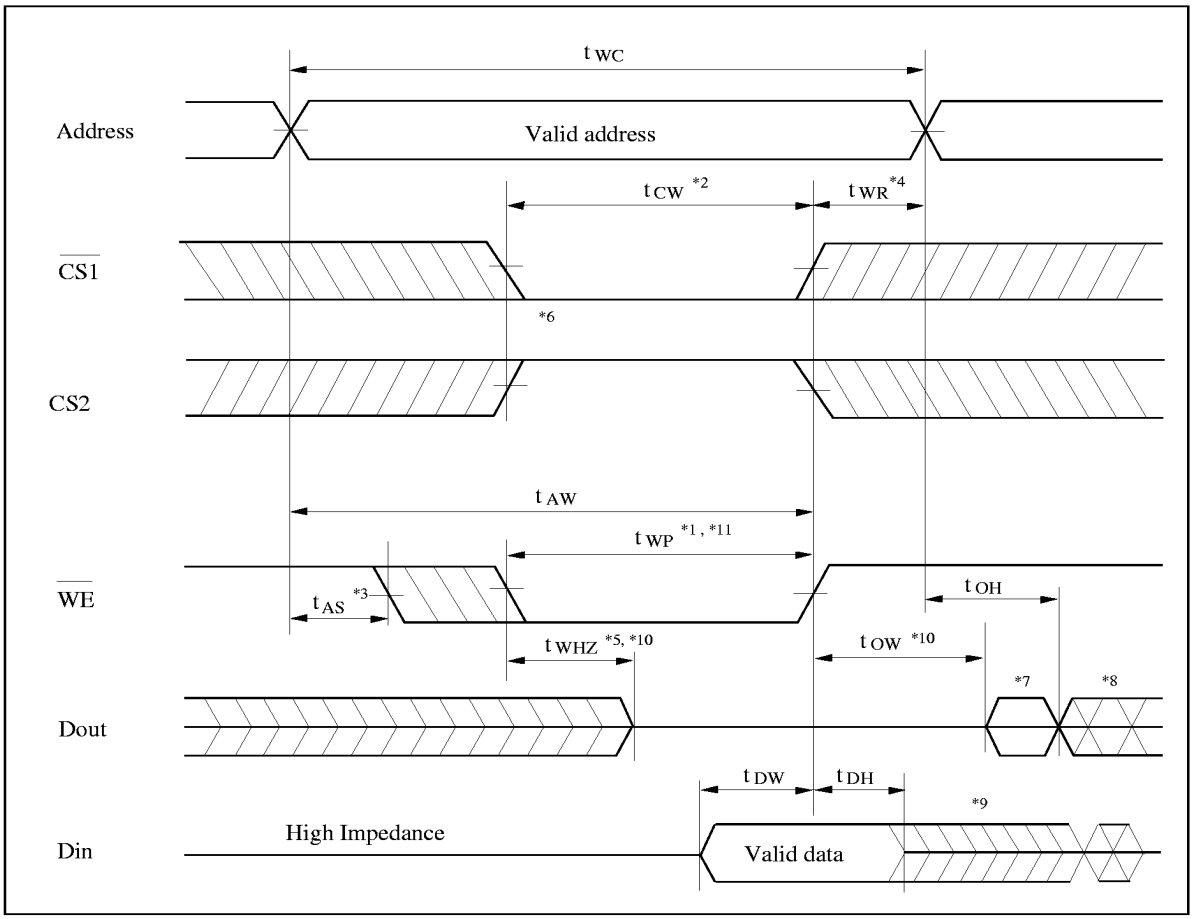
Write Cycle

		HM628128BI					
		-8		-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	85	—	100	—	ns	
Chip selection to end of write	t_{CW}	75	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	
Address valid to end of write	t_{AW}	75	—	80	—	ns	
Write pulse width	t_{WP}	55	—	60	—	ns	11
Write recovery time	t_{WR}	0	—	0	—	ns	
Write to output in high-Z	t_{WHZ}	0	30	0	35	ns	10
Data to write time overlap	t_{DW}	35	—	40	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	10

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ low fix)



Notes: 1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

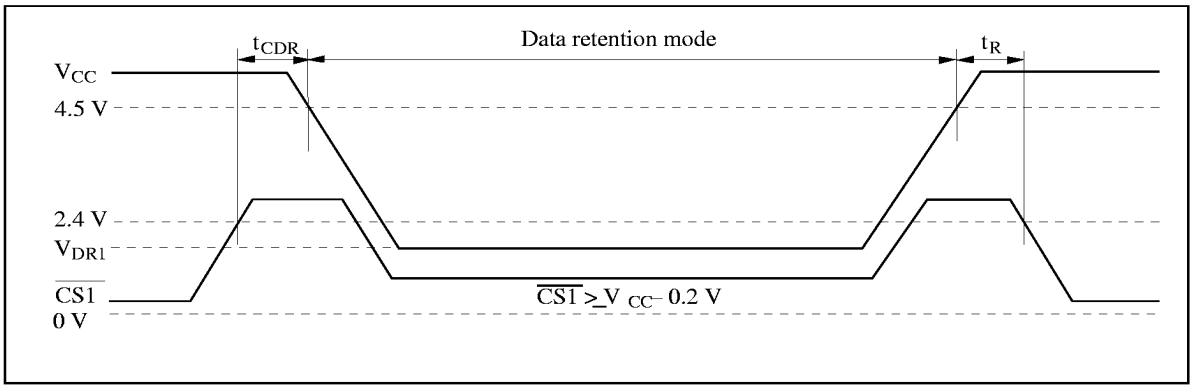
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. If the $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after the $\overline{WE}$ going low, the outputs remain in a high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read date of next address.

9. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
10. This parameter is sampled and not 100 % tested.
11. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of date bus contention, $t_{WP} \geq t_{DW}$ (min) + t_{WHZ} (max).

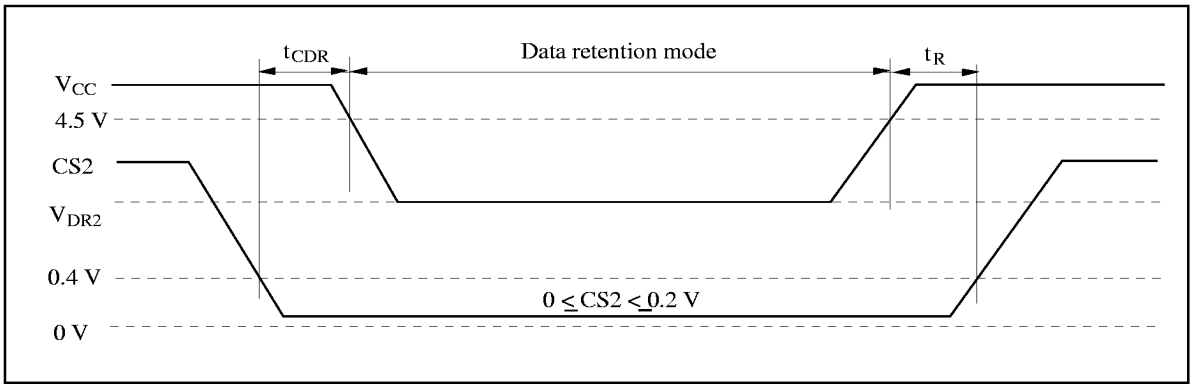
Low V_{CC} Data Retention Characteristics (Ta = –40 to +85ºC)

Parameter	Symbol	Min	Typ*2	Max	Unit	Test conditions*3
V_{CC} for data retention	V_{DR}	2.0	—	—	V	0 V ≤ Vin ≤ V_{CC}, (1)0 V ≤ CS2 ≤ 0.2V or (2)CS2 ≥ V_{CC} – 0.2V, $\overline{CS1}$ ≥ V_{CC} – 0.2V
Data retention current	I_{CCDR}	—	1	50*1	µA	V_{CC} = 3V, 0V ≤ Vin ≤ 3V (1)0V ≤ CS2 ≤ 0.2V or (2)CS2 ≥ V_{CC} – 0.2V, $\overline{CS1}$ ≥ V_{CC} – 0.2V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5*4	—	—	ms	

Low V_{CC} Data Retention Waveform (1) ($\overline{CS1}$ Controlled)[*3]



Low V_{CC} Data Retention Waveform (2) (CS2 Controlled)[*3]

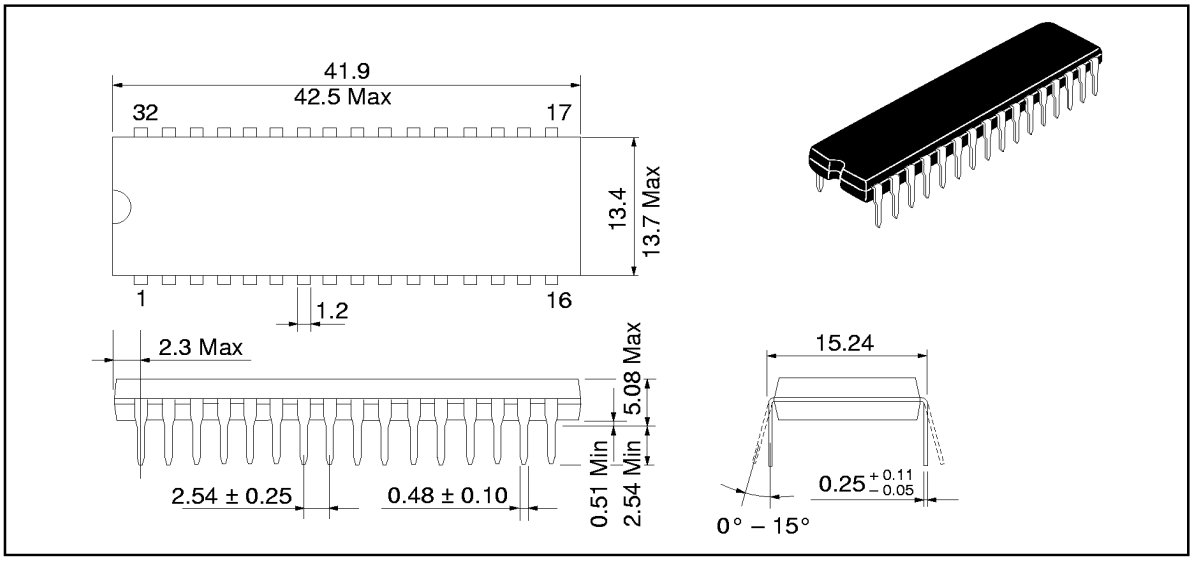


Notes: 1. This characteristics is guaranteed 20 µA max. at Ta = –40 to +40°C.

2. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
3. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} –0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
4. V_{CC} rising time must be more than 50 ms. When V_{CC} rising time is less than 50 ms, t_R must be 50 ms or more.

Package Dimensions

DP-32



FP-32D