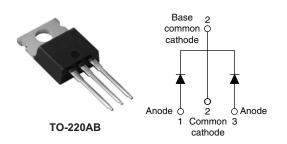


Vishay High Power Products

# **Dual High-Voltage Trench MOS Barrier Schottky Rectifier**



2 x 20 A

100 V

0.67 V

**PRODUCT SUMMARY** 

I<sub>F(AV)</sub>

V<sub>RRM</sub>

Maximum V<sub>F</sub> at 20 A at 125 °C

### FEATURES

- 150 °C high performance Schottky diode
- Very low forward voltage drop
- Extremely low reverse leakage
- Optimized V<sub>F</sub> vs. I<sub>R</sub> trade off for high efficiency
- · Increased ruggedness for reverse avalanche capability
- RBSOA available on demand
- Negligible switching losses
- Solder dip 260 °C, 40 s
- Full lead (Pb)-free and RoHS compliant devices
- · Designed and qualified for industrial level

### **APPLICATIONS**

- High efficiency SMPS
- High frequency switching
- · Output rectification
- Reverse battery protection
- Freewheeling
- Dc-to-dc systems
- Increased power density systems

MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL CHARACTERISTICS VALUES UNITS						
V <sub>RRM</sub>		100	N/			
V <sub>F</sub>	20 Apk, T <sub>J</sub> = 125 °C (typical, per leg)	0.63	v			
TJ	Range	- 40 to 150	°C			

VOLTAGE RATINGS						
PARAMETER SYMBOL TEST CONDITIONS V40100L-F UNITS						
Maximum DC reverse voltage	V <sub>R</sub>	T <sub>J</sub> = 25 °C	100	V		

ABSOLUTE MAXIMUM RATINGS							
PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum averageper legforward currentper device			EQ.9% duty cycle at T 160.90 reatons years way of arm		20		
		$I_{F(AV)}$ 50 % duty cycle at $T_C$ = 160 °C, rectangular waveform		40			
Maximum peak one cycle non-repetitive surge current per leg		I <sub>FSM</sub>	5 $\mu s$ sine or 6 $\mu s$ rect. pulse	Following any rated load condition and with rated V <sub>RRM</sub> applied	900	A	
			10 ms sine or 6 ms rect. pulse		300		
Non-repetitive avalanche energy per leg		E <sub>AS</sub>	$T_J = 25 \text{ °C}, I_{AS} = 1.5 \text{ A}, L = 60 \text{ mH}$		67.5	mJ	
		that $T_J < T_J$ max. $I_{AS}$ at $T_J$ max.	puency of operation and time pulse duration so ax. $I_{AS}$ at $T_J$ max. as a function of time pulse		A		



COMPLIANT

## V40100L-F



## Vishay High Power Products

Dual High-Voltage Trench MOS Barrier Schottky Rectifier

ELECTRICAL SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CO	TEST CONDITIONS TYP. MAX. UN				
		5 A	T <sub>J</sub> = 25 °C	0.51	-	v	
		10 A		0.59	-		
Forward voltage drop per leg	V <sub>FM</sub> <sup>(1)</sup>	20 A		0.72	0.82		
	VFM ()	5 A		0.44	-		
		10 A T <sub>J</sub> = 125 °C	0.53	-			
		20 A		0.63	0.67		
Reverse leakage current	I <sub>RM</sub> <sup>(2)</sup>	T <sub>J</sub> = 25 °C	$V_R = Rated V_R$	-	1000	μA	
		T <sub>J</sub> = 125 °C		21	45	mA	
Maximum voltage rate of change	dV/dt	Rated V <sub>R</sub>		-	10 000	V/µs	

#### Notes

 $^{(1)}$  Pulse width < 300  $\mu s,$  duty cycle < 2 %

<sup>(2)</sup> Pulse test: Pulse width  $\leq$  40 ms

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction and storage temperature rang	je	T <sub>J</sub> , T <sub>Stg</sub>		- 40 to 150	°C	
Maximum thermal resista junction to case per leg	nce,		<b>20</b>	4	°C/W	
Maximum thermal resista junction to case per device	,	R <sub>thJC</sub>	DC operation	2		
Typical thermal resistance case to heatsink	e,	R <sub>thCS</sub>		0.5		
Approximate weight				2	g	
				0.07	oz.	
Mounting torque	minimum			6 (5)	kgf · cm	
	maximum			12 (10)	(lbf ⋅ in)	
Marking device			Case style TO-220AB	V40100L		



### Dual High-Voltage Trench MOS Vishay High Power Products Barrier Schottky Rectifier

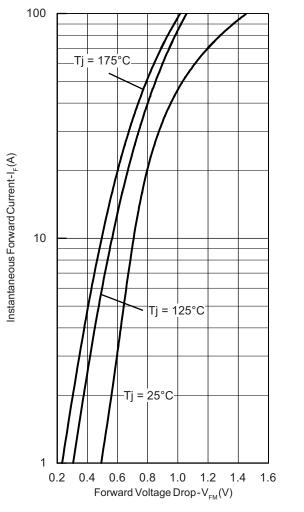


Fig. 1 - Maximum Forward Voltage Drop Characteristics

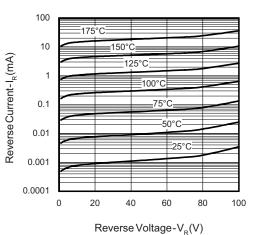


Fig. 2 - Typical Values of Reverse Current vs.



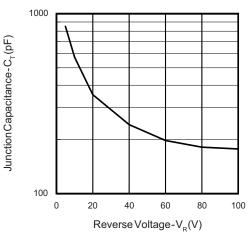


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

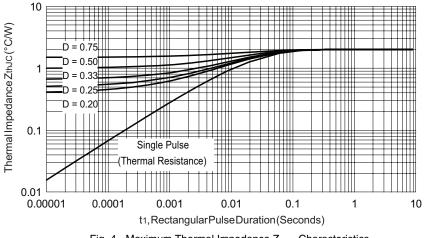


Fig. 4 - Maximum Thermal Impedance  $Z_{\text{thJC}}$  Characteristics

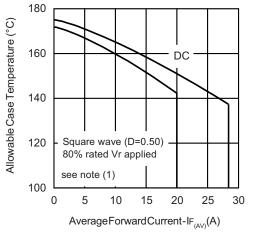
# V40100L-F

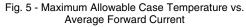


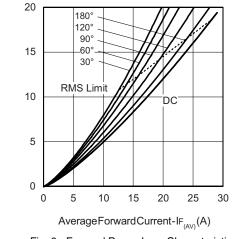
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Average Power Loss-(Watts)









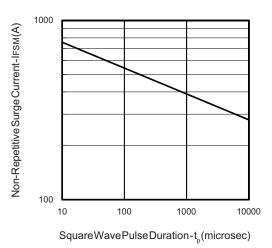


Fig. 7 - Maximum Non-Repetitive Surge Current

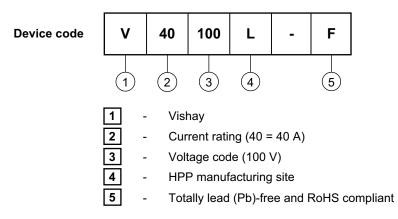
#### Note

<sup>(1)</sup> Formula used:  $T_C = T_J - (Pd + Pd_{REV}) \times R_{thJC}$ ;  $Pd = Forward power loss = I_{F(AV)} \times V_{FM} at (I_{F(AV)}/D)$  (see fig. 6);  $Pd_{REV} = Inverse power loss = V_{R1} \times I_R (1 - D)$ ;  $I_R at V_{R1} = 80 \%$  rated  $V_R$ 



Dual High-Voltage Trench MOS Vishay High Power Products Barrier Schottky Rectifier

### ORDERING INFORMATION TABLE



LINKS TO RELATED DOCUMENTS				
Dimensions http://www.vishay.com/doc?95222				
Part marking information	http://www.vishay.com/doc?95028			



**Vishay Semiconductors** 

**TO-220AB** 

### **DIMENSIONS** in millimeters and inches





.ead	assignments

**Diodes** 

1. - Anode/open 2. - Cathode 3. - Anode

SYMBOL	MILLIMETERS		INCHES		NOTES
STWDUL	MIN.	MAX.	MIN.	MAX.	NOTES
А	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6

#### Notes

- <sup>(1)</sup> Dimensioning and tolerancing as per ASME Y14.5M-1994
- <sup>(2)</sup> Lead dimension and finish uncontrolled in L1
- <sup>(3)</sup> Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- $^{\left( 4\right) }$  Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1

MILLIMETERS INCHES SYMBOL NOTES MIN. MAX. MIN. MAX. 10.51 0.414 10.11 0.398 3,6 Е E1 6.86 8.89 0.270 0.350 6 E2 0.76 0.030 7 --2.41 2.67 0.095 0.105 е 0.208 e1 4.88 5.28 0.192 H1 6.09 6.48 0.240 0.255 6,7 13.52 14.02 0.532 0.552 L L1 3.32 3.82 0.131 0.150 2 ØΡ 3.54 3.73 0.139 0.147 2.60 0.102 Q 3.00 0.118 90° to 93° 90° to 93° θ

Conforms to JEDEC outline TO-220AB

- (7) Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, except A2 (maximum) and D2 (minimum) where dimensions are derived from the actual package outline



Vishay

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