9-BIT MAGNITUDE COMPARATOR

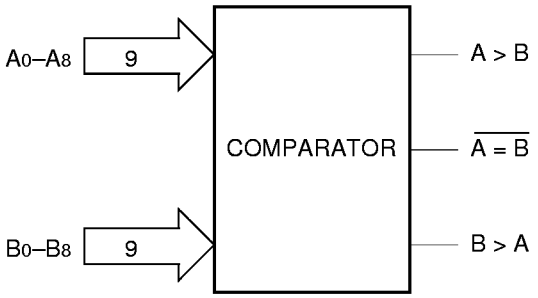
FEATURES

- **1100ps max. Propagation Delay $\overline{A = B}$**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E166**
- **Available in 28-pin PLCC package**

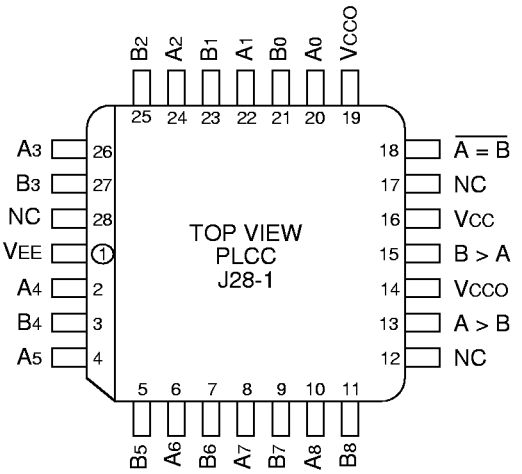
DESCRIPTION

The SY10/100E166 are 9-bit magnitude comparators designed for use in new, high-performance ECL systems. The E166 compares the binary value of two 9-bit words and indicates whether one word is greater than or equal to the other.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
A_0–A_8	A Data Inputs
B_0–B_8	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A = B}$	A Equal to B Output (active-LOW)
V_{CCO}	V_{CC} to Output

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Issue Date: February, 1998

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	113	136	—	113	136	—	113	136		
	100E	—	113	136	—	113	136	—	130	156		

AC ELECTRICAL CHARACTERISTICS

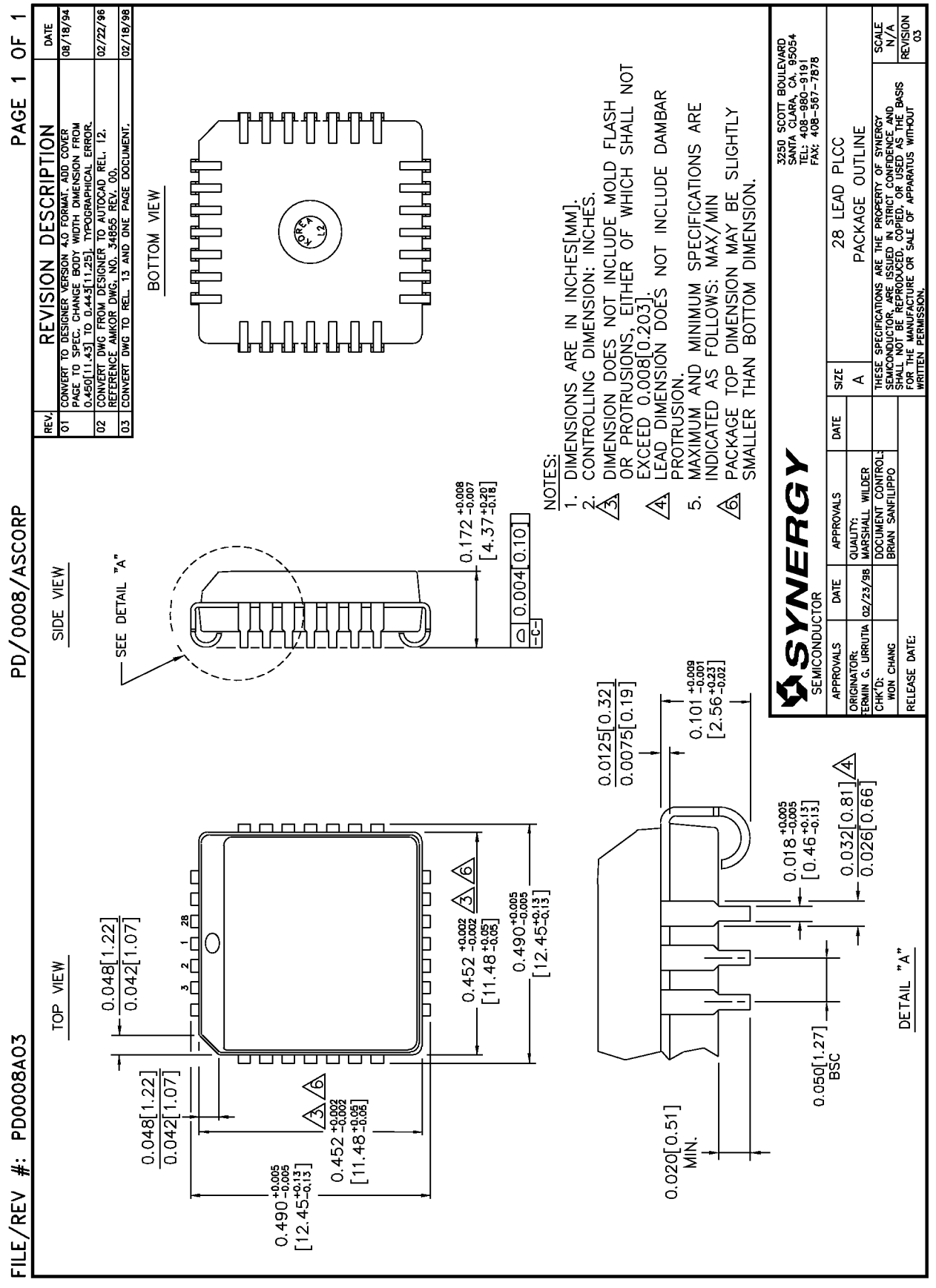
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	D to A = B	500	750	1100	500	750	1100	500	750	1100		
	D to A < B, A > B	500	850	1400	500	850	1400	500	850	1400		
t_r	Rise/Fall Time	300	450	800	300	450	800	300	450	800	ps	—
t_f	20% to 80%											

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E166JC	J28-1	Commercial
SY10E166JCTR	J28-1	Commercial
SY100E166JC	J28-1	Commercial
SY100E166JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)



FEATURES

- 1000MHz min. operating frequency
- Extended 100E V_{EE} range of –4.2V to –5.5V
- 800ps max. clock to output
- Single-ended outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E167
- Available in 28-pin PLCC package

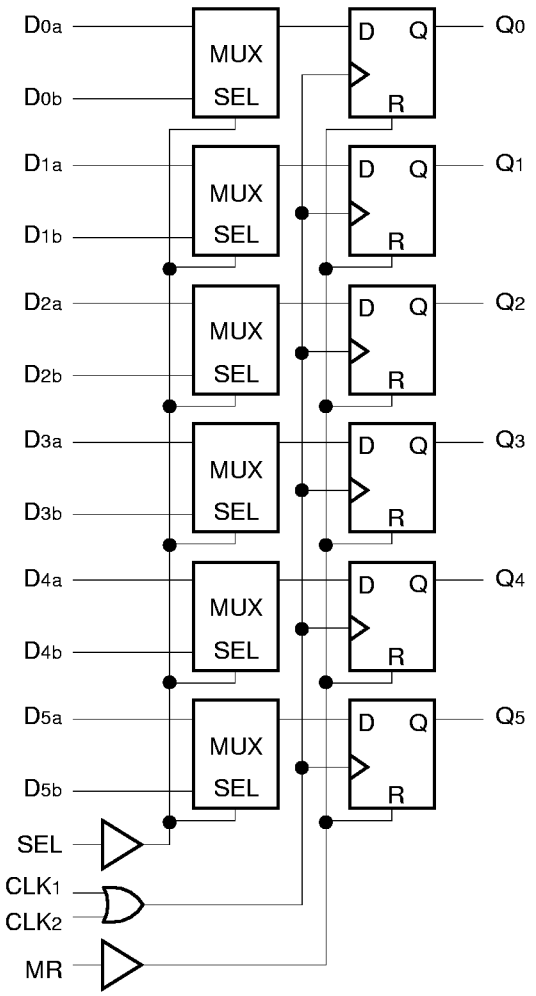
DESCRIPTION

The SY10/100E167 offer six 2:1 multiplexers followed by D flip-flops with single-ended outputs, designed for use in new, high-performance ECL systems. The Select (SEL) control allows one of the two data inputs to the multiplexer to pass through. The two external clock signals (CLK_1, CLK_2) are gated through a logical OR operation before use as control for the six flip-flops. The selected data are transferred to the flip-flops on the rising edge of CLK_1 or CLK_2 (or both).

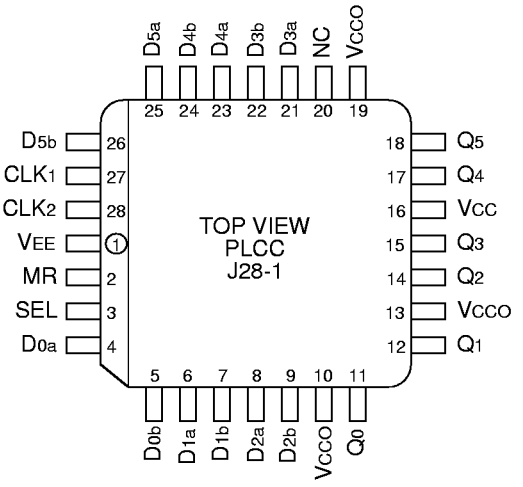
The multiplexer operation is controlled by the Select (SEL) signal which selects one of the two bits of input data at each mux to be passed through.

When a logic HIGH is applied to the Master Reset (MR) signal, it operates asynchronously to take all outputs Q to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D_{0a}–D_{5a}	Input Data a
D_{0b}–D_{5b}	Input Data b
SEL	Select Input
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0–Q_5	Data Outputs
V_{CCO}	V_{CC} to Output

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