

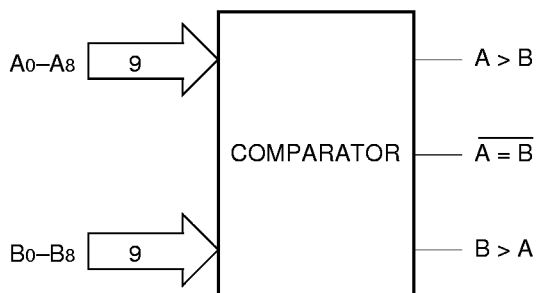
FEATURES

- 1100ps max. Propagation Delay $\overline{A = B}$
- Extended 100E V_{EE} range of -4.2V to -5.5V
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75K Ω input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E166
- Available in 28-pin PLCC package

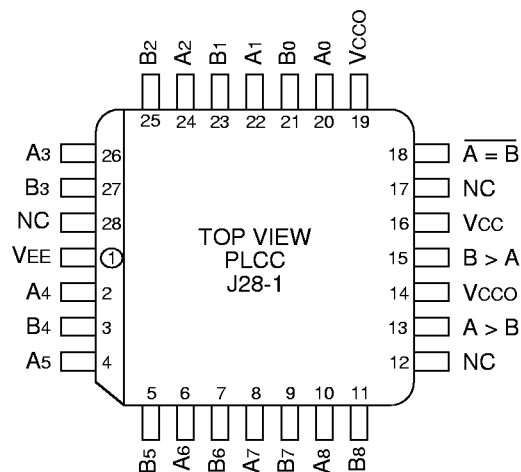
DESCRIPTION

The SY10/100E166 are 9-bit magnitude comparators designed for use in new, high-performance ECL systems. The E166 compares the binary value of two 9-bit words and indicates whether one word is greater than or equal to the other.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
A0-A8	A Data Inputs
B0-B8	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A = B}$	A Equal to B Output (active-LOW)
Vcco	Vcc to Output

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I_{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
	10E	—	113	136	—	113	136	—	113	136		
	100E	—	113	136	—	113	136	—	130	156		

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = V_{EE} (\text{Min.})$ to $V_{EE} (\text{Max.})$; $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	$T_A = 0^\circ\text{C}$			$T_A = +25^\circ\text{C}$			$T_A = +85^\circ\text{C}$			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output D to A = B D to A < B, A > B	500 500	750 850	1100 1400	500 500	750 850	1100 1400	500 500	750 850	1100 1400	ps	—
t_r t_f	Rise/Fall Time 20% to 80%	300	450	800	300	450	800	300	450	800	ps	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E166JC	J28-1	Commercial
SY10E166JCTR	J28-1	Commercial
SY100E166JC	J28-1	Commercial
SY100E166JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

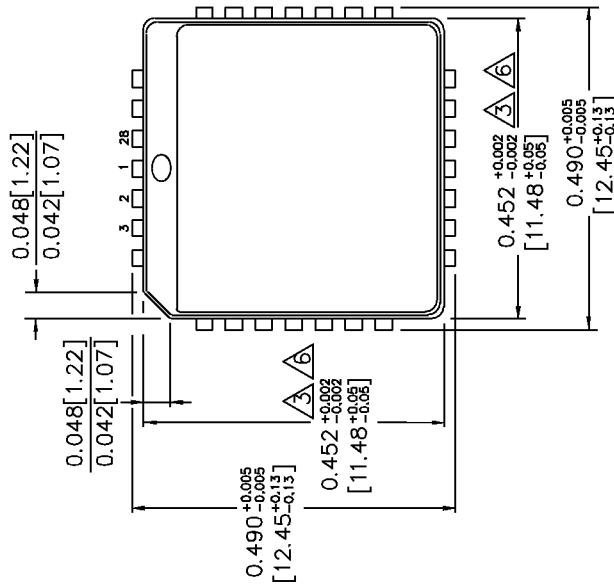
FILE/REV #: PD0008A03

PD/0008/ASCORP

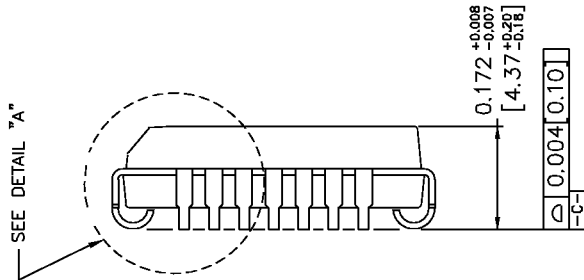
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REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450(11.43) TO 0.443(11.25). TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34855 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

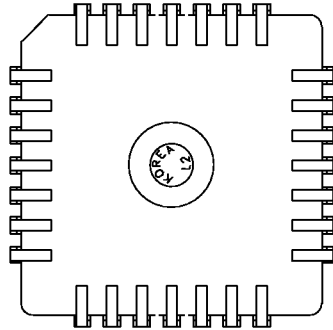
TOP VIEW



SIDE VIEW



BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



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APPROVALS	DATE	APPROVALS	DATE	SIZE	SCALE
ORIGINATOR: ERMIN G. LIRRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	28 LEAD PLCC
CHK'D: RON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			PACKAGE OUTLINE
RELEASE DATE:					THESE SPECIFICATIONS ARE THE PROPERTY OF SYNERGY SEMICONDUCTOR. ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, OR USED AS THE BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS WITHOUT WRITTEN PERMISSION.
					N/A
					REVISION
					03

FEATURES

- 1000MHz min. operating frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 800ps max. clock to output
- Single-ended outputs
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- ESD protection of 2000V
- Fully compatible with Motorola MC10E/100E167
- Available in 28-pin PLCC package

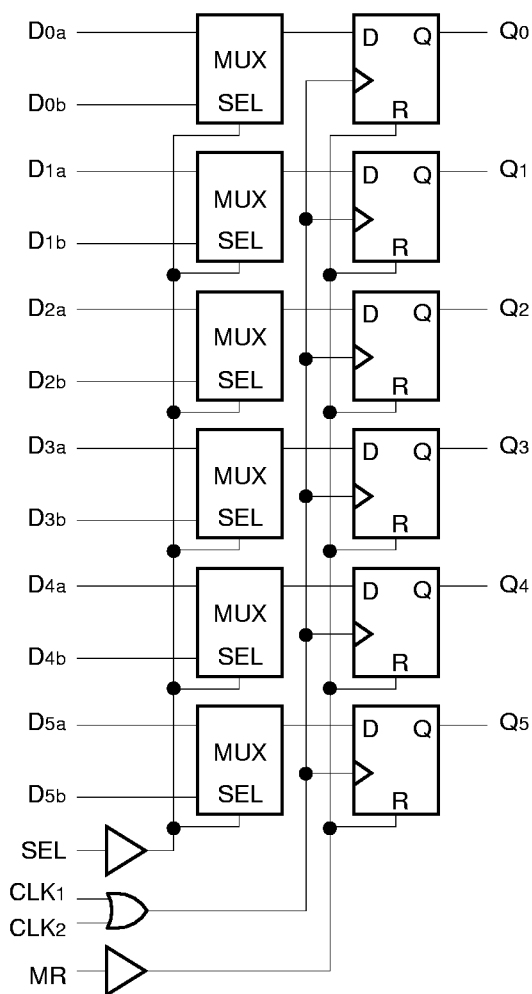
DESCRIPTION

The SY10/100E167 offer six 2:1 multiplexers followed by D flip-flops with single-ended outputs, designed for use in new, high-performance ECL systems. The Select (SEL) control allows one of the two data inputs to the multiplexer to pass through. The two external clock signals (CLK1, CLK2) are gated through a logical OR operation before use as control for the six flip-flops. The selected data are transferred to the flip-flops on the rising edge of CLK1 or CLK2 (or both).

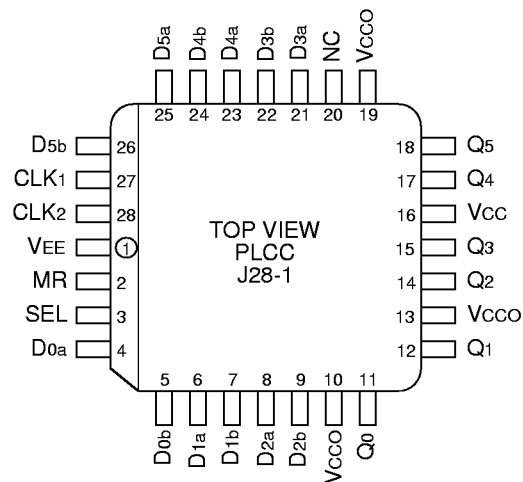
The multiplexer operation is controlled by the Select (SEL) signal which selects one of the two bits of input data at each mux to be passed through.

When a logic HIGH is applied to the Master Reset (MR) signal, it operates asynchronously to take all outputs Q to a logic LOW.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0a-D5a	Input Data a
D0b-D5b	Input Data b
SEL	Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q5	Data Outputs
VCCO	Vcc to Output