FAIRCHILD SEMICONDUCTOR™

PRELIMINARY
July 1998

NM24C00 – 512-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C00 devices are 512 bits of CMOS non-volatile electrically erasable memory. This device conforms to all specifications in the I²C™ 2-wire protocol and is designed to minimize device pin count, and simplify PC board layout requirements.

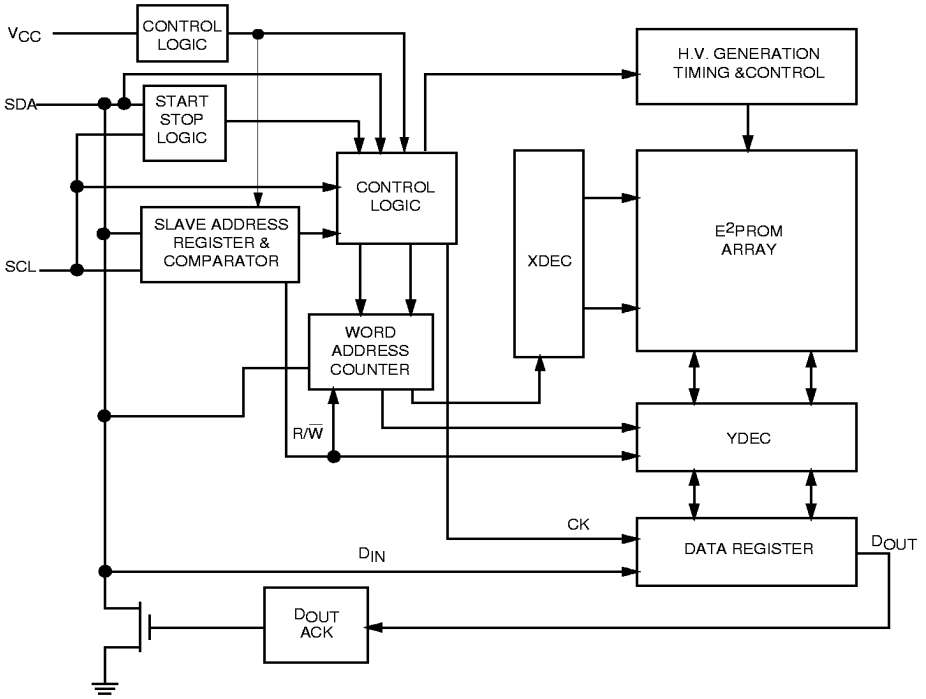
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 kHz clock frequency (F)
- 500µA active current typical
  10µA standby current typical
  1µA standby typical (L)
  0.1µA standby typical (LZ)
- I²C compatible interface
  – Provides bidirectional data transfer protocol
- Self timed write cycle
  Typical write cycle time of 6ms
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin SO and 8-pin TSSOP
- Internal ERASE/WRITE logic is disabled if V_{CC} is below 3.8V (V_{CC} = 5 ± 10%). Available on the 5V version NM24C00 (only).

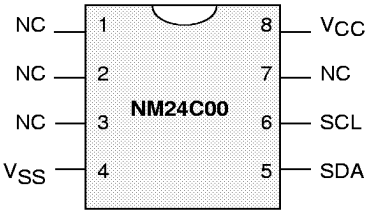
Block Diagram



DS500068-1

Connection Diagrams

SO Package (M8) and TSSOP Package (MT8)



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Top View
See Package
Number M08A and MTC8

Pin Names

V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Internal Connection
V_{CC}	Power Supply

Ordering Information

								Letter	Description
NM	24	C	XX	F	LZ	E	XX		
							Package	M8	8-pin SOIC
								MT8	8-pin TSSOP
						Temp. Range		None	0 to 70°C
								V	-40 to +125°C
								E	-40 to +85°C
					Voltage Operating Range			Blank	4.5V to 5.5V
								L	2.7V to 5.5V
								LZ	2.7V to 5.5V and <1µA Standby Current
				SCL Clock Frequency				Blank	100KHz
								F	400KHz
			Density					00	512bit
		C						C	CMOS Technology
	Interface							24	IIC - 2 Wire
NM								**NM**	**Fairchild Non-Volatile Memory**

Absolute Maximum Ratings

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	
NM24C00	0°C to +70°C
NM24C00E	-40°C to +85°C
NM24C00V	-40°C to +125°C
Positive Power Supply	
NM24C00	4.5V to 5.5V
NM24C00L	2.7V to 5.5V
NM24C00LZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB} (Note 2)	Standby Current for L Standby Current for LZ	V_{IN} = GND or V_{CC} V_{IN} = GND or V_{CC}		1 0.1	10 1	µA µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		–0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V (Note 1)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

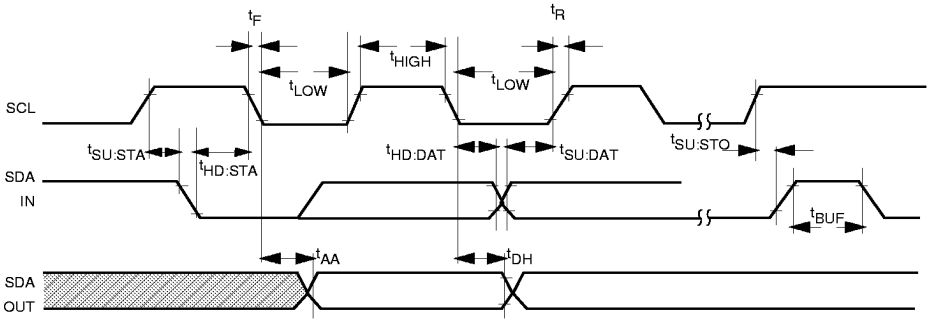
Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Read and Write Cycle Limits (Standard and Low V_{CC} Range - 2.7V-5.5V)

Symbol	Parameter	100 kHz		400kHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		µs
t_{LOW}	Clock Low Period	4.7		1.5		µs
t_{HIGH}	Clock High Period	4.0		0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		0		µs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	µs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 2)	Write Cycle Time - NM24C00 - NM24C00L, NM24C00LZ		10 15		10 15	ms

Note 2: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C00 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

BUS TIMING



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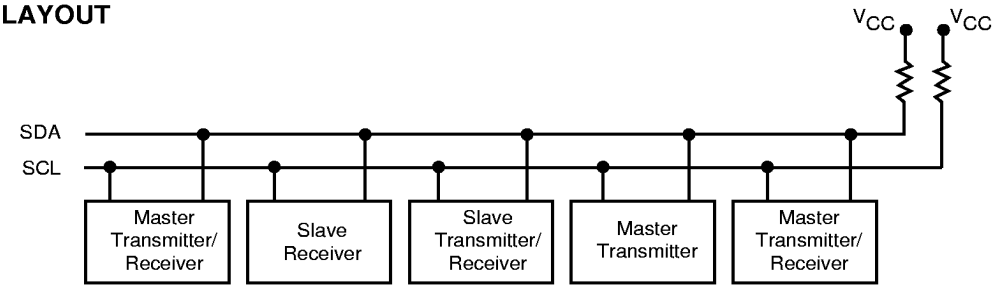
SYSTEM LAYOUT



Note 3: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7 kΩ)

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DEFINITIONS	
WORD	8 bits (byte) of data
MASTER	Any I^2C device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Pin Descriptions

SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

SDA Serial Data

This is a bi-directional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to V_{CC}.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

Noise Protection

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

Device Operation

The NM24C00 supports a bi-directional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the NM24C00 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

Bus Characteristics

The following bus protocol has been defined:

1. Data transfer may be initiated only when the bus is not busy.
2. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 1).

Bus not Busy

Both data and clock lines remain HIGH.

Start Condition

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGh determines a START condition. All commands must be preceded by a START condition.

Stop Condition

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited.

Bus Characteristics (Continued)

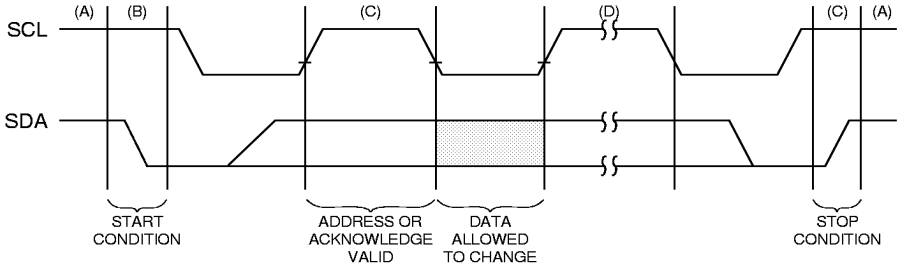
Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The NM24C00 does not generate any acknowledge bits if an internal programming cycle is in progress,

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that ha been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition (Figure 2).

DATA TRANSFER SEQUENCE ON THE SERIAL BUS (Figure 1)



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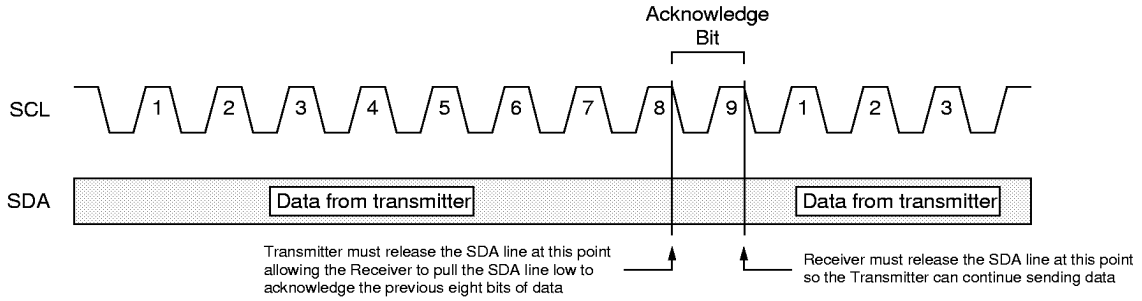
ACKNOWLEDGE TIMING (Figure 2)



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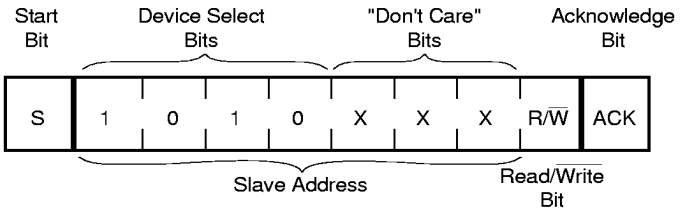
Device Addressing

After generating a START condition, the bus master transmits a control byte consisting of a slave address and an R/$\overline{W}$ bit that indicates what type of operation is to be performed. The slave address for the NM24C00 consists of a 4-bit device code (1010) followed by three "don't care" bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected (Figure 3). The NM24C00 monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

CONTROL BYTE FORMAT (FIGURE 3)



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Write Operations

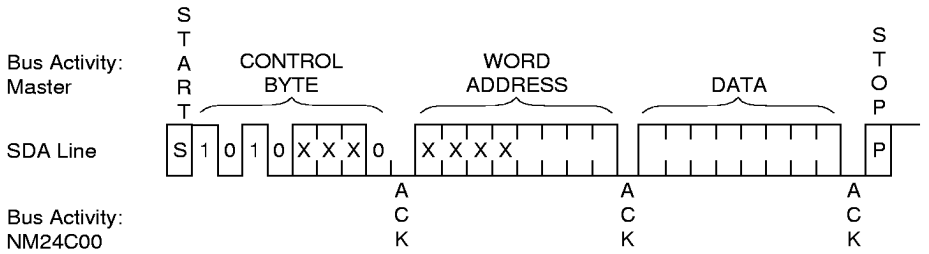
Byte Write

Following the start signal from the master, the device code (4 bits), the "don't care" bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after is has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the NM24C00. Only the lower six address bits are used by the device, and the upper four bits are "don't cares." The NM24C00 will acknowledge the address byte and the master device will then transmit the data word to be written into the addressed memory location. The NM24C00 acknowledges again and the master generates a stop condition. This intiates the internal write cycle, and during this time the NM24C00 will not generate acknowledge signals (Figure 4) . After a byte write command, the interal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a fill eight data bits have been transmitted, then the write command will abort and no data will be written. The NM24C00M8/MT8 employs a V_{CC} threshold detector circuit which disables the internal programming circuit if V_{CC} is below 3.8V.

Low V_{CC} Lockout

NM24C00 provides data security against inadvertent writes that could potentially happen during the time the device is being powered on, powered down and brown out conditions by monitoring the V_{CC} voltage during a write cycle. Whenever a write cycle is started, the built-in circuitry starts to monitor the V_{CC} level throughout the duration of the write command sequence until the master issues the required STOP condition to start the actual internal write operation. If the sensed V_{CC} voltage is below 3.8V at any point during this monitoring period, the device prohibits the write operation and does not generate the ACK pulse. This low V_{CC} lockout feature is only available for standard 5V device.

BYTE WRITE (FIGURE 4)



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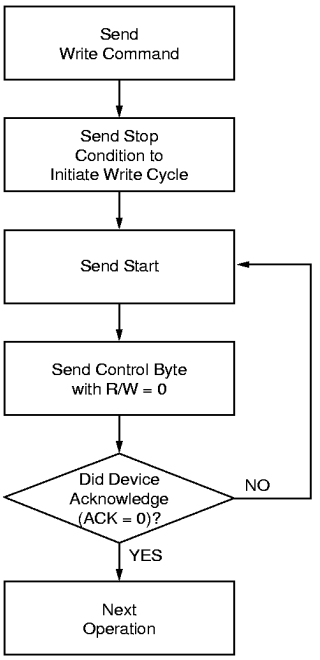
X = "Don't Care" Bit

Acknowledge Polling

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete,. then the device will return the ACK and the master can then proceed with the next read or write command. See Figure 5 for flow diagram.

ACKNOWLEDGE POLLING FLOW (FIGURE 5)



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Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read

The NM24C00 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read operation was tp address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 6).

Random Read

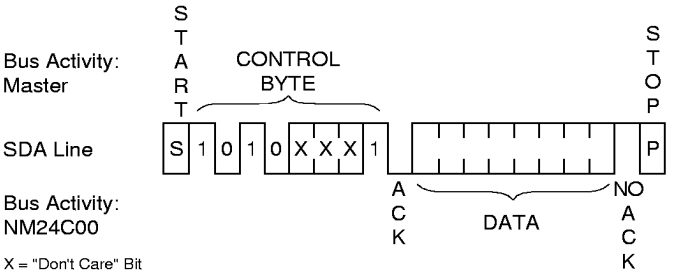
Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the device as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The NM24C00 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the device discontinues transmission (Figure 7). After this command, the internal address counter will point to the address location following the one that was just read.

Sequential Read

Sequential reads are initiated in the same was as a random read except that after the device transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the device to transmit the next sequentially addressed 8-bit word (Figure 8).

To provide sequential reads the NM24C00 contains an internal address pointer which is incrmented by one at the completion of each read operation. This address pointer allows the entire memory to be serially read during one operation.

CURRENT ADDRESS READ (Figure 6)



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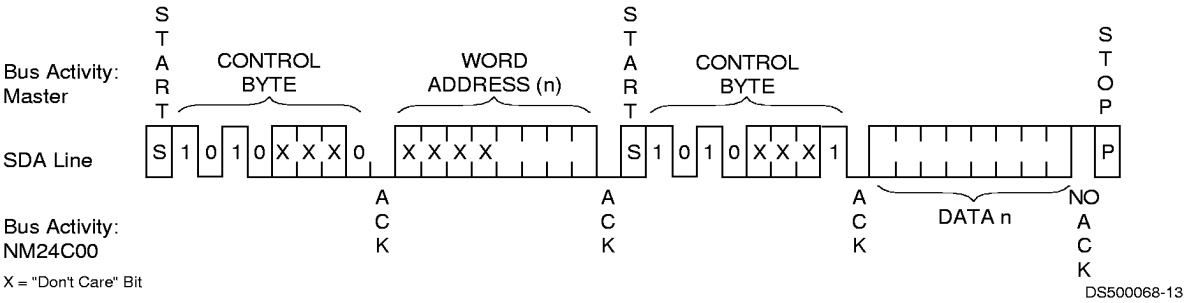
RANDOM READ (Figure 7)



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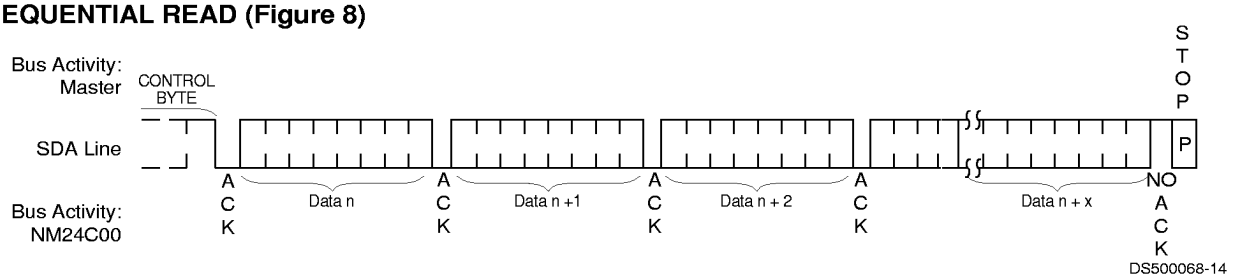
SEQUENTIAL READ (Figure 8)



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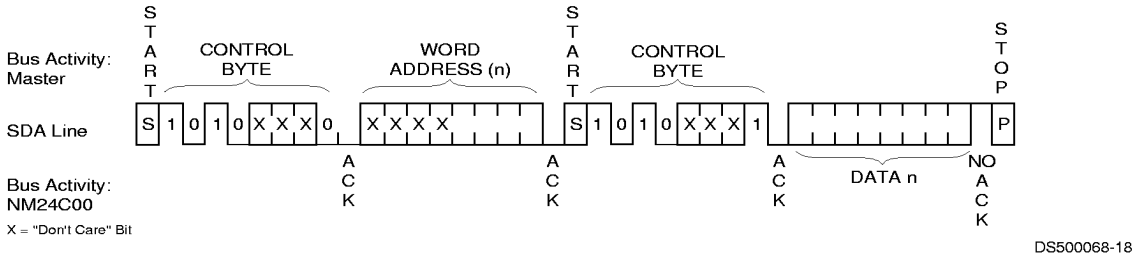
Read Operations (Continued)

Random Read (Figure 9)



X = "Don't Care" Bit

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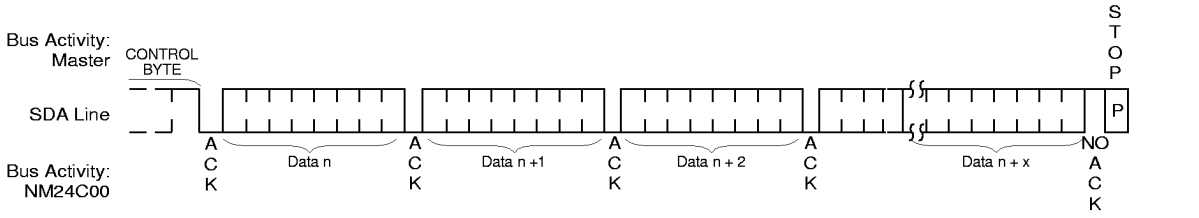
Sequential Read (Figure 10)



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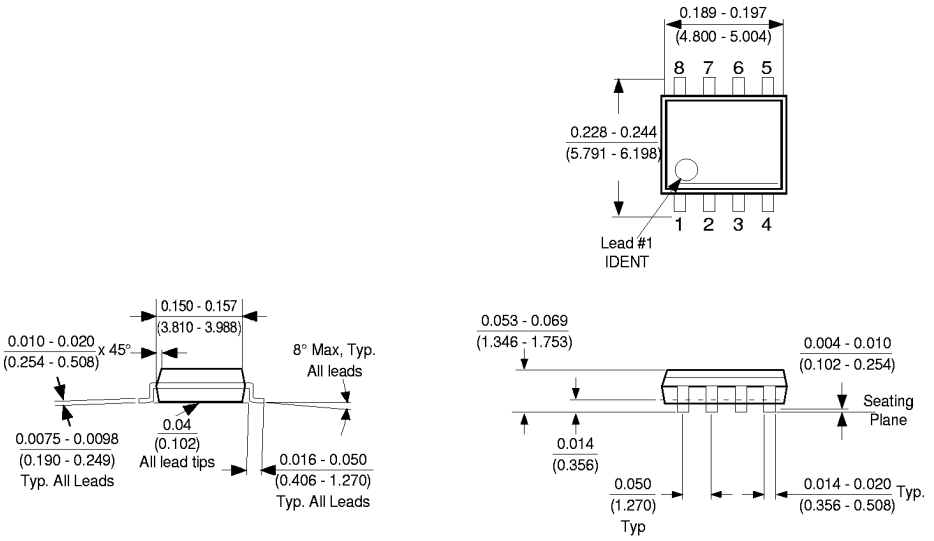
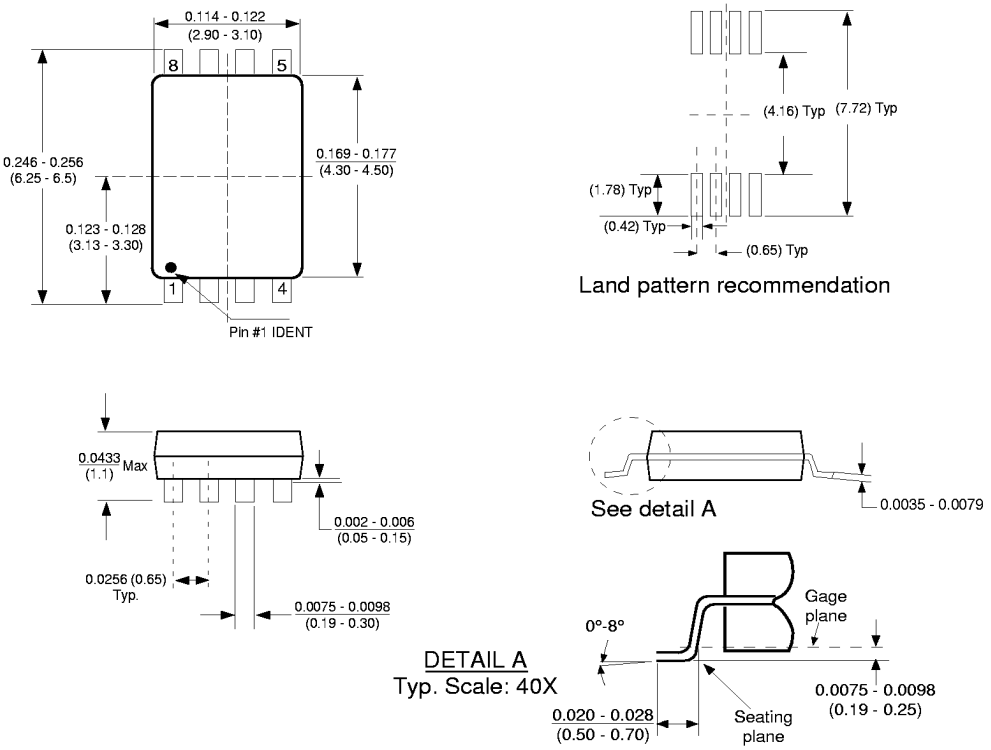
Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin Molded Small Outline Package (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted



Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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