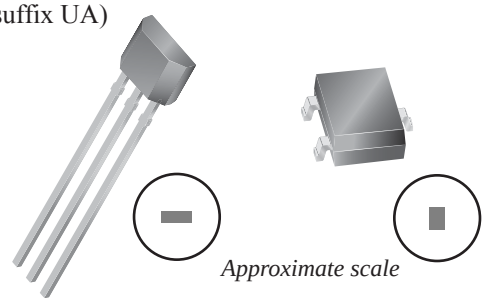
5 V Field-Programmable Linear Hall Effect Sensor IC with 3 V Supply Functionality, Analog Output, and Miniature Package Options

Features and Benefits

- Low power consumption using 3 V supply
- Factory programmed sensitivity temperature coefficient (0.13%/°C nominal)
- Programmability at end-of-line
- Ratiometric sensitivity, quiescent voltage output, and clamps for interfacing with application DAC
- Temperature-stable quiescent voltage output and sensitivity
- Precise recoverability after temperature cycling
- Output voltage clamps provide short circuit diagnostic capabilities
- Wide ambient temperature range: –40°C to 150°C
- Resistant to mechanical stress
- Miniature package options

Packages

3-pin ultramini SIP
1.5 mm × 4 mm × 3 mm
(suffix UA)



Approximate scale

Description

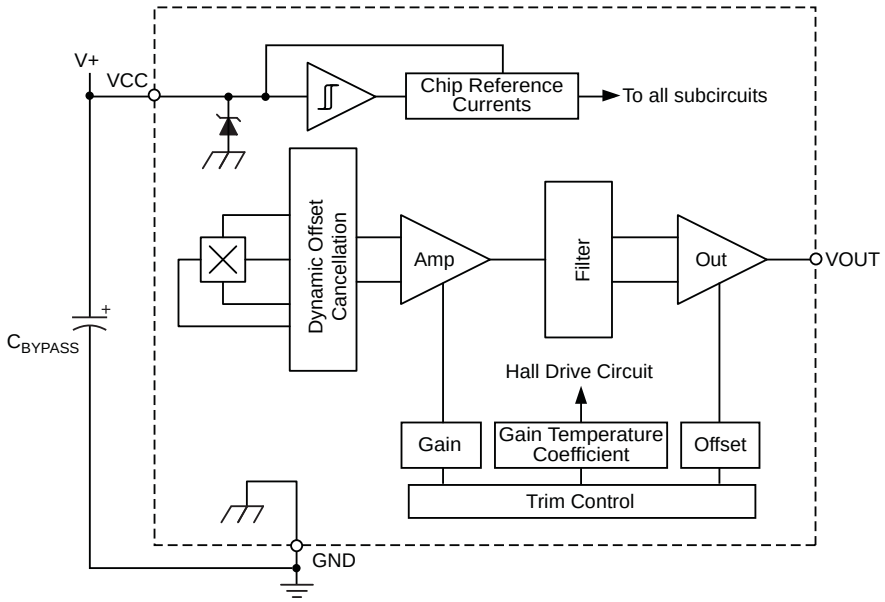
The Allegro® A1386 programmable, linear, Hall effect sensor IC is designed for low power, high accuracy, and small package size applications. The accuracy of this device is enhanced via programmability on the output pin for end-of-line optimization without the added complexity and cost of a fully programmable device.

The A1386 has two operating modes, normal and low power. In normal operation mode the A1386 operates much like its predecessors, the A1381, A1382, A1383, and A1384, as a highly accurate, user-programmable linear sensor IC with a ratiometric output. In low power mode, the device actually disengages some internal components in order to reduce power consumption. Although the accuracy of the device is substantially reduced during low power operation, it remains effective as a detector of magnetic regions (such as north and south poles on a rotating ring magnet). This unique feature allows the device to be used in systems that are put to sleep, during which time there may be only 3 V available, or in applications that have start-up conditions where the available supply voltage may drop below 4.5 V for a period of time.

This ratiometric Hall effect device provides a voltage output that is proportional to the applied magnetic field over the entire

Continued on the next page…

Functional Block Diagram



Description (continued)

2.7 to 5.5 V supply operating region. Both the quiescent voltage output and magnetic sensitivity are user adjustable. The quiescent voltage output can be set to approximately 50% of the supply voltage, and the sensitivity adjusted between 1.90 and 3.50 mV/G for V_{CC} = 5 V. The sensitivity temperature coefficient is programmed at the factory, at 0.13%/°C nominal, to compensate for Neodymium-style magnets. The features of this linear device make it ideal for the high accuracy requirements of automotive and industrial applications. Performance is guaranteed over an extended temperature range, –40°C to 150°C.

Each device contains a BiCMOS monolithic circuit that integrates a Hall element, temperature-compensating circuitry to reduce the intrinsic sensitivity drift of the Hall element, a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary dynamic offset cancellation technique.

The A1386 device is provided in a 3-pin ultramini single-in-line package (UA suffix), and a 3-pin surface mount SOT-23W package (LH suffix). Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Selection Guide

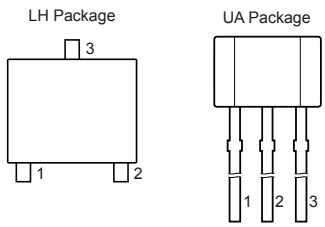
Part Number	Packing*	Package	T_A (°C)
A1386LLHLT-T	Tape and reel, 3000 pieces/reel	Surface mount	–40 to 150
A1386LUA-T	Bulk bag, 500 pieces/bag	Through hole	

*Contact Allegro for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		28	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUT(SOURCE)}$	VOUT to GND	8	mA
Output Sink Current	$I_{OUT(SINK)}$	VCC to VOUT	2	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	T_J(max)		165	°C

Pin-out Diagrams



Terminal List Table

Number		Name	Description
LH	UA		
1	1	VCC	Input power supply; use bypass capacitor to connect to ground
3	2	GND	Ground
2	3	VOUT	Output signal

OPERATING CHARACTERISTICS, valid over full operating temperature range, T_A; C_{BYPASS}= 0.1 µF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units[1]
Electrical Characteristics						
Supply Voltage	$V_{CC(NORM)}$		4.5	–	5.5	V
	$V_{CC(LOWPWR)}$		2.8	–	3.2	V
Supply Voltage Turn On Time	t_{VCC}		–	–	10	ms
Operation Mode Threshold Voltage[2]	V_{THRESH}	$V_{CC(LOWPWR)} \rightarrow V_{CC(NORM)}$	–	4.1	–	V
		$V_{CC(NORM)} \rightarrow V_{CC(LOWPWR)}$	–	3.7	–	V
Supply Zener Clamp Voltage	V_Z	T_A = 25°C, I_{CC} = 11 mA	6	8.3	–	V
Supply Current	I_{CC}	$V_{CC} = V_{CC(NORM)}$, $R_{L(PULLDWN)}$ = 10 kΩ	–	6.4	8	mA
		$V_{CC} = V_{CC(LOWPWR)}$, $R_{L(PULLDWN)}$ = 10 kΩ	–	–	4	mA
Power-On Time[2]	t_{PO}	$V_{CC} = V_{CC(NORM)}$, T_A = 25°C, C_{BYPASS} = open, C_L (of test probe) = 4.7 nF	–	30	–	µs
		$V_{CC} = V_{CC(LOWPWR)}$, T_A = 25°C, C_{BYPASS} = open, C_L (of test probe) = 4.7 nF	–	50	–	µs
Internal Bandwidth	BW_i	Small signal –3 dB, 100 $G_{(p-p)}$, magnetic input signal	–	20	–	kHz
Chopping Frequency[3]	f_C	T_A = 25°C	–	200	–	kHz
Output Characteristics						
VOUT Voltage Clamp[4]	$V_{CLP(HIGH)}$	V_{CC} = 5 V, T_A = 25°C, B = 750 G, Sens = 3.3 mV/G, $R_{L(PULLDWN)}$ = 10 kΩ	4.39	4.5	4.58	V
		V_{CC} = 3 V, T_A = 25°C, B = 750 G, Sens = 3.3 mV/G, $R_{L(PULLDWN)}$ = 10 kΩ	2.62	2.7	2.78	V
	$V_{CLP(LOW)}$	V_{CC} = 5 V, T_A = 25°C, B = –750 G, Sens = 3.3 mV/G, $R_{L(PULLDWN)}$ = 10 kΩ	0.39	0.5	0.58	V
		V_{CC} = 3 V, T_A = 25°C, B = –750 G, Sens = 3.3 mV/G, $R_{L(PULLDWN)}$ = 10 kΩ	0.19	0.3	0.37	V
VOUT Noise (peak to peak)	$V_{N(p-p)}$	$V_{CC} = V_{CC(NORM)}$, T_A = 25°C, C_L = 4.7 nF, Sens = 3.3 mV/G, no external filter	–	18	–	mV
		$V_{CC} = V_{CC(LOWPWR)}$, T_A = 25°C, C_L = 4.7 nF, Sens = 1.75 mV/G, no external filter	–	18	–	mV
VOUT DC Output Resistance	R_{OUT}		–	< 1	–	Ω
VOUT Load Capacitance	C_L	VOUT to GND	–	–	4.7	nF
VOUT Load Resistance	$R_{L(PULLDWN)}$	VOUT to GND	10	–	–	kΩ
VOUT Output Slew Rate	SR	$V_{CC} = V_{CC(NORM)}$, C_L = 4.7 nF	–	140	–	V/ms
		$V_{CC} = V_{CC(LOWPWR)}$, C_L = 4.7 nF	–	50	–	V/ms

Continued on the next page...

OPERATING CHARACTERISTICS (continued), valid over full operating temperature range, T_A; C_{BYPASS}= 0.1 µF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units[1]
Pre-Programming Targets						
Pre-Programming Quiescent Voltage Output	$V_{OUT(Q)PRE}$	V_{CC} = 3 V, B = 0 G, T_A = 25°C	1.34	–	1.53	V
		V_{CC} = 5 V, B = 0 G, T_A = 25°C	–	2.5	–	V
Pre-Programming Sensitivity	$Sens_{PRE}$	V_{CC} = 3 V, T_A = 25°C	–	–	1.14	mV/G
		V_{CC} = 5 V, T_A = 25°C	–	1.4	–	mV/G
Quiescent Voltage Output Programming						
Guaranteed Quiescent Voltage Output Range[4,5,6]	$V_{OUT(Q)}$	V_{CC} = 5 V, B = 0 G, T_A = 25°C	2.4	–	2.6	V
Quiescent Voltage Output Programming Bits			–	5	–	bit
Average Quiescent Voltage Output Step Size[7,8]	$Step_{VOUT(Q)}$	V_{CC} = 5 V	12	16	18	mV
Quiescent Voltage Output Programming Resolution[9]	$Err_{PGVOUT(Q)}$	V_{CC} = 5 V	–	$Step_{VOUT(Q)}$ × ±0.5	–	mV
Sensitivity Programming						
Guaranteed Sensitivity Range [4,5,10]	Sens	V_{CC} = 5 V, T_A = 25°C	1.9	–	3.3	mV/G
Sensitivity Programming Bits			–	6	–	bit
Average Sensitivity Step Size[7,8]	$Step_{SENS}$	V_{CC} = 5 V, T_A = 25°C	30	40	50	µV/G
Sensitivity Programming Resolution[9]	Err_{PGSENS}	V_{CC} = 5 V, T_A = 25°C	–	$Step_{SENS}$ × ±0.5	–	mV/G
Lock Bit Programming						
Overall Programming Lock Bit	LOCK		–	1	–	bit
Factory Programmed Sensitivity Temperature Coefficient						
Factory Programmed Sensitivity Temperature Coefficient Target	$TC_{SENS(TGT)}$	V_{CC} = 5 V, T_A = 150°C	–	0.13	–	%/°C
Factory Programmed Sensitivity Temperature Coefficient Range[11]	TC_{SENS}		0.10	–	0.16	%/°C
Error Components						
Linearity Sensitivity Error[2]	Lin_{ERR}	V_{CC} = $V_{CC(NORM)}$	–	±1.5	–	%
		V_{CC} = $V_{CC(LOWPWR)}$	–	±2	–	%
Symmetry Sensitivity Error[2]	Sym_{ERR}	V_{CC} = $V_{CC(NORM)}$	–	±1.5	–	%
		V_{CC} = $V_{CC(LOWPWR)}$	–	±2	–	%
Ratiometry Quiescent Voltage Output Error[2,12]	$Rat_{ERRVOUT(Q)}$	V_{CC} = $V_{CC(NORM)}$	–	±1.5	–	%
		V_{CC} = $V_{CC(LOWPWR)}$	–	±2.5	–	%
Ratiometry Sensitivity Error[2,13]	$Rat_{ERRSENS}$	V_{CC} = $V_{CC(NORM)}$	–	±1.5	–	%
		V_{CC} = $V_{CC(LOWPWR)}$	–	±2.5	–	%
Ratiometry Clamp Error[2,13]	Rat_{ERRCLP}	V_{CC} = $V_{CC(NORM)}$, T_A = 25°C	–	±1.5	–	%
		V_{CC} = $V_{CC(LOWPWR)}$, T_A = 25°C	–	±2.5	–	%

Continued on the next page...

OPERATING CHARACTERISTICS (continued), valid over full operating temperature range, T_A; C_{BYPASS}= 0.1 µF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units[1]
Drift Characteristics						
Quiescent Voltage Output Drift Through Temperature Range[2]	$\Delta V_{OUT(Q)}$	$V_{CC} = V_{CC(NORM)}$, Sens = 3.3 mV/G, T_A = 25°C to 150°C	–	–	±35	mV
		$V_{CC} = V_{CC(LOWPWR)}$, Sens = 1.75 mV/G, T_A = 25°C to 150°C	–	±35	–	mV
Maximum Sensitivity Drift Through Temperature Range[14,15]	$\Delta Sens_{TC}$	$V_{CC} = V_{CC(NORM)}$	–	±3	–	%
		$V_{CC} = V_{CC(LOWPWR)}$	–	±5	–	%
Sensitivity Drift Due to Package Hysteresis[2,15]	$\Delta Sens_{PKG}$	T_A = 25°C; after temperature cycling	–	±2	–	%

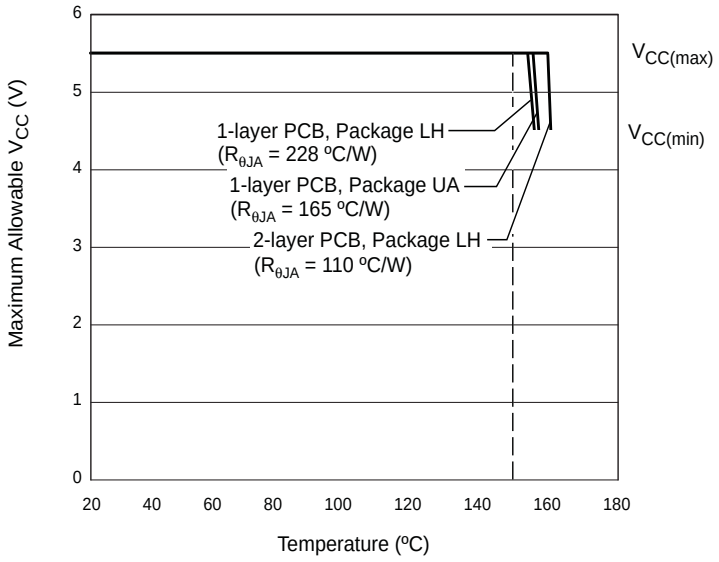
[1]1G (gauss) = 0.1 mT (millitesla).
[2]See Characteristic Definitions section.
[3]f_C varies up to approximately ± 20% over the full operating ambient temperature range, T_A, and process.
[4]Sens, $V_{OUT(Q)}$, $V_{CLP(LOW)}$, and $V_{CLP(HIGH)}$ scale with V_{CC} due to ratiometry.
[5]For optimal device accuracy in the $V_{CC(NORM)}$ operating range, the device should be programmed with V_{CC} = 5 V.
[6]$V_{OUT(Q)}$(max) is the value available with all programming fuses blown (maximum programming code set). The $V_{OUT(Q)}$ range is the total range from $V_{OUT(Q)init}$ up to and including $V_{OUT(Q)}$(max). See Characteristic Definitions section.
[7]Step size is larger than required, to account for manufacturing spread. See Characteristic Definitions section.
[8]Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.
[9]Overall programming value accuracy. See Characteristic Definitions section.
[10]Sens(max) is the value available with all programming fuses blown (maximum programming code set). Sens range is the total range from $Sens_{init}$ up to and including Sens(max). See Characteristic Definitions section.
[11]Factory programmed at 150°C and calculated relative to 25°C.
[12]Percent change from actual value at V_{CC} = 3 V or V_{CC} = 5 V, for a given temperature, over the guaranteed supply voltage operating range.
[13]Percent change from actual value at V_{CC} = 3 V or V_{CC} = 5 V, with T_A = 25°C, over the guaranteed supply voltage operating range.
[14]Sensitivity drift from expected value of V_{OUT} at T_A , after programming TC_{SENS}. See Characteristic Definitions section.
[15]Guaranteed by design only. Parameter is not tested in production flow.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

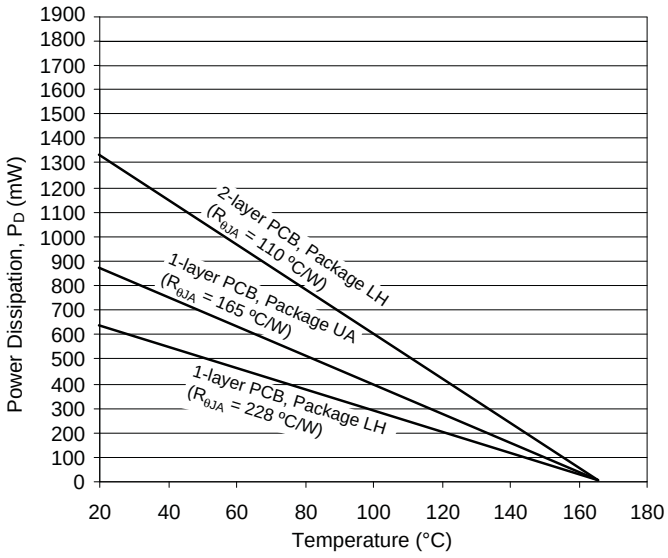
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W

*Additional thermal information available on Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



Characteristic Definitions

Supply Voltage Turn On Time To ensure that the internal components of the A1386 device are initialized to their proper values, the supply voltage, V_{CC}, must be powered up within a specified time interval. Supply Voltage Turn On Time, t_{VCC}, is defined as the time it takes for the supply voltage to transition from 10% to 90% of its steady state value.

Operating Mode Threshold The A1386 has two modes of operation, *Normal* and *Low Power*. In Low Power mode, certain components of the device are disengaged to limit the current consumption of the device. As a result, the overall device accuracy is limited. In Normal mode, all components are fully functional.

The V_{CC} supply level is used by the device to determine the mode of operation. The threshold voltage, V_{THRESH}, is the V_{CC} threshold voltage required to switch from Low Power operation to Normal operation ($V_{CC(LOWPWR)} \rightarrow V_{CC(NORM)}$) or from Normal operation to Low Power operation ($V_{CC(NORM)} \rightarrow V_{CC(LOWPWR)}$). A region of hysteresis exists between the Normal V_{CC} operational range and the Low Power V_{CC} operational range, as shown in figure 1. At the initial power up, the device remains in the Low Power operating mode until reaching the $V_{CC(LOWPWR)} \rightarrow V_{CC(NORM)}$ V_{THRESH} voltage.

Power-On Time When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO}, is defined as: the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in figure 2.

Quiescent Voltage Output In the quiescent state (no significant magnetic field: B = 0 G), the output, $V_{OUT(Q)}$, has a constant ratio to the supply voltage, V_{CC} , throughout the entire operating ranges of V_{CC} and ambient temperature, T_A.

Guaranteed Quiescent Voltage Output Range The quiescent voltage output, $V_{OUT(Q)}$, can be programmed around its nominal value of 2.5 V, within the guaranteed quiescent voltage range limits, $V_{OUT(Q)}$(min) and $V_{OUT(Q)}$(max). The available guaranteed

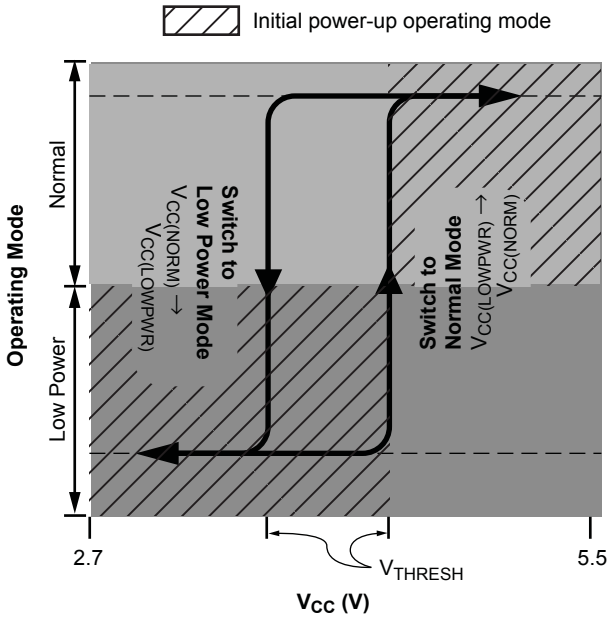


Figure 1. Operating Mode relationship to V_{CC}, with V_{CC} shown over the full operating range

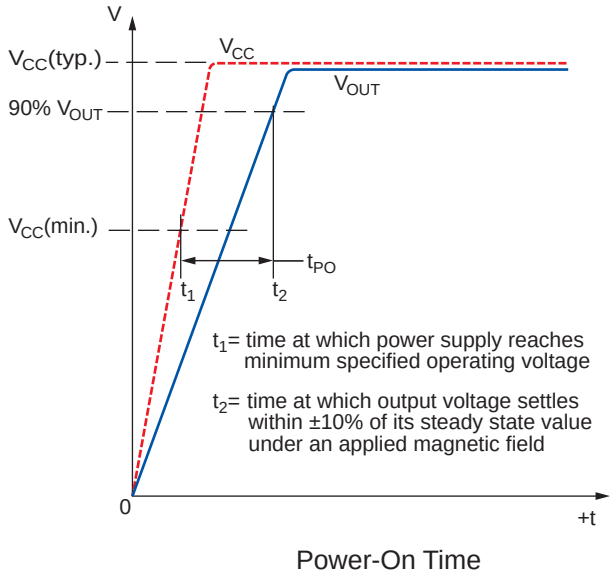


Figure 2. V_{CC} and V_{OUT} during power-on time interval

programming range for $V_{OUT(Q)}$ falls within the distributions of the initial, $V_{OUT(Q)init}$, and the maximum programming code for setting $V_{OUT(Q)}$, as shown in figure 3.

Average Quiescent Voltage Output Step Size The average quiescent voltage output step size for a single device is determined using the following calculation:

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)init}}{2^n - 1} . \quad (1)$$

where:

n is the number of available programming bits in the trim range,

$2^n - 1$ is the value of the maximum programming code in the range, and

$V_{OUT(Q)maxcode}$ is the quiescent voltage output at code $2^n - 1$.

Quiescent Voltage Output Programming Resolution The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) . \quad (2)$$

Quiescent Voltage Output Drift Through Temperature Range Due to internal component tolerances and thermal considerations, the quiescent voltage output, $V_{OUT(Q)}$, may drift from its nominal value over the operating ambient temperature, T_A. For purposes of specification, the Quiescent Voltage Output Drift Through Temperature Range, $\Delta V_{OUT(Q)}$ (mV), is defined as:

$$\Delta V_{OUT(Q)} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} . \quad (3)$$

$V_{OUT(Q)}$ should be calculated using the actual measured values of $V_{OUT(Q)(TA)}$ and $V_{OUT(Q)(25°C)}$, rather than programming target values.

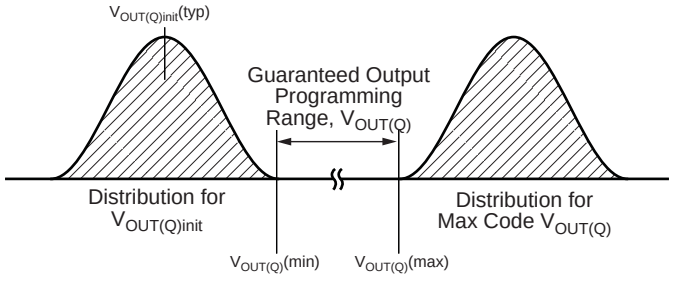


Figure 3. Relationship of the guaranteed quiescent output voltage and overall $V_{OUT(Q)}$ values.

Sensitivity The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG} , \quad (4)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity Temperature Coefficient Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{Sens} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\% \right) \left(\frac{1}{T2 - T1} \right) , \quad (5)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = Sens_{T1} \times [100\% + TC_{SENS} (T_A - T1)] . \quad (6)$$

$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ and TC_{SENS} rather than programming target values.

Sensitivity Drift Through Temperature Range Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range, T_A. For purposes of specification, the sensitivity drift through temperature range, $\Delta Sens_{TC}$, is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{TA} - Sens_{EXPECTED(TA)}}{Sens_{EXPECTED(TA)}} \times 100\% . \quad (7)$$

Sensitivity Drift Due to Package Hysteresis Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling.

For purposes of specification, the sensitivity drift due to package hysteresis, $\Delta Sens_{PKG}$, is defined as:

$$\Delta Sens_{PKG} = \frac{Sens_{(25°C)2} - Sens_{(25°C)1}}{Sens_{(25°C)1}} \times 100\% \quad , \qquad (8)$$

where $Sens_{(25°C)1}$ is the programmed value of sensitivity at T_A = 25°C, and $Sens_{(25°C)2}$ is the value of sensitivity at T_A = 25°C, but after temperature cycling T_A up to 150°C, down to –40°C, and back to up 25°C.

Linearity Sensitivity Error The A1386 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity error (%) is measured and defined as:

$$Lin_{ERRPOS} = \left(1 - \frac{Sens_{BPOS2}}{Sens_{BPOS1}}\right) \times 100\% \quad ,$$

$$Lin_{ERRNEG} = \left(1 - \frac{Sens_{BNEG2}}{Sens_{BNEG1}}\right) \times 100\% \quad , \qquad (9)$$

where:

$$Sens_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \qquad (10)$$

and B_{POSx} and B_{NEGx} are positive and negative magnetic fields, with respect to the quiescent voltage output such that $|B_{POS2}| > |B_{POS1}|$ and $|B_{NEG2}| > |B_{NEG1}|$. Then:

$$Lin_{ERR} = \max(Lin_{ERRPOS}, Lin_{ERRNEG}) \quad . \qquad (11)$$

Symmetry Sensitivity Error The magnetic sensitivity of the A1386 device is constant for any two applied magnetic fields of equal magnitudes and opposite polarities.

Symmetry error, Sym_{ERR} (%), is measured and defined as:

$$Sym_{ERR} = \left(1 - \frac{Sens_{BPOS}}{Sens_{BNEG}}\right) \times 100\% \quad , \qquad (12)$$

where $Sens_{Bx}$ is as defined in equation 10, and B_{POS} and B_{NEG} are positive and negative magnetic fields such that $|B_{POS}| = |B_{NEG}|$.

Ratiometry Error The A1386 device features a ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, magnetic sensitivity, Sens, and clamp voltages, $V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$, are proportional to the supply voltage, V_{CC}. In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in quiescent voltage output, $Rat_{ERRVOUT(Q)}$ (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (13)$$

The ratiometric error in magnetic sensitivity, $Rat_{ERRSens}$ (%), for a given supply voltage, V_{CC}, is defined as:

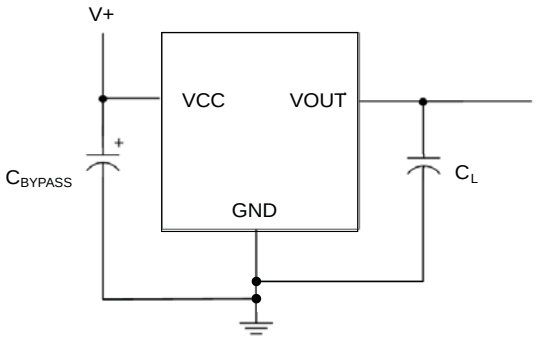
$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (14)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage, V_{CC}, is defined as:

$$Rat_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (15)$$

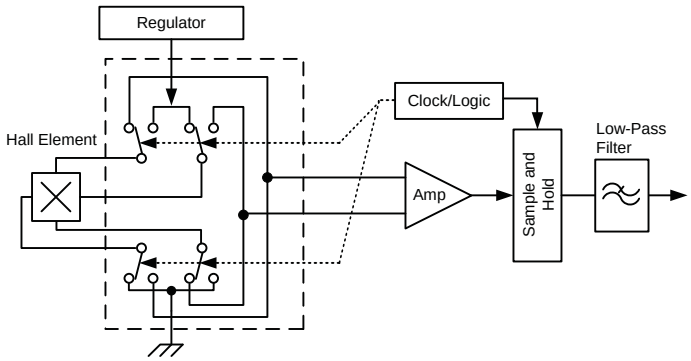
where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Typical Application Drawing



Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at base band, while the DC offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. The chopper stabilization technique uses a 200 kHz high frequency clock. For the demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and Precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Chopper Stabilization Technique

Programming Guidelines

Overview

Programming is accomplished by sending a series of input voltage pulses serially through the VOUT pin of the device. A unique combination of different voltage level pulses controls the internal programming logic of the device to select a target programmable parameter and change its value. There are two programming pulses, referred to as a *high* voltage pulse, V_{PH}, consisting of a $V_{P(LOW)} - V_{P(HIGH)} - V_{P(LOW)}$ sequence and a *mid* voltage pulse, V_{PM}, consisting of a $V_{P(LOW)} - V_{P(MID)} - V_{P(LOW)}$ sequence.

The A1386 features Try mode, Blow mode, and Lock mode:

- In Try mode, the value of a single programmable parameter may be set and measured. The parameter value is stored temporarily, and resets after cycling the supply voltage. Note that other parameters cannot be accessed simultaneously in this mode.
- In Blow mode, the value of a single programmable parameter may be permanently set by blowing solid-state fuses internal to the device. Additional parameters may be blown sequentially.
- In Lock mode, a device-level fuse is blown, blocking the further programming of all parameters.

The programming sequence is designed to help prevent the device from being programmed accidentally; for example, as a result of noise on the supply line.

Although any programmable variable power supply can be used to generate the pulse waveforms, Allegro highly recommends using the Allegro Sensor Evaluation Kit, available on the Allegro website On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

Definition of Terms

Register. The section of the programming logic that controls the choice of programmable modes and parameters.

Bit Field. The internal fuses unique to each register, represented as a binary number. Incrementing the bit field of a particular register causes its programmable parameter to change, based on the internal programming logic.

Key. A series of V_{PM} voltage pulses used to select a register, with a value expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as key 1, or bit 0.

Code. The number used to identify the combination of fuses activated in a bit field, expressed as the decimal equivalent of the binary value. The LSB of a bit field is denoted as code 1, or bit 0.

Addressing. Incrementing the bit field code of a selected register by serially applying a pulse train through the VOUT pin of the device. Each parameter can be measured during the addressing process, but the internal fuses must be blown before the programming code (and parameter value) becomes permanent.

Fuse Blowing. Applying a V_{PH} voltage pulse of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset.

Blow Pulse. A V_{PH} voltage pulse of sufficient duration at the $V_{P(HIGH)}$ level to blow the addressed fuse.

Cycling the Supply. Powering-down, and then powering-up the supply voltage. Cycling the supply is used to clear the programming settings in Try mode.

Programming Pulse Requirements, Protocol at T_A = 25°C

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Units
Programming Voltage	$V_{P(LOW)}$	Measured at the VOUT pin.	-	-	5.5	V
	$V_{P(MID)}$		14	15	16	V
	$V_{P(HIGH)}$		26	27	28	V
Programming Current	I_P	Minimum supply current required to ensure proper fuse blowing. In addition, a minimum capacitance, C_{BLOW} = 0.1 µF, must be connected between the VOUT and GND pins during programming to provide the current necessary for fuse blowing.	300	-	-	mA
Pulse Width	$t_{OFF(HIGH)}$	Duration at $V_{P(LOW)}$ level following a $V_{P(HIGH)}$ level.	30	-	-	µs
	$t_{OFF(MID)}$	Duration at $V_{P(LOW)}$ level following a $V_{P(MID)}$ level.	5	-	-	µs
	$t_{ACTIVE(HIGH)}$	Duration of $V_{P(HIGH)}$ level for V_{PH} pulses during key/code selection.	30	-	-	µs
	$t_{ACTIVE(MID)}$	Duration of $V_{P(MID)}$ level for V_{PH} pulses during key/code selection.	15	-	-	µs
	t_{BLOW}	Duration at $V_{P(HIGH)}$ level for fuse blowing.	30	-	-	µs
Pulse Rise Time	t_{Pr}	Rise time required for transitions from $V_{P(LOW)}$ to either $V_{P(MID)}$ or $V_{P(HIGH)}$.	1	-	100	µs
Pulse Fall Time	t_{Pf}	Fall time required for transitions from $V_{P(HIGH)}$ to either $V_{P(MID)}$ to $V_{P(LOW)}$.	1	-	100	µs

Programming Procedures

Parameter Selection

Each programmable parameter can be accessed through a specific register. To select a register, a sequence of voltage pulses consisting of a V_{PH} pulse, a series of V_{PM} pulses, and a V_{PH} pulse (with no V_{CC} supply interruptions) must be applied serially to the VOUT pin. The number of V_{PM} pulses is called the *key*, and uniquely identifies each register. The pulse train used for selection of the first register, key 1, is shown in figure 4.

The A1386 has two registers that select among the three programmable parameters:

- Register 1:
  Sensitivity, Sens
- Register 2:
  Quiescent voltage output, $V_{OUT(Q)}$
  Overall device locking, LOCK

Bit Field Addressing

After a programmable parameter has been selected, a V_{PH} pulse transitions the programming logic into the bit field addressing state. Applying a series of V_{PM} pulses to the VOUT pin of the device, as shown in figure 5, increments the bit field of the selected parameter.

When addressing the bit field, the number of V_{PM} pulses is represented by a decimal number called a *code*. Addressing activates the corresponding fuse locations in the given bit field by incrementing the binary value of an internal DAC. The value of the bit field (and code) increments by one with the falling edge of each V_{PM} pulse, up to the maximum possible code (see the Programming Logic table). As the value of the bit field code increases, the value of the programmable parameter changes.

Measurements can be taken after each pulse to determine if the desired result for the programmable parameter has been reached. Cycling the supply voltage resets all the locations in the bit field that have unblown fuses to their initial states.

Fuse Blowing

After the required code is found for a given parameter, its value can be set permanently by blowing individual fuses in the appropriate register bit field. Blowing is accomplished by applying a V_{PH} pulse, called a *blow pulse*, of sufficient duration at the $V_{P(HIGH)}$ level to permanently set an addressed bit by blowing a fuse internal to the device. Due to power requirements, the fuse for each bit in the bit field must be blown individually. To accomplish this, the code representing the desired parameter value

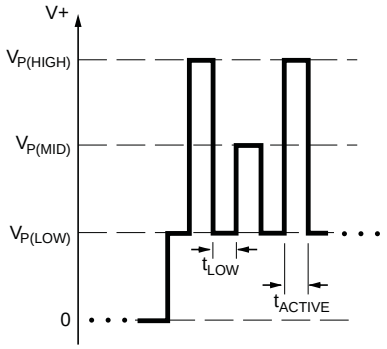


Figure 4. Parameter selection pulse train. This shows the sequence for selecting the register corresponding to key 1, indicated by a single V_{PM} pulse.

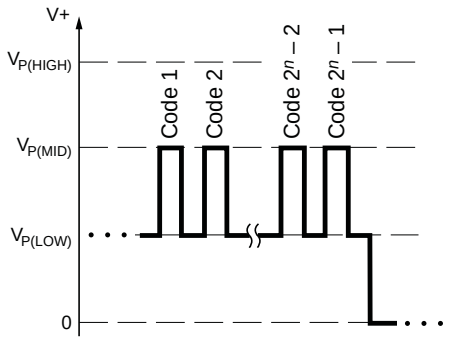


Figure 5. Bit field addressing pulse train. Addressing the bit field by incrementing the code causes the programmable parameter value to change. The number of bits available for a given programming code, *n*, varies among parameters; for example, the bit field for $V_{OUT(Q)}$ has 6 bits available, which allows 63 separate codes to be used.

must be translated to a binary number. For example, as shown in figure 6, decimal code 5 is equivalent to the binary number 101. Therefore bit 2 (code 4) must be addressed and blown, the device power supply cycled, and then bit 0 (code 1) addressed and blown. An appropriate sequence for blowing code 5 is shown in figure 7. The order of blowing bits, however, is not important. Blowing bit 0 first, and then bit 2 is acceptable.

Note: After blowing, the programming is not reversible, even after cycling the supply power. Although a register bit field fuse cannot be reset after it is blown, additional bits within the same register can be blown at any time until the device is locked. For example, if bit 1 (binary 10) has been blown, it is still possible to blow bit 0. The end result would be binary 11 (decimal code 3).

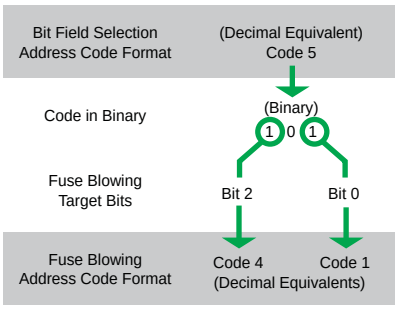


Figure 6. Example of code 5 broken into its binary components, which are code 4 and code 1.

Locking the Device

After the desired code for each parameter is programmed, the device can be locked to prevent further programming of any parameters.

Additional Guidelines

The additional guidelines in this section should be followed to ensure the proper behavior of these devices:

- A 0.1 µF blowing capacitor, C_{BLOW}, must be mounted between the VOUT pin and the GND pin during programming, to ensure enough current is available to blow fuses.
- The C_{BLOW} blowing capacitor must be replaced in the final application with a suitable C_L. (The maximum load capacitance is 10 nF for proper operation.)
- The power supply used for programming must be capable of delivering at least 26 V and 300 mA.
- Be careful to observe the t_{LOW} delay time before powering down the device after blowing each bit.
- The following programming order is recommended:
  1. Sens
  2. $V_{OUT(Q)}$
  3. LOCK (only after all other parameters have been programmed and validated, because this prevents any further programming of the device)

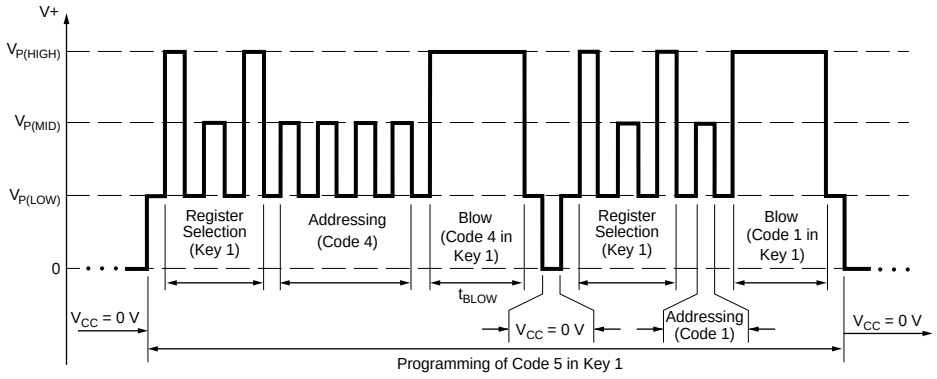


Figure 7. Example of programming pulses applied to the VOUT pin that result in permanent parameter settings. In this example, the register corresponding to key 1 is selected and code 5 is addressed and blown.

Programming Modes

Try Mode

Try mode allows a single programmable parameter to be tested without permanently setting its value. Multiple parameters cannot be tested simultaneously in this mode. After powering the VCC supply, select the desired parameter register and address its bit field. When addressing the bit field, each V_{PM} pulse increments the value of the parameter register, up to the maximum possible code (see Programming Logic table). The addressed parameter value remains stored in the device even after the programming drive voltage is removed from the VOUT pin, allowing the value to be measured. Note that for accurate time measurements, the blow capacitor, C_{BLOW}, should be removed during output voltage measurement.

It is not possible to decrement the value of the register without resetting the parameter bit field. To reset the bit field, and thus the value of the programmable parameter, cycle the supply (V_{CC}) voltage.

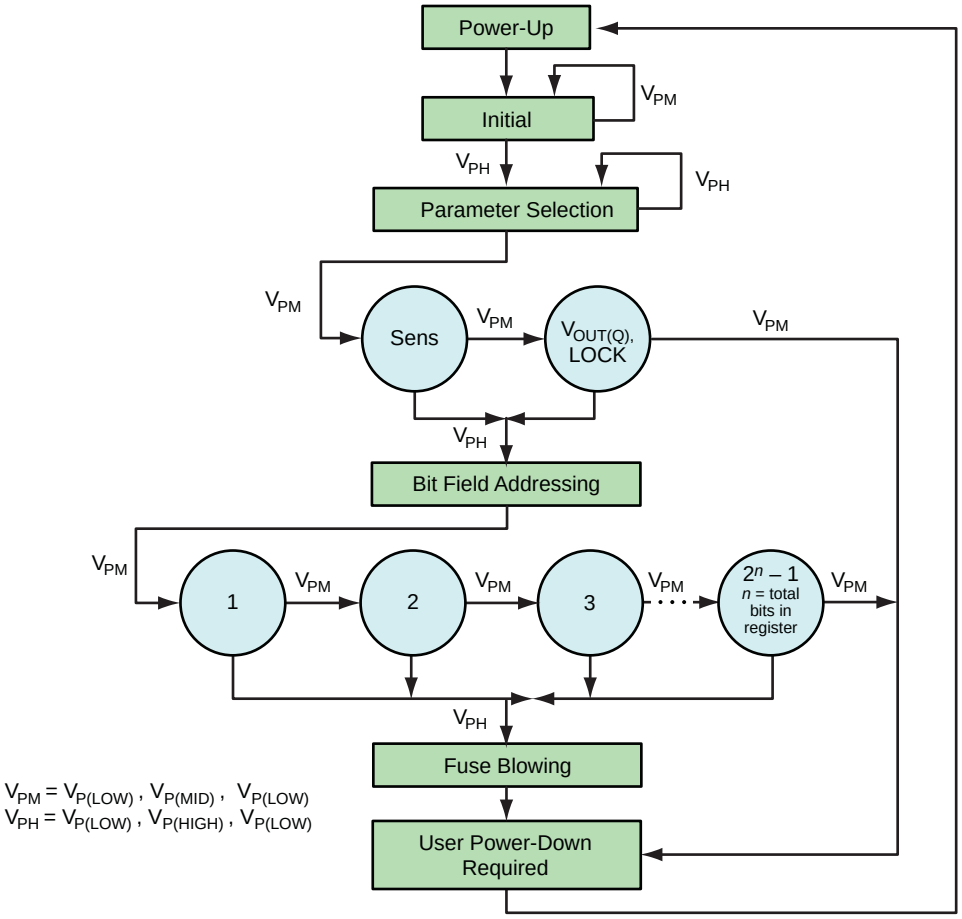
Blow Mode

After the required value of the programmable parameter is found using Try mode, its corresponding code should be blown to make its value permanent. To do this, select the required parameter register, and address and blow each required bit separately (as described in the Fuse Blowing section). The supply must be cycled between blowing each bit of a given code. After a bit is blown, cycling the supply will not reset its value.

Lock Mode

To lock the device, address the LOCK bit and apply a blow pulse with C_{BLOW} in place. After locking the device, no future programming of any parameter is possible.

Programming State Machine



Initial State After system power-up, the programming logic is reset to a known state. This is referred to as the Initial state. All the bit field locations that have intact fuses are set to logic 0. While in the Initial state, any V_{PM} pulses on the VOUT pin are ignored. To enter the Parameter Selection state, apply one V_{PH} pulse on the VOUT pin.

Parameter Selection State This state allows the selection of the parameter register containing the bit fields to be programmed. To select a parameter register, increment through the keys by applying V_{PM} pulses on the VOUT pin. Register keys select among the following programming parameters:

- 1 pulse - Sens
- 2 pulses - $V_{OUT(Q)}$ and LOCK

To enter the Bit Field Addressing state, apply one V_{PH} pulse on the VOUT pin.

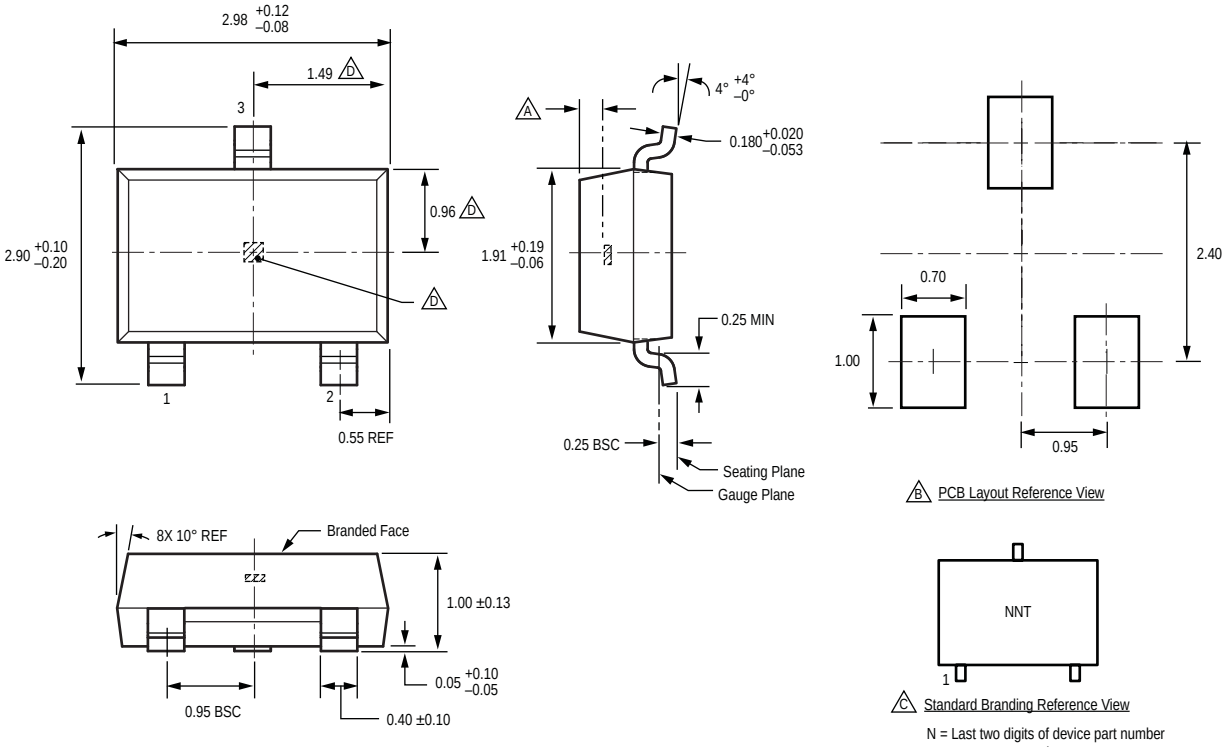
Bit Field Addressing State This state allows the selection of the individual bit fields to be programmed in the selected parameter register (see Programming Logic table). To leave this state, either cycle device power or blow the fuses for the selected code. Note that merely addressing the bit field does not permanently set the value of the selected programming parameter; fuses must be blown to do so.

Fuse Blowing State To blow an addressed bit field, apply a V_{PH} pulse on the VOUT pin. Power to the device should then be cycled before additional programming is attempted. Note: Each bit representing a decimal code must be blown individually (see the Fuse Blowing section).

Programming Logic Table

Programmable Parameter (Register Key)	Bit Field Address		Description
	Binary Format [MSB → LSB]	Decimal Equivalent Code	
Sens (1)	000000	0	Initial value ($Sens_{init}$)
	111111	63	Maximum value of sensitivity (Sens) in range
$V_{OUT(Q)}$, LOCK (2)	000000	0	Initial value ($V_{OUT(Q)init}$)
	011111	31	Maximum value of quiescent voltage output ($V_{OUT(Q)}$) in range; B = 0 G
	100000	32	LOCK bit, enables permanent locking of all programming bit fields in the device

Package LH, 3 Pin; (SOT-23W)



For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Active Area Depth, 0.28 mm REF

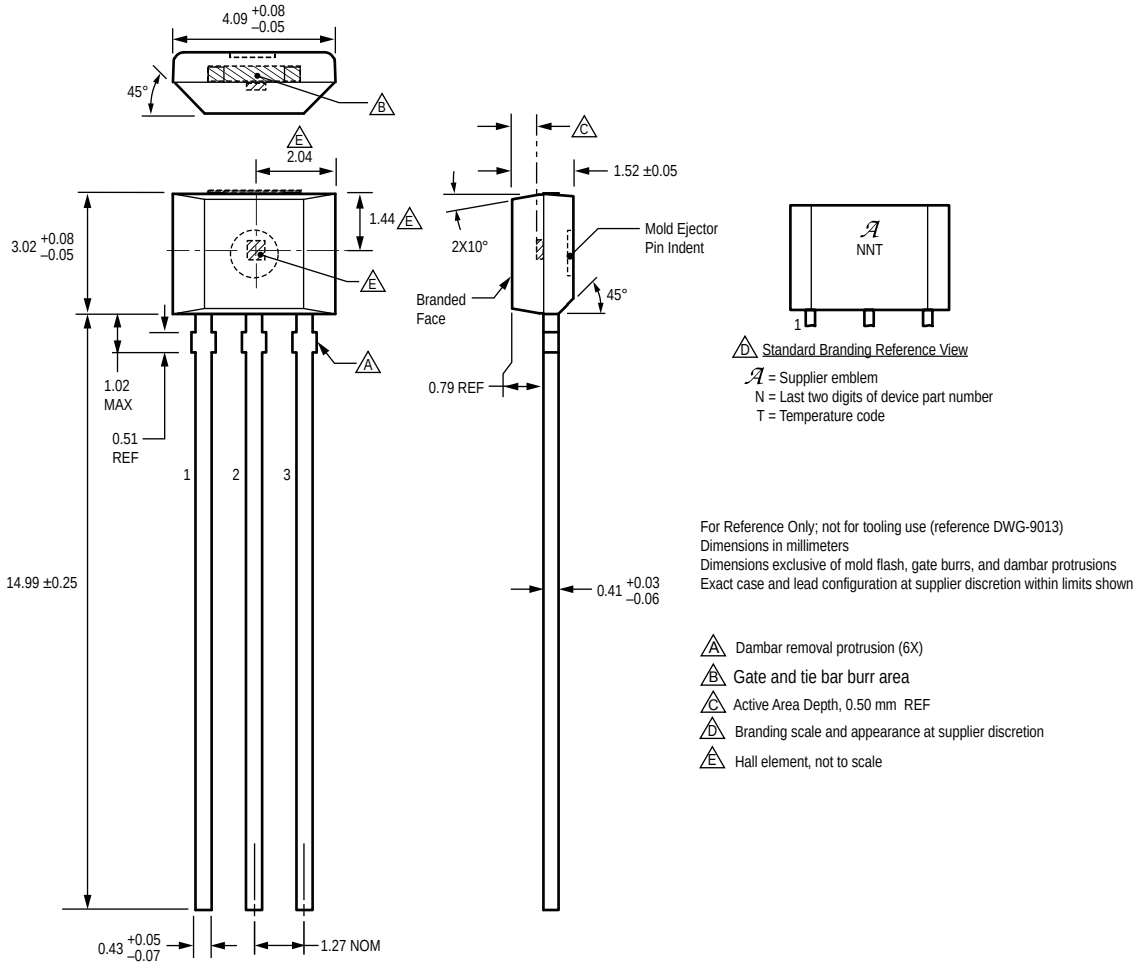
B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

N = Last two digits of device part number
T = Temperature code

Package UA, 3-Pin SIP



Please note that there are changes to the existing UA package drawing pending. Please contact the Allegro Marketing department for additional information.

For the latest version of this document, visit our website:
www.allegromicro.com