

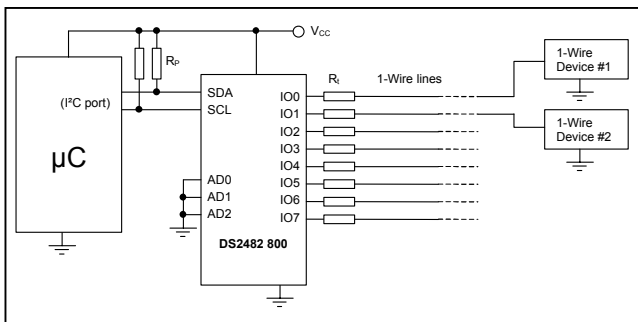
### GENERAL DESCRIPTION

The DS2482-800 is an I<sup>2</sup>C™ to 1-Wire® bridge device that interfaces directly to standard (100kHz max) or fast (400kHz max) I<sup>2</sup>C masters to perform bi-directional protocol conversion between the I<sup>2</sup>C master and any downstream 1-Wire slave devices. Relative to any attached 1-Wire slave device, the DS2482-800 is a 1-Wire master. Internal factory-trimmed timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and Overdrive 1-Wire communication speeds. To optimize 1-Wire waveform generation, the DS2482-800 performs slew-rate control on rising and falling 1-Wire edges and has a programmable feature to mask the fast presence pulse edge that some 1-Wire slave devices can generate. Programmable strong pullup features support 1-Wire power delivery to 1-Wire devices such as EEPROMs and sensors. The DS2482-800 combines these features with eight independent 1-Wire I/O channels. The I<sup>2</sup>C slave address assignment is controlled by three binary address inputs, resolving potential conflicts with other I<sup>2</sup>C slave devices in the system.

### APPLICATIONS

- Wireless Base Stations
- Central Office Switches
- PBXs
- Rack-Based Servers
- Medical Clinical Diagnostic Equipment

### TYPICAL OPERATING CIRCUIT



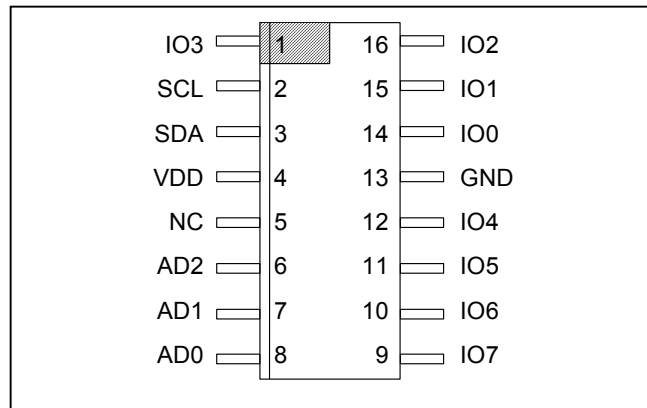
### FEATURES

- I<sup>2</sup>C Host Interface, Supports 100kHz and 400kHz I<sup>2</sup>C Communication Speeds
- 1-Wire Master I/O with Selectable Active or Passive 1-Wire Pullup
- Provides Reset/Presence, 8-Bit, Single-Bit, and Three-Bit 1-Wire I/O Sequences
- Eight Channels of Independently Operated 1-Wire I/O
- Standard and Overdrive 1-Wire Communication Speeds
- Slew Controlled 1-Wire Edges
- Selectable 1-Wire Slave Presence Pulse Falling Edge Masking to Control Fast Edges on the 1-Wire Line
- Supports Low-Impedance 1-Wire Strong Pullup for EEPROMs, Temp Sensors, or Other 1-Wire Slaves That Have Momentary High Current Modes
- Three Address Inputs for I<sup>2</sup>C Address Assignment
- Wide Operating Range: 2.9V to 5.5V, -40°C to +85°C
- 16-Pin SO Package (150 mil)

### ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2482S-800	-40 to +85°C	16 SO (150 mil)
DS2482S-800/T&R	-40 to +85°C	16 SO (150 mil)

### PIN CONFIGURATION



I<sup>2</sup>C is a trademark of Philips Corp. Purchase of I<sup>2</sup>C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.  
1-Wire is a registered trademark of Dallas Semiconductor.

**Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: [www.maxim-ic.com/errata](http://www.maxim-ic.com/errata).

**ABSOLUTE MAXIMUM RATINGS**

Voltage Range on Any Pin Relative to Ground  
 Maximum Current Into Any Pin  
 Operating Temperature Range  
 Junction Temperature  
 Storage Temperature Range  
 Soldering Temperature

-0.5V, +6V  
 $\pm 20\text{mA}$   
 $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$   
 $+150^{\circ}\text{C}$   
 $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 See IPC/JEDEC J-STD-020A

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.*

**ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 2.9\text{V}$  to  $5.5\text{V}$ ,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC}$	3.3V	2.9	3.3	3.7	V
		5V	4.5	5.0	5.5	
Operating Current	$I_{CC}$	(Note 1)			0.75	mA
1-Wire Input High	$V_{IH1}$	3.3V (Notes 2, 3)	1.9			V
		5V (Notes 2, 3)	3.4			
1-Wire Input Low	$V_{IL1}$	3.3V (Notes 2, 3)			0.75	V
		5V (Notes 2, 3)			1.0	
1-Wire Weak Pullup Resistor	$R_{WPU}$	(Note 4)	800		1675	$\Omega$
1-Wire Output Low	$V_{OL1}$	At 4mA load			0.4	V
Active Pullup On Time	$t_{APUOT}$	Standard (Notes 4, 5)	2.3	2.5	2.7	$\mu\text{s}$
		Overdrive (Notes 4, 5)	0.4	0.5	0.6	
Strong Pullup Voltage Drop	$\Delta V_{STRPU}$	$V_{CC} \geq 3.2\text{V}$ , 1.5mA load			0.3	V
		$V_{CC} \geq 5.2\text{V}$ , 3mA load			0.5	
3.3V Pulldown Slew Rate (Note 6)	$PD_{SRC}$	Standard (3.3V $\pm 5\%$ )	1		4.2	V/ $\mu\text{s}$
		Overdrive (3.3V $\pm 5\%$ )	5		22.1	
5V Pulldown Slew Rate (Note 6)	$PD_{SRC}$	Standard (5.0V $\pm 5\%$ )	2		6.5	V/ $\mu\text{s}$
		Overdrive (5.0V $\pm 5\%$ )	10		40	
3.3V Pullup Slew Rate (Note 6)	$PU_{SRC}$	Standard (3.3V $\pm 5\%$ )	0.8		4	V/ $\mu\text{s}$
		Overdrive (3.3V $\pm 5\%$ )	1.3		6	
5V Pullup Slew Rate (Note 6)	$PU_{SRC}$	Standard (5.0V $\pm 5\%$ )	2.7		20	V/ $\mu\text{s}$
		Overdrive (5.0V $\pm 5\%$ )	3.4		31	
Power-On Reset Trip Point	$V_{POR}$				2.2	V
<b>1-Wire TIMING (Note 16) See Figures 3, 5, 6, and 7</b>						
Write 1/Read Low Time	$t_{W1L}$	Standard	7.6	8	8.4	$\mu\text{s}$
		Overdrive	0.9	1	1.1	
Read Sample Time	$t_{MSR}$	Standard	13.3	14	15	$\mu\text{s}$
		Overdrive	1.4	1.5	1.8	
1-Wire Time Slot	$t_{slot}$	Standard	65.8	69.3	72.8	$\mu\text{s}$
		Overdrive	9.9	10.5	11.0	
Fall Time High-to-Low at Standard Speed (Note 6)	$t_{F1}$	3.3V to 0V (Note 5)	0.6		2.6	$\mu\text{s}$
		5.5V to 0V (Note 5)	0.7		2.2	
3.3V to 0V (Note 5)		0.1		0.5		
5.5V to 0V (Note 5)		0.1		0.4		
Fall Time High-to-Low at Overdrive Speed (Note 6)						

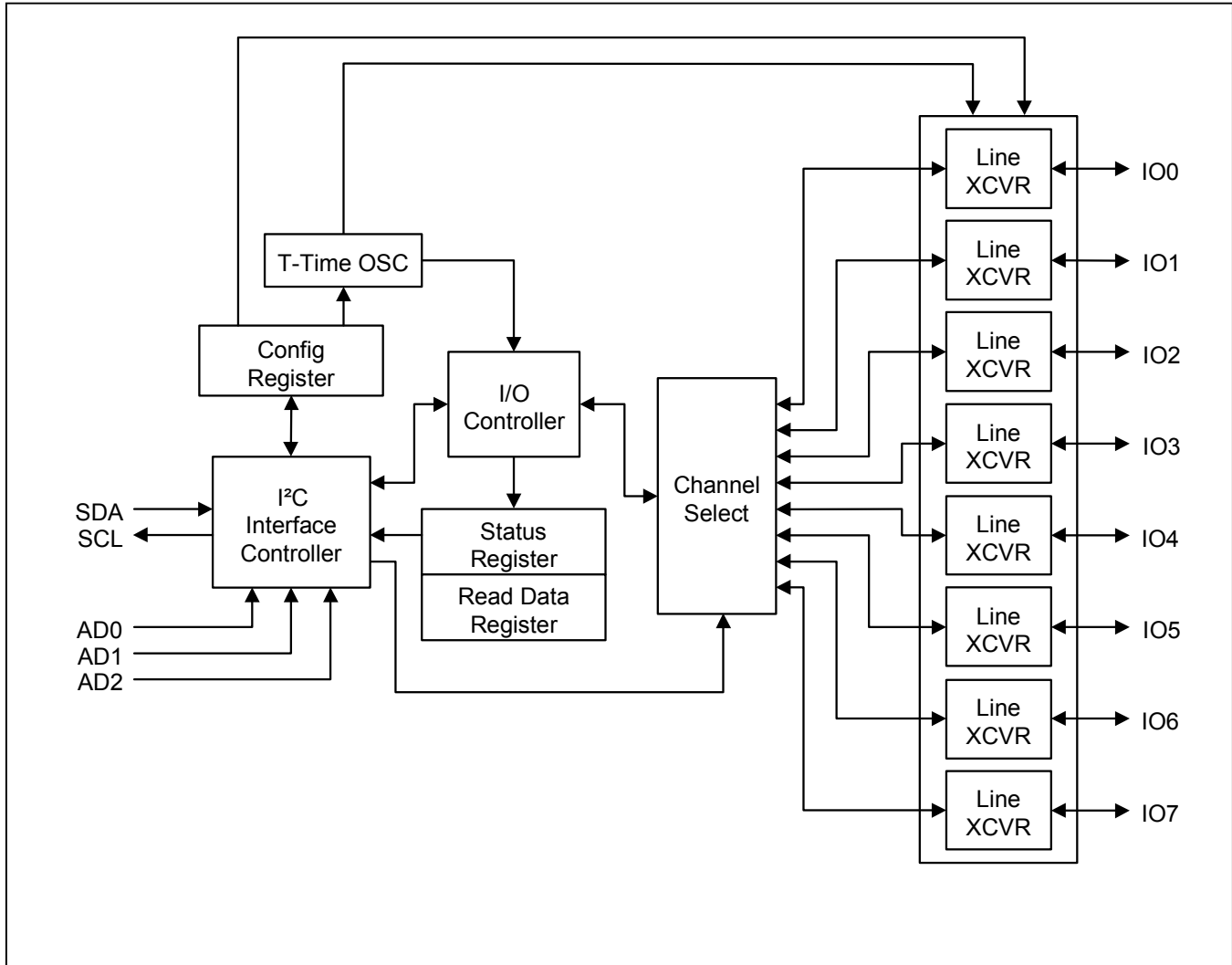
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	$t_{WOL}$	Standard	60	64	68	$\mu\text{s}$
		Overdrive	7.1	7.5	7.9	
Write 0 Recovery Time	$t_{RECO}$	Standard	5.0	5.3	5.6	$\mu\text{s}$
		Overdrive	2.8	3.0	3.2	
Reset Low Time	$t_{RSTL}$	Standard	570	600	630	$\mu\text{s}$
		Overdrive	68.4	72	75.6	
Presence-Detect Sample Time	$t_{MSP}$	Standard	66.5	70	73.5	$\mu\text{s}$
		Overdrive	7.1	7.5	7.9	
Sampling for Short and Interrupt	$t_{SI}$	Standard	7.6	8	8.4	$\mu\text{s}$
		Overdrive	0.7	0.75	0.8	
Reset High Time	$t_{RSTH}$	Standard	554.8	584	613.2	$\mu\text{s}$
		Overdrive	70.3	74	77.7	
Presence Pulse Mask Start	$t_{ppm1}$	(Note 7)	9.5	10	10.5	$\mu\text{s}$
Presence Pulse Mask Stop	$t_{ppm2}$	(Note 7)	57	60	63	$\mu\text{s}$
<b>I<sup>2</sup>C-Pins (Note 8) See Figure 10</b>						
LOW Level Input Voltage	$V_{IL}$	$V_{CC} = 2.9\text{V to }3.7\text{V}$	-0.5		$0.25 \times V_{CC}$	V
		$V_{CC} = 4.5\text{V to }5.5\text{V}$			$0.22 \times V_{CC}$	
HIGH Level Input Voltage	$V_{IH}$		$0.7 \times V_{CC}$		$V_{CC} + 0.5\text{V}$	V
Hysteresis of Schmitt Trigger Inputs	$V_{hys}$		$0.05 \times V_{CC}$			V
LOW Level Output Voltage at 3mA Sink Current	$V_{OL}$				0.4	V
Output Fall Time from $V_{Ihmin}$ to $V_{ILmax}$ with a Bus Capacitance from 10pF to 400pF	$t_{of}$		60		250	ns
Pulse Width of Spikes that are Suppressed by the Input Filter	$t_{SP}$	SDA and SCL pins only			50	ns
Input Current Each I/O Pin with an Input Voltage Between $0.1V_{CCmax}$ and $0.9V_{CCmax}$	$I_i$	(Notes 9, 10)	-10		10	$\mu\text{A}$
Input Capacitance	$C_i$	(Note 9)			10	pF
SCL Clock Frequency	$f_{SCL}$		0		400	kHz
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated.	$t_{HD:STA}$		0.6			$\mu\text{s}$
LOW Period of the SCL Clock	$t_{LOW}$		1.3			$\mu\text{s}$
HIGH Period of the SCL Clock	$t_{HIGH}$		0.6			$\mu\text{s}$
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			$\mu\text{s}$
Data Hold Time	$t_{HD:DAT}$	(Notes 11, 12)			0.9	$\mu\text{s}$
Data Setup Time	$t_{SU:DAT}$	(Note 13)	250			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			$\mu\text{s}$
Bus Free Time Between a STOP and START Condition	$t_{BUF}$		1.3			$\mu\text{s}$
Capacitive Load for Each Bus Line	$C_b$	(Note 14)			400	pF
Oscillator Warm-Up Time	$t_{OSCWUP}$	(Note 15)			100	$\mu\text{s}$

- Note 1:** Operating current with 1-Wire write byte sequence followed by continuous Read of Status Register at 400KHz in Overdrive.
- Note 2:** With standard speed the total capacitive load of the 1-Wire bus should not exceed 1nF, otherwise the passive pullup on threshold  $V_{IL1}$  may not be reached in the available time. With Overdrive speed the capacitive load on the 1-Wire bus must not exceed 300pF.
- Note 3:** Active pullup guaranteed to turn on between  $V_{IL1MAX}$  and  $V_{IH1MIN}$ .
- Note 4:** Active or resistive pullup choice is configurable.
- Note 5:** Fall time high to low ( $t_{F1}$ ) is derived from  $PD_{SRC}$ , referenced from  $0.9 \times V_{CC}$  to  $0.1 \times V_{CC}$ .
- Note 6:** These values apply at full load, i. e., 1nF at standard speed and 0.3nF at Overdrive speed. For reduced load, the pulldown slew rate is slightly faster.
- Note 7:** Presence pulse masking only applies to standard speed.
- Note 8:** All I<sup>2</sup>C timing values are referred to  $V_{IHmin}$  and  $V_{ILmax}$  levels.
- Note 9:** Applies to SDA, SCL, and AD0, AD1, AD2.
- Note 10:** I/O pins of the DS2482 do not obstruct the SDA and SCL lines if  $V_{CC}$  is switched off.
- Note 11:** The DS2482 provides a hold time of at least 300ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- Note 12:** The maximum  $t_{HD-DAT}$  has only to be met if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.
- Note 13:** A Fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU-DAT} \geq 250ns$  must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_r \max + t_{SU-DAT} = 1000 + 250 = 1250ns$  (according to the standard-mode I<sup>2</sup>C-bus specification) before the SCL line is released.
- Note 14:**  $C_B$  = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times according to I<sup>2</sup>C-Bus Specification v2.1 are allowed.
- Note 15:** I<sup>2</sup>C communication should not take place for the max  $t_{OSCWUP}$  time following a power-on reset.
- Note 16:** Except for  $t_{F1}$ , all 1-Wire timing specifications and  $t_{APUOT}$  are derived from the same timing circuit. Therefore, if one of these parameters is found to be off the typical value, it is safe to assume that all of these parameters deviate from their typical value in the same direction and by the same degree.

## PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IO3	IO Driver for 1-Wire Line #3
2	SCL	I <sup>2</sup> C Serial Clock Input; must be tied to VCC through a pullup resistor.
3	SDA	I <sup>2</sup> C Serial Data Input/Output; must be tied to VCC through a pullup resistor.
4	VCC	Power Supply Input
5	NC	Not Connected
6	AD2	I <sup>2</sup> C Address Inputs; must be tied to VCC or GND. These inputs determine the I <sup>2</sup> C slave address of the device, see Figure 9.
7	AD1	
8	AD0	
9	IO7	IO Driver for 1-Wire Line #7
10	IO6	IO Driver for 1-Wire Line #6
11	IO5	IO Driver for 1-Wire Line #5
12	IO4	IO Driver for 1-Wire Line #4
13	GND	Ground Reference
14	IO0	IO Driver for 1-Wire Line #0
15	IO1	IO Driver for 1-Wire Line #1
16	IO2	IO Driver for 1-Wire Line #2

Figure 1. Block Diagram



## DETAILED DESCRIPTION

The DS2482-800 is a self-timed 8-channel 1-Wire master, which supports advanced 1-Wire waveform features including standard and Overdrive speeds, active pullup, strong pullup for power delivery, and presence pulse masking. Once supplied with command and data, the I/O controller of the DS2482 performs time-critical 1-Wire communication functions such as reset/presence detect cycle, read-byte, write-byte, single-bit R/W and triplet for ROM Search, without requiring interaction with the host processor. The host obtains feedback (completion of a 1-Wire function, presence pulse, 1-Wire short, search direction taken) through the Status Register and data through the Read Data register. The DS2482 communicates with a host processor through its I²C bus interface in standard-mode or in fast-mode. The logic state of three address pins (2 address pins with the 1-channel version) determines the I²C slave address of the DS2482, allowing up to 8 devices operating on the same bus segment without requiring a hub.

## DEVICE REGISTERS

The DS2482 has four registers that the I²C host can read: Channel Selection, Configuration, Status, and Read Data. These registers are addressed by a read pointer. The position of the read pointer, i.e., the register that the host will read in a subsequent read access, is defined by the instruction that the host has DS2482 executed last. The host has read and write access to the Channel Selection and Configuration Registers to select one of several 1-Wire channels and to enable certain 1-Wire features.

## Channel Selection Register

The content of the Channel Selection Register specifies which of the channels is selected and will be the target of subsequent 1-Wire communication commands. The DS2482-800 supports eight 1-Wire communication channels IO0 to IO7. Only one of these channels can be active/selected at any time. Once selected, a 1-Wire channel remains selected until a different channel is selected through the **Channel Select command** or by initiating a device reset. After a device reset (power-up cycle or initiated by the Device Reset command) the IO0 channel is selected.

## Configuration Register

The DS2482 supports allows four 1-Wire features that are enabled or selected through the Configuration Register. These features are:

- Active Pullup (APU)
- Presence Pulse Masking (PPM)
- Strong Pullup (SPU)
- 1-Wire Speed (1WS)

These features can be selected in any combination. They apply equally to all 1-Wire channels. While APU, PPM and 1WS maintain their state, SPU returns to its inactive state as soon as the strong pullup has ended.

## Configuration Register Bit Assignment

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{1WS}$	$\overline{SPU}$	$\overline{PPM}$	$\overline{APU}$	1WS	SPU	PPM	APU

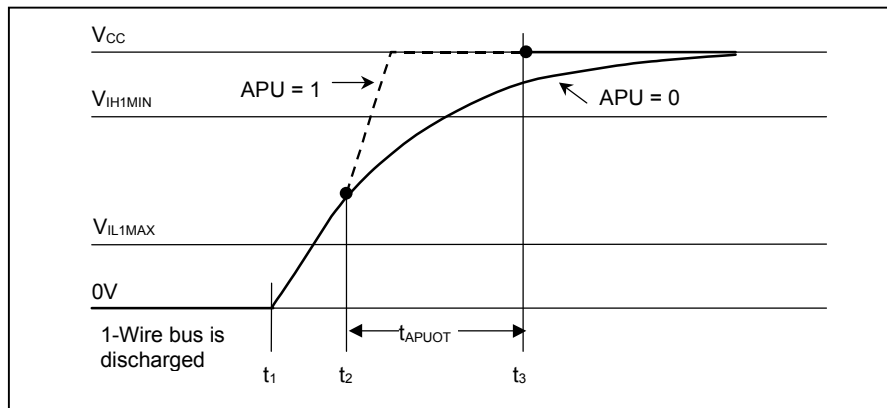
After a device reset (power-up cycle or initiated by the Device Reset command) the Configuration Register reads 00h. When writing to the Configuration Register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.

## Active Pullup (APU)

The APU bit controls whether an active pullup (controlled slew-rate transistor) or a passive pullup ( $R_{WPU}$  resistor) will be used to drive a 1-Wire line from low to high. When APU = 0, active pullup is disabled (resistor mode). Active Pullup should be selected if the 1-Wire line has a substantial length (30 meters or more) or if there is a large number (~20 or more) of devices connected to a 1-Wire line. **The active pullup does not apply to the rising edge of a presence pulse or a recovery after a short on the 1-Wire line.**

The circuit that controls rising edges (Figure 2) operates as follows: At  $t_1$  the pulldown (from DS2482 or 1-Wire slave) ends. From this point on the 1-Wire bus is pulled high through  $R_{WPU}$  internal to the DS2482.  $V_{CC}$  and the capacitive load of the 1-Wire line determine the slope. In case that active pullup is disabled (APU = 0), the resistive pullup continues, as represented by the solid line. With active pullup enabled (APU = 1), when at  $t_2$  the voltage has reached a level between  $V_{IL1max}$  and  $V_{IH1min}$ , the DS2482 actively pulls the 1-Wire line high applying a controlled slew rate, as represented by the dashed line. The active pullup continues until  $t_{APUOT}$  is expired at  $t_3$ . From that time on the resistive pullup will continue.

**Figure 2. Rising Edge Pullup**

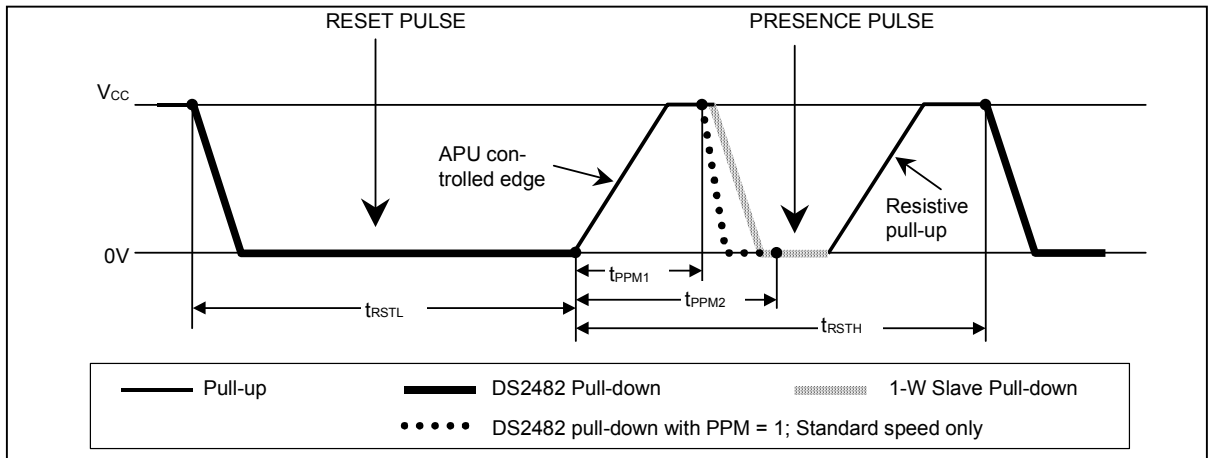


### Presence Pulse Masking (PPM)

The PPM bit controls whether the DS2482 will mask the leading edge (falling) of presence pulses. When PPM = 0, masking is disabled. Presence pulse masking applies only to standard 1-Wire speed (1WS = 0); this bit has no function if 1WS = 1 (Overdrive speed). Presence pulse masking can improve the performance of large 1-Wire networks since it prevents the fast falling edge of a presence pulse generated by a 1-Wire slave device from propagating through the network and getting reflected. Reflections can cause glitches in the network that in turn may cause slave devices to lose synchronization with the 1-Wire master.

Figure 3 shows the timing references for the PPM. If enabled (PPM = 1), the DS2482 begins pulling the 1-Wire line low at  $t_{PPM1}$  after the reset low time  $t_{RSTL}$  is expired. The pulldown ends at  $t_{PPM2}$ , at which a 1-Wire slave, if present, will be pulling the 1-Wire line low. The falling edge of the presence pulse mask is slew rate controlled.

**Figure 3. Presence Pulse Masking**

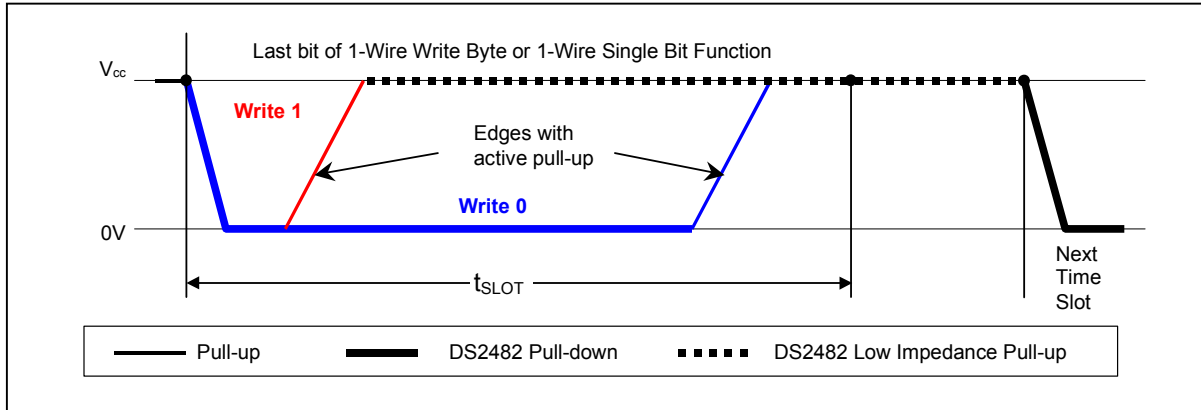


### Strong Pullup (SPU)

The SPU bit controls whether the DS2482 applies a low-impedance pullup to  $V_{CC}$  on the 1-Wire line after the last bit of either a **1-Wire Write Byte** command or after a **1-Wire Single Bit** command has completed. The strong pullup feature is commonly used with 1-Wire EEPROM devices when copying scratchpad data to the main memory or when performing a SHA-1 computation, and with parasitically powered temperature sensors or A-to-D converters. The respective device data sheets specify the location in the communications protocol after which the strong pullup should be applied. The SPU bit in the configuration register of the DS2482 must be set immediately prior to issuing the command that puts the 1-Wire device into the state where it needs the extra power.

If SPU is 1, the DS2482 applies **active pullup** to the rising edge of the time slot in which the strong pullup starts, regardless of the APU bit setting. However, in contrast to setting APU = 1 for active pullup, the low-impedance pullup will not end after  $t_{APUOT}$  is expired. Instead, as shown in Figure 4, the low-impedance pullup remains active until: a) the next 1-Wire communication command (the typical case), b) by writing to the Configuration Register with the SPU bit being 0 (alternative), or c) by issuing the Device Reset command. Additionally, when the pullup ends, the SPU bit is automatically reset to 0. Using the strong pullup does not change the state of the APU bit in the Configuration Register.

Figure 4. Low-Impedance Pullup Timing



### 1-Wire Speed (1WS)

The 1WS bit determines the timing of any 1-Wire communication generated by the DS2482. All 1-Wire slave devices support standard speed (1WS = 0), where the transfer of a single bit ( $t_{\text{SLOT}}$  in Figure 4) is completed within 65 $\mu\text{s}$ . Many 1-Wire device can also communicate at a higher data rate, called Overdrive speed. To change from standard to Overdrive speed, a 1-Wire device needs to receive an Overdrive Skip ROM or Overdrive Match ROM command, as explained in the device data sheets. The change in speed occurs immediately after the 1-Wire device has received the speed-changing command code. The DS2482 must take part in this speed change to stay synchronized. This is accomplished by writing to the Configuration Register with the 1WS bit being 1 **immediately after** the 1-Wire Byte command that changes the speed of a 1-Wire device. Writing to the Configuration Register with the 1WS bit being 0 followed by a 1-Wire Reset command changes the DS2482 and any 1-Wire devices on the active 1-Wire line back to standard speed.

### Status Register

The read-only Status Register is the general means for the DS2482 to report bit-type data from the 1-Wire side, 1-Wire busy status and its own reset status to the host processor. All 1-Wire communication commands and the Device Reset command position the read pointer at the Status Register for the host processor to read with minimal protocol overhead. Status information is updated during the execution of certain commands only. Details are given in the description of the various status bits below.

### Status Register Bit Assignment

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DIR	TSB	SBR	RST	LL	SD	PPD	1WB

### 1-Wire Busy (1WB)

The 1WB bit reports to the host processor whether the 1-Wire line is busy. During 1-Wire communication 1WB is 1; once the command is completed, 1WB returns to its default 0. Details on when 1WB changes state and for how long it remains at 1 are found in the *Function Commands* section.

### Presence Pulse Detect (PPD)

The PPD bit is updated with every 1-Wire Reset command. If the DS2482 detects a presence pulse from a 1-Wire device at  $t_{\text{MSP}}$  during the Presence Detect cycle, the PPD bit will be set to 1. This bit will return to its default 0 if there is no presence pulse or if the 1-Wire line is shorted during a subsequent 1-Wire Reset command.

### Short Detected (SD)

The SD bit is updated with every 1-Wire Reset command. If the DS2482 detects a logic 0 on the 1-Wire line at  $t_{\text{SI}}$  during the Presence Detect cycle, the SD bit will be set to 1. This bit will return to its default 0 with a subsequent 1-Wire Reset command provided that the short has been removed. If SD is 1, PPD will be 0. The DS2482 cannot distinguish between a short and a DS1994 or DS2404 signaling a 1-Wire interrupt. For this reason, if a DS2404/DS1994 is used in the application, the interrupt function must be disabled. The interrupt signaling is explained in the respective device data sheets.



**Logic Level (LL)**

The LL bit reports the logic state of the active 1-Wire line without initiating any 1-Wire communication. The 1-Wire line is sampled for this purpose every time the Status Register is read. The sampling and updating of the LL bit takes place when the host processor has addressed the DS2482 in read mode (during the acknowledge cycle), provided that the Read Pointer is positioned at the Status Register.

**Device Reset (RST)**

If the RST bit is 1, the DS2482 has performed an internal reset cycle, either caused by a power-on reset or from executing the Device Reset command. The RST bit is cleared automatically when the DS2482 executes a Write Configuration command to restore the selection of the desired 1-Wire features.

**Single Bit Result (SBR)**

The SBR bit reports the logic state of the active 1-Wire line sampled at  $t_{MSR}$  of a 1-Wire Single Bit command or the first bit of a 1-Wire Triplet command. The power-on default of SBR is 0. If the 1-Wire Single Bit command sends a 0-bit, SBR should be 0. With a 1-Wire Triplet command, SBR could be 0 as well as 1, depending on the response of the 1-Wire devices connected. The same result applies to a 1-Wire Single Bit command that sends a 1-bit.

**Triplet Second Bit (TSB)**

The TSB bit reports the logic state of the active 1-Wire line sampled at  $t_{MSR}$  of the second bit of a 1-Wire Triplet command. The power-on default of TSB is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands.

**Branch Direction Taken (DIR)**

Whenever a 1-Write Triplet command is executed, this bit reports to the host processor the search direction that was chosen by the 3rd bit of the triplet. The power-on default of DIR is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands. For additional information see the description of the 1-Wire Triplet command and the Dallas Application Note 187, "1-Wire Search Algorithm".

**FUNCTION COMMANDS**

The DS2482 understands 9 function commands, which fall into four categories: device control, I<sup>2</sup>C communication, 1-Wire setup and 1-Wire communication. The feedback path to the host is controlled by a read pointer, which is set automatically by each function command for the host to efficiently access relevant information. The host processor sends these commands and applicable parameters as strings of one or two bytes using the I<sup>2</sup>C interface. The I<sup>2</sup>C protocol requires that each byte be acknowledged by the receiving party to confirm acceptance or not be acknowledged to indicate an error condition (invalid code or parameter) or to end the communication. Details of the I<sup>2</sup>C protocol including acknowledge are found in the I<sup>2</sup>C interface description of this document.

**Device Reset**

<b>Command Code</b>	F0h
<b>Command Parameter</b>	None
<b>Description</b>	Performs a global reset of device state machine logic, which in turn selects IO0 as the active 1-Wire channel. Terminates any ongoing 1-Wire communication.
<b>Typical Use</b>	Device initialization after power-up; re-initialization (reset) as desired.
<b>Restriction</b>	None (can be executed at any time)
<b>Error Response</b>	None
<b>Command Duration</b>	Maximum 525ns, counted from falling SCL edge of the command code acknowledge bit.
<b>1-Wire Activity</b>	Ends maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
<b>Read Pointer Position</b>	Status Register (for busy polling)
<b>Status Bits Affected</b>	RST set to 1, 1WB, PPD, SD, SBR, TSB, DIR set to 0
<b>Configuration Bits Affected</b>	1WS, APU, PPM, SPU set to 0

## Set Read Pointer

<b>Command Code</b>	E1h
<b>Command Parameter</b>	Pointer Code
<b>Description</b>	Sets the read pointer to the specified register. Overwrites the read pointer position of any 1-Wire communication command in progress.
<b>Typical Use</b>	To prepare reading the result from a 1-Wire Byte command; random read access of registers.
<b>Restriction</b>	None (can be executed at any time)
<b>Error Response</b>	If the pointer code is not valid, the pointer code will not be acknowledged and the command will be ignored.
<b>Command Duration</b>	None; the read pointer is updated on the rising SCL edge of the pointer code acknowledge bit.
<b>1-Wire Activity</b>	Not Affected
<b>Read Pointer Position</b>	As Specified by the Pointer Code
<b>Status Bits Affected</b>	None
<b>Configuration Bits Affected</b>	None

## Valid Pointer Codes

Register Selection	Code
Status Register	F0h
Read Data Register	E1h
Channel Selection Register	D2h
Configuration Register	C3h

## Write Configuration

<b>Command Code</b>	D2h
<b>Command Parameter</b>	Configuration Byte
<b>Description</b>	Writes a new configuration byte. The new settings take effect immediately. <b>NOTE:</b> When writing to the Configuration Register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.
<b>Typical Use</b>	Defining the features for subsequent 1-Wire communication.
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code and parameter will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored.
<b>Command Duration</b>	None; the configuration register is updated on the rising SCL edge of the configuration byte acknowledge bit.
<b>1-Wire Activity</b>	None
<b>Read Pointer Position</b>	Configuration Register (to verify write)
<b>Status Bits Affected</b>	RST set to 0
<b>Configuration Bits Affected</b>	1WS, SPU, PPM, APU updated

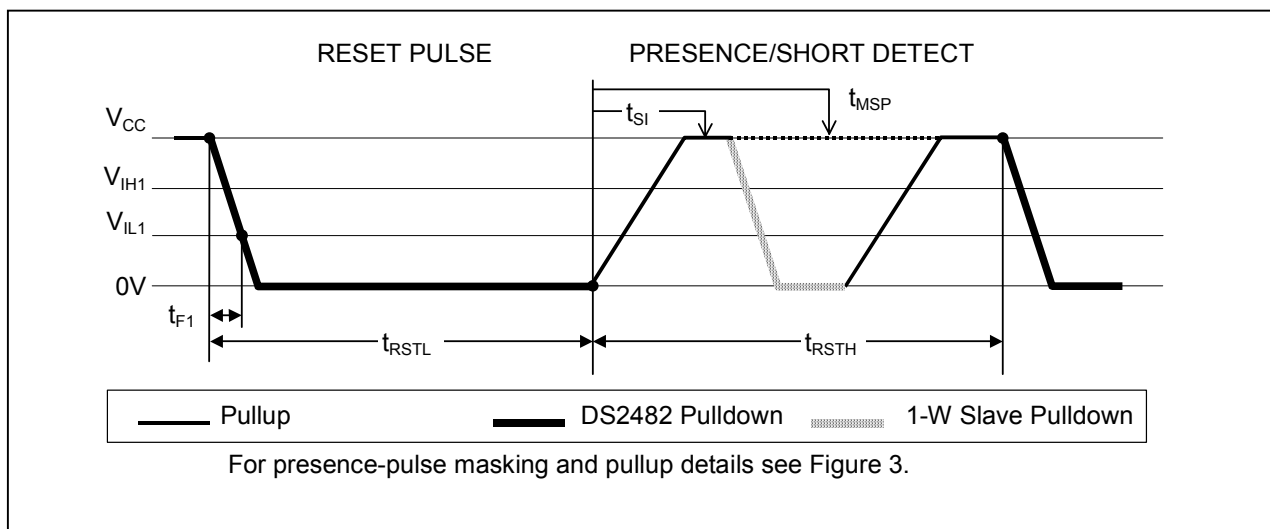
## Channel Select

<b>Command Code</b>	C3h
<b>Command Parameter</b>	Selection Code
<b>Description</b>	Sets the 1-Wire IO channel for subsequent 1-Wire communication commands. <b>NOTE:</b> The selection code read back is different from the code written. See the table below for the respective values.
<b>Typical Use</b>	Selecting a 1-Wire IO channel other than IO0; randomly selecting one of the available 1-Wire IO channels.
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code and parameter will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored. If the selection code is not valid, the selection code will not be acknowledged and the command will be ignored.
<b>Command Duration</b>	None; the channel selection register is updated on the rising SCL edge of the selection code acknowledge bit.
<b>1-Wire Activity</b>	None
<b>Read Pointer Position</b>	Channel Selection Register (to verify write)
<b>Status Bits Affected</b>	None
<b>Configuration Bits Affected</b>	None

### Valid Channel Selection Codes

Channel Selection	Code (to be written)	Code (read back)
Channel IO0 (default)	F0h	B8h
Channel IO1	E1h	B1h
Channel IO2	D2h	AAh
Channel IO3	C3h	A3h
Channel IO4	B4h	9Ch
Channel IO5	A5h	95h
Channel IO6	96h	8Eh
Channel IO7	87h	87h

**Figure 5. 1-Wire Reset/Presence Detect Cycle**



## 1-Wire Reset

<b>Command Code</b>	B4h
<b>Command Parameter</b>	None
<b>Description</b>	Generates a 1-Wire Reset/Presence Detect cycle (Figure 5) at the selected IO channel. The state of the 1-Wire line is sampled at $t_{SI}$ and $t_{MSP}$ and the result is reported to the host processor through the status register, bits PPD and SD.
<b>Typical Use</b>	To initiate or end any 1-Wire communication sequence.
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored.
<b>Command Duration</b>	$t_{RSTL} + t_{RSTH} +$ maximum 262.5ns, counted from the falling SCL edge of the command code acknowledge bit.
<b>1-Wire Activity</b>	Begins maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
<b>Read Pointer Position</b>	Status Register (for busy polling)
<b>Status Bits Affected</b>	1WB (set to 1 for $t_{RSTL} + t_{RSTH}$ ), PPD is updated at $t_{RSTL} + t_{MSP}$ , SD is updated at $t_{RSTL} + t_{SI}$
<b>Configuration Bits Affected</b>	1WS, PPM, APU apply

## 1-Wire Single Bit

<b>Command Code</b>	87h
<b>Command Parameter</b>	Bit Byte
<b>Description</b>	Generates a single 1-Wire time slot with a bit value 'V' as specified by the bit byte at the selected 1-Wire IO channel. A 'V' value of 0b will generate a write-zero time slot (Figure 6), a value of 1b will generate a write one slot, which also functions as a read data time slot (Figure 7). In either case the logic level at the 1-Wire line is tested at $t_{MSR}$ and SBR is updated.
<b>Typical Use</b>	To perform single bit writes or reads on a 1-Wire IO channel when single bit communication is necessary (the exception).
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code and bit byte will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored.
<b>Command Duration</b>	$t_{SLOT} +$ maximum 262.5ns, counted from the falling SCL edge of the first bit (MS bit) of the bit byte.
<b>1-Wire Activity</b>	Begins maximum 262.5ns after the falling SCL edge of the MS bit of the bit byte.
<b>Read Pointer Position</b>	Status Register (for busy polling and data reading)
<b>Status Bits Affected</b>	1WB (set to 1 for $t_{SLOT}$ ) SBR is updated at $t_{MSR}$ DIR (may change its state)
<b>Configuration Bits Affected</b>	1WS, APU, SPU apply

### Bit Allocation in the Bit Byte

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
V	x	x	x	x	x	x	x

x = don't care

Figure 6. Write-0 Time Slot

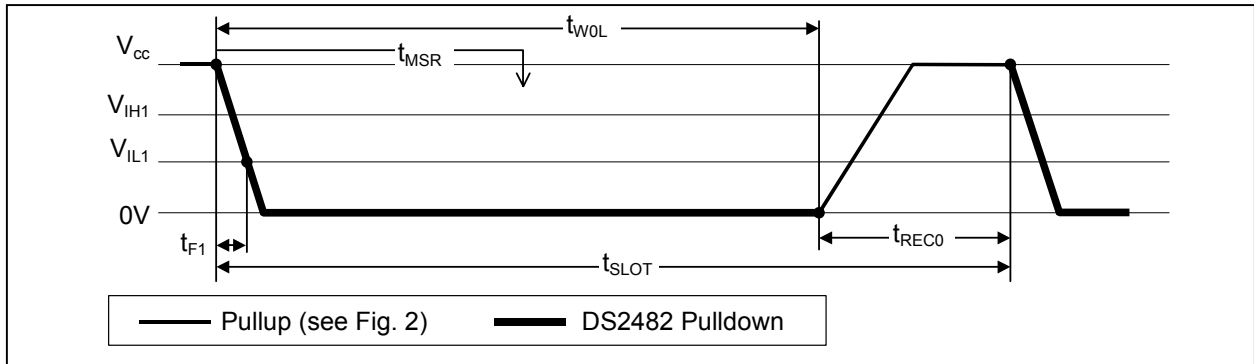
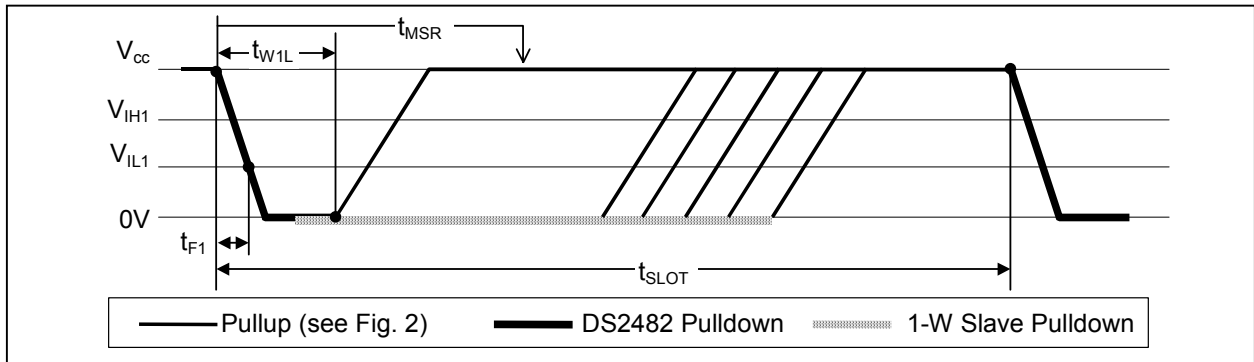


Figure 7. Write-1 and Read-Data Time Slot



**NOTE on Figure 7:** Depending on its internal state, a 1-Wire slave device will transmit data to its master (e.g., the DS2482). When responding with a 0, a 1-Wire slave will start pulling the line low during  $t_{W1L}$ ; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, a 1-Wire slave will not hold the line low at all, and the voltage starts rising as soon as  $t_{W1L}$  is over. 1-Wire device data sheets use the term  $t_{RL}$  instead of  $t_{W1L}$  to describe a read-data time slot. Technically,  $t_{RL}$  and  $t_{W1L}$  have identical specifications and cannot be distinguished from each other.

## 1-Wire Write Byte

<b>Command Code</b>	A5h
<b>Command Parameter</b>	Data Byte
<b>Description</b>	Writes single data byte to selected 1-Wire IO channel.
<b>Typical Use</b>	To write commands or data to a 1-Wire IO channel; equivalent to executing eight 1-Wire Single Bit commands, but faster due to less I <sup>2</sup> C traffic.
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code and data byte will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored.
<b>Command Duration</b>	$8 \times t_{SLOT} + \text{maximum } 262.5\text{ns}$ , counted from falling edge of the last bit (LS bit) of the data byte.
<b>1-Wire Activity</b>	Begins maximum 262.5ns after falling SCL edge of the LS bit of the data byte (i.e., before the data byte acknowledged). <b>NOTE:</b> The bit order on the I <sup>2</sup> C bus and the 1-Wire line is different. (1-Wire: LS-bit first; I <sup>2</sup> C: MS-bit first) Therefore, 1-Wire activity cannot begin before the DS2482 has received the full data byte.
<b>Read Pointer Position</b>	Status Register (for busy polling)
<b>Status Bits Affected</b>	1WB (set to 1 for $8 \times t_{SLOT}$ )
<b>Configuration Bits Affected</b>	1WS, SPU, APU apply

## 1-Wire Read Byte

<b>Command Code</b>	96h
<b>Command Parameter</b>	None
<b>Description</b>	Generates eight read data time slots on the selected 1-Wire IO channel and stores result in the Read Data Register.
<b>Typical Use</b>	To read data from a 1-Wire IO channel; equivalent to executing eight 1-Wire Single Bit commands with $V = 1$ (write 1 time slot), but faster due to less I <sup>2</sup> C traffic.
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored.
<b>Command Duration</b>	$8 \times t_{\text{SLOT}} + \text{maximum } 262.5\text{ns}$ , counted from the falling SCL edge of the command code acknowledge bit.
<b>1-Wire Activity</b>	Begins maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
<b>Read Pointer Position</b>	Status Register (for busy polling) <b>NOTE:</b> To read the data byte received from the 1-Wire IO channel, issue the Set Read Pointer command and select the Read Data Register. Then access the DS2482 in read mode.
<b>Status Bits Affected</b>	1WB (set to 1 for $8 \times t_{\text{SLOT}}$ )
<b>Configuration Bits Affected</b>	1WS, APU apply

## 1-Wire Triplet

<b>Command Code</b>	78h
<b>Command Parameter</b>	Direction Byte
<b>Description</b>	Generates three time slots, two read-time slots and one write time slot, at the selected 1-Wire IO channel. The type of write-time slot depends on the result of the read-time slots and the direction byte. The direction byte determines the type of write-time slot if both read-time slots are 0 (a typical case). In this case the DS2482 will generate a write-1 time slot if $V = 1$ and a write-0 time slot if $V = 0$ . If the read-time slots are 0 and 1, there will follow a write 0 time slot. If the read-time slots are 1 and 0, there will follow a write 1 time slot. If the read-time slots are both 1 (error case), the subsequent write time slot will be a write 1.
<b>Typical Use</b>	To perform a 1-Wire Search ROM sequence; a full sequence requires this command to be executed 64 times to identify and address one device.
<b>Restriction</b>	1-Wire activity must have ended before the DS2482 can process this command.
<b>Error Response</b>	Command code and direction byte will not be acknowledged if 1WB = 1 at the time the command code is received and the command will be ignored.
<b>Command Duration</b>	$3 \times t_{\text{SLOT}} + \text{maximum } 262.5\text{ns}$ , counted from the falling SCL edge of the first bit (MS bit) of the direction byte.
<b>1-Wire Activity</b>	Begins maximum 262.5ns after the falling SCL edge of the MS bit of the direction byte.
<b>Read Pointer Position</b>	Status Register (for busy polling)
<b>Status Bits Affected</b>	1WB (set to 1 for $3 \times t_{\text{SLOT}}$ ) SBR is updated at the first $t_{\text{MSR}}$ TSB and DIR are updated at the second $t_{\text{MSR}}$ (i.e., at $t_{\text{SLOT}} + t_{\text{MSR}}$ )
<b>Configuration Bits Affected</b>	1WS, APU apply

**Bit Allocation in the Direction Byte**

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
V	x	x	x	x	x	x	x

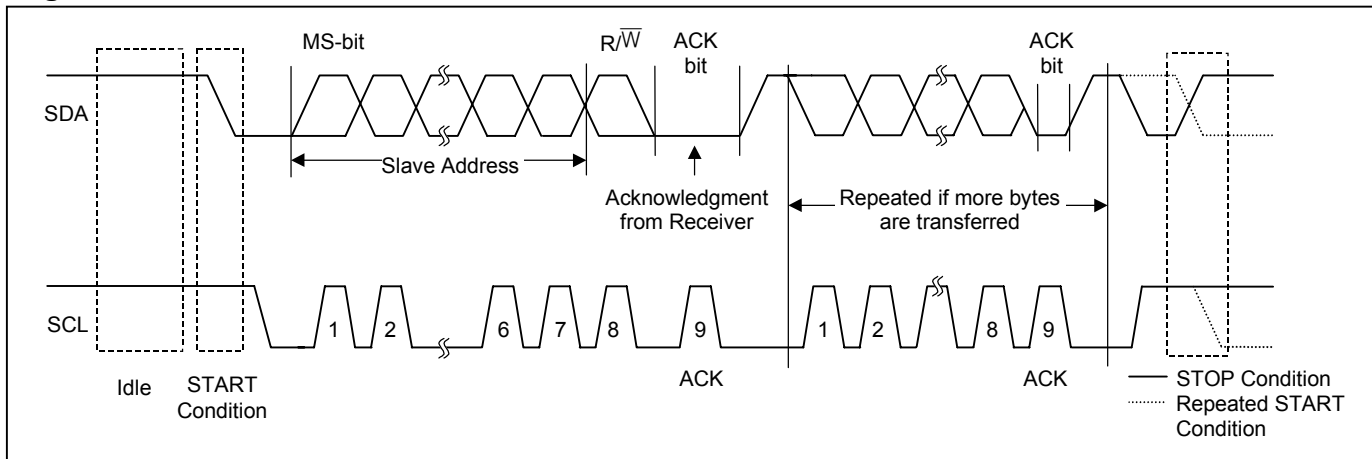
x = don't care

**I<sup>2</sup>C INTERFACE****General Characteristics**

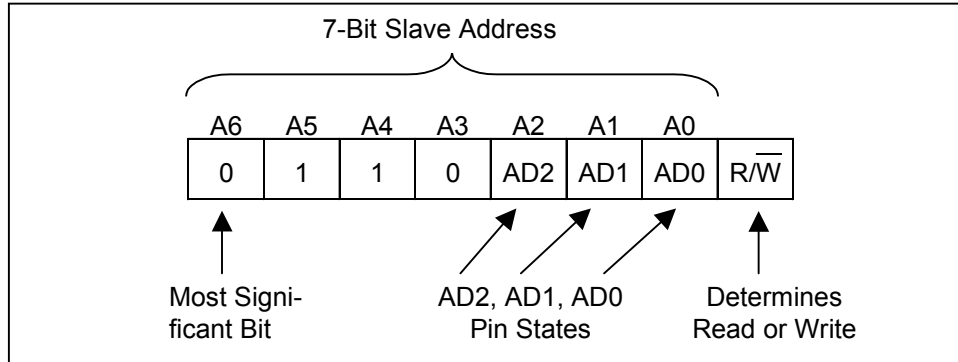
The I<sup>2</sup>C bus uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I<sup>2</sup>C bus can be transferred at rates of up to 100kbps in the Standard-mode, up to 400kbps in the Fast-mode. The DS2482 works in both modes.

A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the communication is called a “master.” The devices that are controlled by the master are “slaves.” To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus.

Data transfers may be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP (Figure 8). Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

**Figure 8. I<sup>2</sup>C Protocol Overview****Slave Address**

The slave address to which the DS2482 responds is shown in Figure 9. The logic states at the address pins AD0, AD1 and AD2 determine the value of the address bits A0, A1, and A2. The address pins allow the device to respond to one of eight possible slave addresses. The slave address is part of the slave-address/control byte. The last bit of the slave-address/control byte ( $R/\overline{W}$ ) defines the data direction. When set to a 0, subsequent data will flow from master to slave (write access); when set to a 1, data will flow from slave to master (read access).

**Figure 9. DS2482 Slave Address****I<sup>2</sup>C Definitions**

The following terminology is commonly used to describe I<sup>2</sup>C data transfers. The timing references are defined in Figure 10.

**Bus Idle or Not Busy:** Both, SDA and SCL, are inactive and in their logic HIGH states.

**START Condition:** To initiate communication with a slave, the master has to generate a START condition. A START condition is defined as a change in state of SDA from HIGH to LOW while SCL remains HIGH.

**STOP Condition:** To end communication with a slave, the master has to generate a STOP condition. A STOP condition is defined as a change in state of SDA from LOW to HIGH while SCL remains HIGH.

**Repeated START Condition:** Repeated starts are commonly used for read accesses to select a specific data source or address to read from. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

**Data Valid:** With the exception of the START and STOP condition, transitions of SDA may occur only during the LOW state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ( $t_{HD:DAT}$  after the falling edge of SCL and  $t_{SU:DAT}$  before the rising edge of SCL, see Figure 10). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum  $t_{SU:DAT} + t_R$  in Figure 10) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

**Acknowledge:** Usually, a receiving device, when addressed, is obliged to generate an acknowledge after the receipt of each byte. The master must generate a clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull SDA LOW during the acknowledge clock pulse in such a way that SDA is stable LOW during the HIGH period of the acknowledge-related clock pulse plus the required setup and hold time ( $t_{HD:DAT}$  after the falling edge of SCL and  $t_{SU:DAT}$  before the rising edge of SCL).

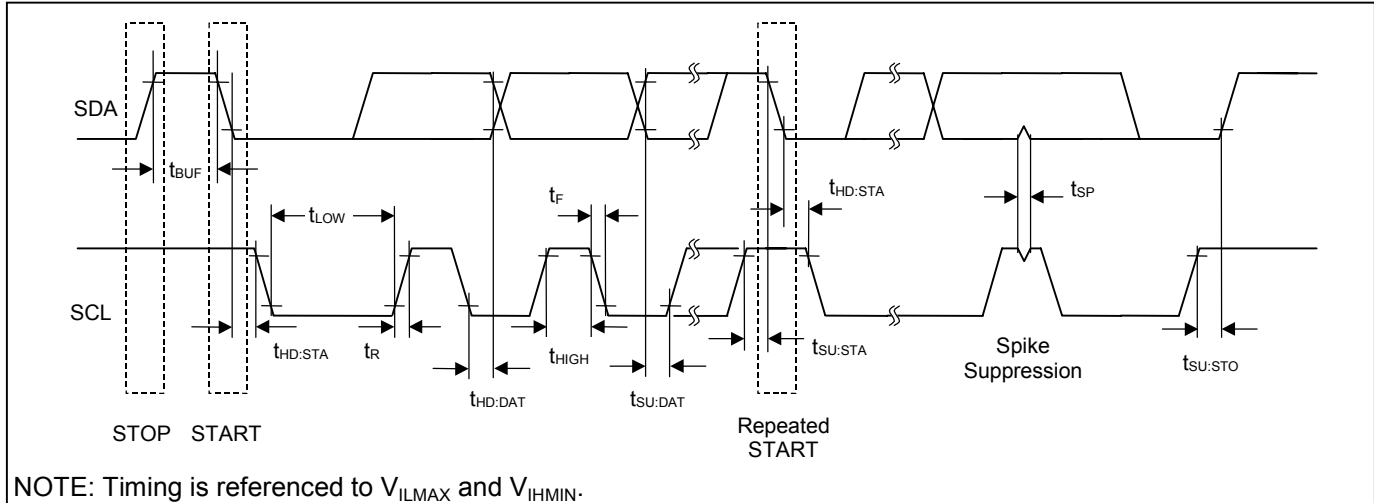
**Not Acknowledged by Slave:** A slave device may be unable to receive or transmit data, e.g., because it is busy performing some real-time function. In this case the slave device will not acknowledge its slave address and leave the SDA line HIGH.

A slave device that is ready to communicate will acknowledge at least its slave address. However, some time later the slave may refuse to accept data, e.g., because of an invalid command code or parameter. In this case the slave device will not acknowledge any of the bytes that it refuses and will leave SDA HIGH. In either case, after a slave has failed to acknowledge, the master first needs to generate a repeated START condition or a STOP condition followed by a START condition to begin a new data transfer.



**Not Acknowledged by Master:** At some time when receiving data, the master must signal an end of data to the slave device. To achieve this, the master does not acknowledge the last byte that it has received from the slave. In response, the slave releases SDA, allowing the master to generate the STOP condition.

**Figure 10. I<sup>2</sup>C Timing Diagram**



### Writing to the DS2482

To write to the DS2482, the master must access the device in write mode, i.e., the slave address must be sent with the direction bit set to 0. The next byte to be sent is a command code, which, depending on the command, may be followed by a command parameter. The DS2482 will acknowledge valid command codes and expected/valid command parameters. Additional bytes or invalid command parameters will never be acknowledged.

### Reading from the DS2482

To read from the DS2482, the master must access the device in read mode, i.e., the slave address must be sent with the direction bit set to 1. The read pointer determines the register that the master will read from. The master may continue reading the same register over and over again, without having to re-address the device, e.g., to watch the 1WB changing from 1 to 0. To read from a different register, the master must issue the Set Read Pointer command and then access the DS2482 again in read mode.

### I<sup>2</sup>C Communication—Legend

SYMBOL	DESCRIPTION
S	START Condition
AD,0	Select DS2482 for Write Access
AD,1	Select DS2482 for Read Access
Sr	Repeated START Condition
P	STOP Condition
A	Acknowledged
A\	Not Acknowledged
(Idle)	Bus Not Busy
<byte>	Transfer of 1 Byte

SYMBOL	DESCRIPTION
DRST	Command "Device Reset", F0h
WCFG	Command "Write Configuration", D2h
CHSL	Command "Channel Select", C3h
SRP	Command "Set Read Pointer", E1h
1WRS	Command "1-Wire Reset", B4h
1WWB	Command "1-Wire Write Byte", A5h
1WRB	Command "1-Wire Read Byte", 96h
1WSB	Command "1-Wire Single Bit", 87h
1WT	Command "1-Wire Triplet", 78h

## Data Direction Codes

Master-to-Slave	Slave-to-Master
-----------------	-----------------

## I<sup>2</sup>C Communication Examples

### Device Reset, e.g., after power-up

S	AD,0	A	DRST	A	<u>Sr</u>	<u>AD,1</u>	<u>A</u>	<u>&lt;byte&gt;</u>	<u>A\</u>	P
---	------	---	------	---	-----------	-------------	----------	---------------------	-----------	---

This example includes an optional read access to verify the success of the command.

### Write Configuration, e.g., before starting 1-Wire activity power-up

Case A: 1-Wire idle (1WB = 0)

S	AD,0	A	WCFG	A	<byte>	A	<u>Sr</u>	<u>AD,1</u>	<u>A</u>	<u>&lt;byte&gt;</u>	<u>A\</u>	P
---	------	---	------	---	--------	---	-----------	-------------	----------	---------------------	-----------	---

This example includes an optional read access to verify the success of the command.

Case B: 1-Wire busy (1WB = 1)

S	AD,0	A	WCFG	A\	P
---	------	---	------	----	---

The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

### Channel Select, e.g., to select another 1-Wire channel

Case A: 1-Wire idle (1WB = 0)

S	AD,0	A	CHSL	A	E1h	A	<u>Sr</u>	<u>AD,1</u>	<u>A</u>	<u>&lt;byte&gt;</u>	<u>A\</u>	P
---	------	---	------	---	-----	---	-----------	-------------	----------	---------------------	-----------	---

E1h is the valid channel selection code for IO1. This example includes an optional read access to verify the success of the command.

Case B: 1-Wire idle (1WB = 0), invalid channel selection code

S	AD,0	A	CHSL	A	E5h	A\	P
---	------	---	------	---	-----	----	---

E5h is an invalid channel selection code.

Case C: 1-Wire busy (1WB = 1)

S	AD,0	A	CHSL	A\	P
---	------	---	------	----	---

The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

### Set Read Pointer, e.g., to read from another register

Case A: valid read pointer code

S	AD,0	A	SRP	A	C3h	A	P
---	------	---	-----	---	-----	---	---

C3h is the valid read pointer code for the configuration register.

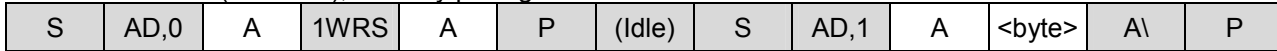
Case B: invalid read pointer code

S	AD,0	A	SRP	A	E5h	A\	P
---	------	---	-----	---	-----	----	---

E5h is an invalid read pointer code.

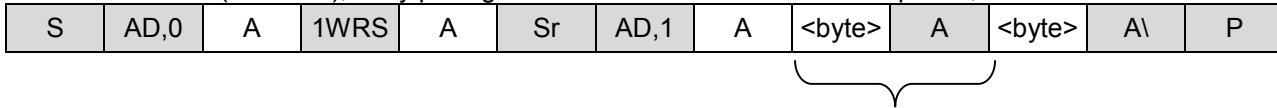
**1-Wire Reset, e.g., to begin or end 1-Wire communication**

Case A: 1-Wire idle (1WB = 0), no busy polling to read the result

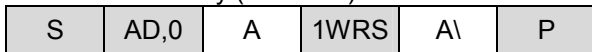


In the first cycle, the master sends the command; then the master waits (Idle) for the 1-Wire Reset to complete. In the second cycle the DS2482 is accessed to read the result of the 1-Wire Reset from the Status Register.

Case B: 1-Wire idle (1WB = 0), busy polling until the 1-Wire Command is completed, then read the result



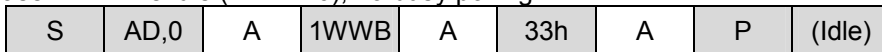
Case C: 1-Wire busy (1WB = 1)



The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

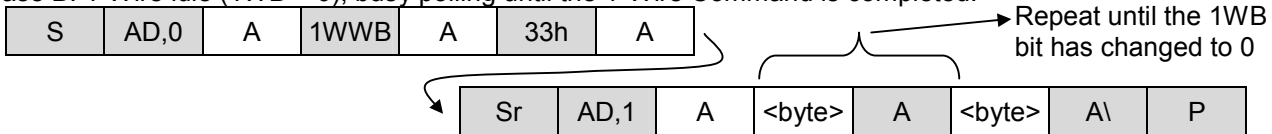
**1-Wire Write Byte, e.g., to send a command code to a 1-Wire IO channel**

Case A: 1-Wire idle (1WB = 0), no busy polling



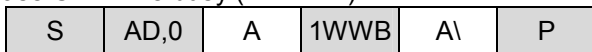
33h is the valid 1-Wire ROM function command for Read ROM. The idle time is needed for the 1-Wire function to complete. There is no data read back from the 1-Wire line with this command.

Case B: 1-Wire idle (1WB = 0), busy polling until the 1-Wire Command is completed.



When 1WB has changed from 1 to 0, the 1-Wire Write Byte command is completed.

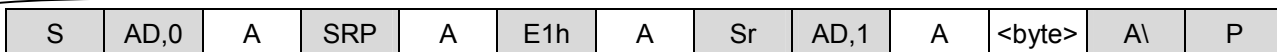
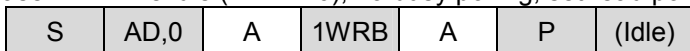
Case C: 1-Wire busy (1WB = 1)



The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

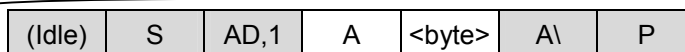
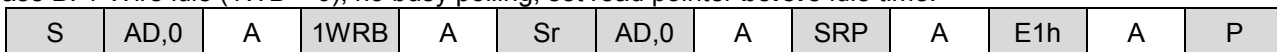
**1-Wire Read Byte, e.g., to read a byte from a 1-Wire IO channel**

Case A: 1-Wire idle (1WB = 0), no busy polling, set read pointer **after** idle time.



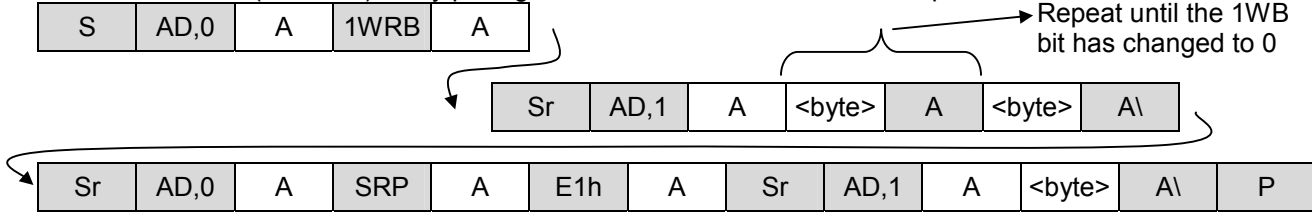
The idle time is needed for the 1-Wire function to complete. Then set the read pointer to the read data register (code E1h) and access the device again to read the data byte that was obtained from the 1-Wire IO channel.

Case B: 1-Wire idle (1WB = 0), no busy polling, set read pointer **before** idle time.



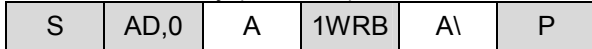
The read pointer is set to the read data register (code E1h) while the 1-Wire Read Byte command is still in progress. Then, after the 1-Wire function is completed, the device is accessed to read the data byte that was obtained from the 1-Wire IO channel.

Case C: 1-Wire idle (1WB = 0), busy polling until the 1-Wire Command is completed.



Poll the Status Register until the 1WB bit has changed from 1 to 0. Then set the read pointer to the read data register (code E1h) and access the device again to read the data byte that was obtained from the 1-Wire IO channel.

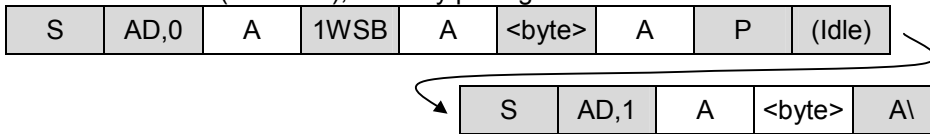
Case D: 1-Wire busy (1WB = 1)



The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

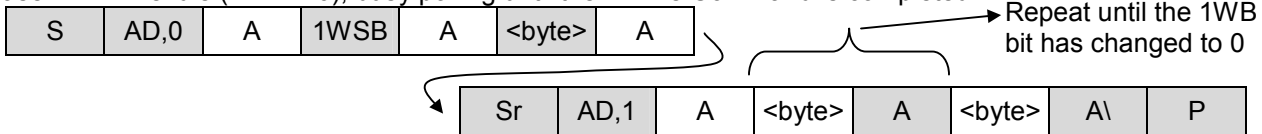
**1-Wire Single Bit, e. g., to generate a single time slot on a 1-Wire IO channel**

Case A: 1-Wire idle (1WB = 0), no busy polling



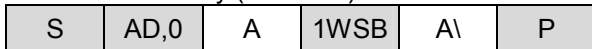
The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire single-bit command.

Case B: 1-Wire idle (1WB = 0), busy polling until the 1-Wire Command is completed.



When 1WB has changed from 1 to 0, the Status Register holds the valid result of the 1-Wire Single Bit command.

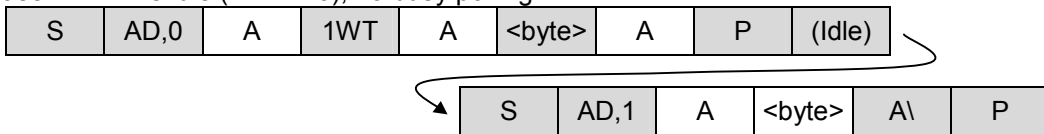
Case C: 1-Wire busy (1WB = 1)



The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

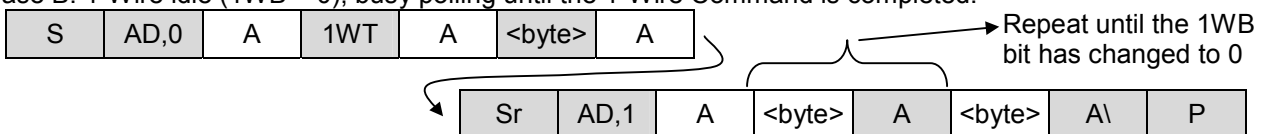
**1-Wire Triplet, e.g., to perform a Search ROM function on a 1-Wire IO channel**

Case A: 1-Wire idle (1WB = 0), no busy polling



The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Triplet command.

Case B: 1-Wire idle (1WB = 0), busy polling until the 1-Wire Command is completed.



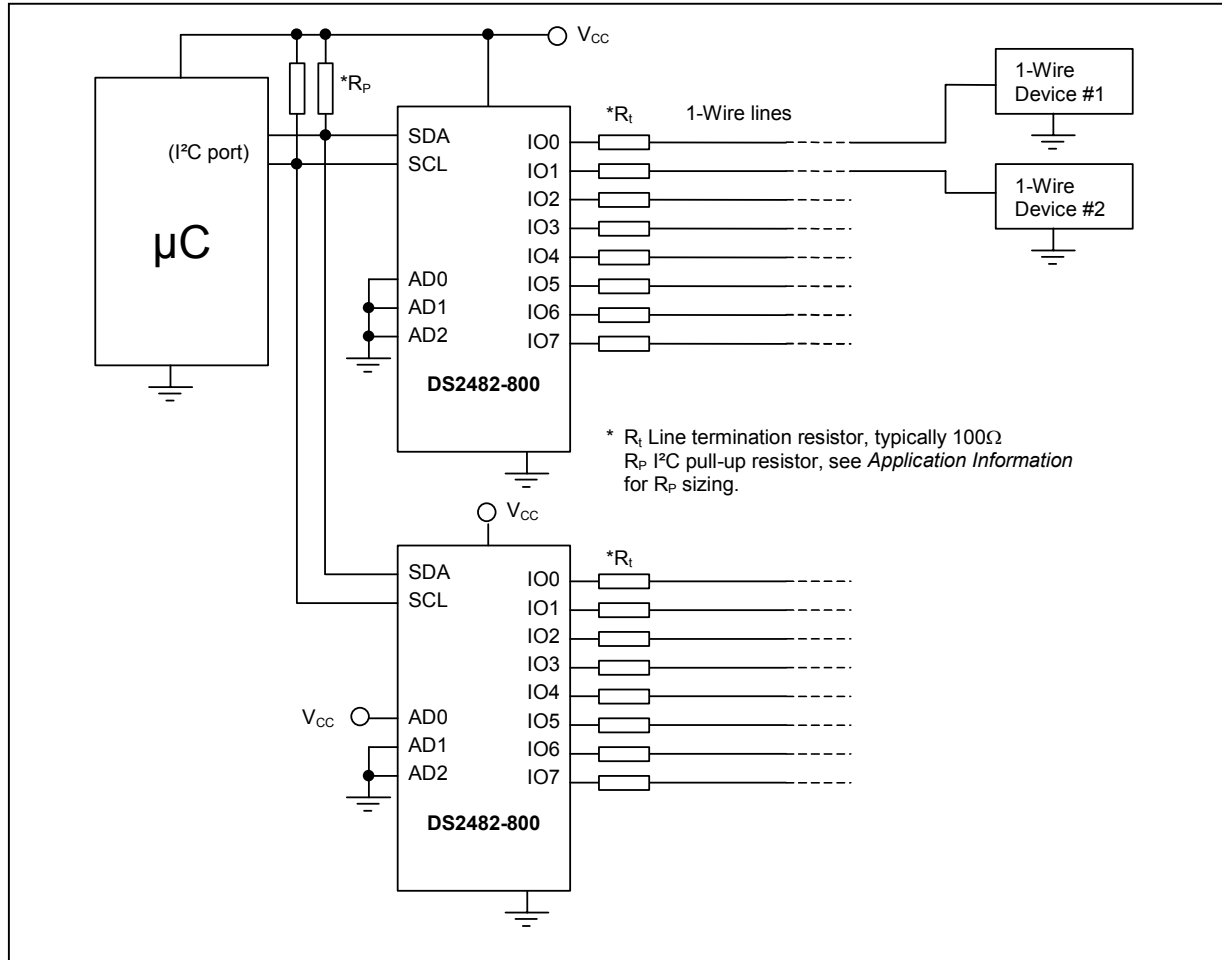
When 1WB has changed from 1 to 0, the Status Register holds the valid result of the 1-Wire Triplet command.

Case C: 1-Wire busy (1WB = 1)

S	AD,0	A	1WT	AI	P
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The master should stop and restart as soon as the DS2482 does not acknowledge the command code.

**Figure 11. Application Schematic**



## Application Information

### SDA and SCL Pullup Resistors

SDA is an open-drain output on the DS2482 that requires a pullup resistor to realize high logic levels. Because the DS2482 uses SCL only as input (no clock stretching) the master can drive SCL either through an open-drain/collector output with a pullup resistor or a push-pull output.

### Pullup Resistor $R_P$ Sizing

According to the I<sup>2</sup>C specification, a slave device must be able to sink at least 3mA at a  $V_{OL}$  of 0.4V. This DC condition determines the minimum value of the pullup resistor:  $R_{pmin} = (V_{CC} - 0.4V)/3mA$ . With an operating voltage of 5.5V, the minimum value for the pullup resistor is 1.7kΩ. The "Minimum RP" line in Figure 12 shows how the minimum pullup resistor changes with the operating voltage.

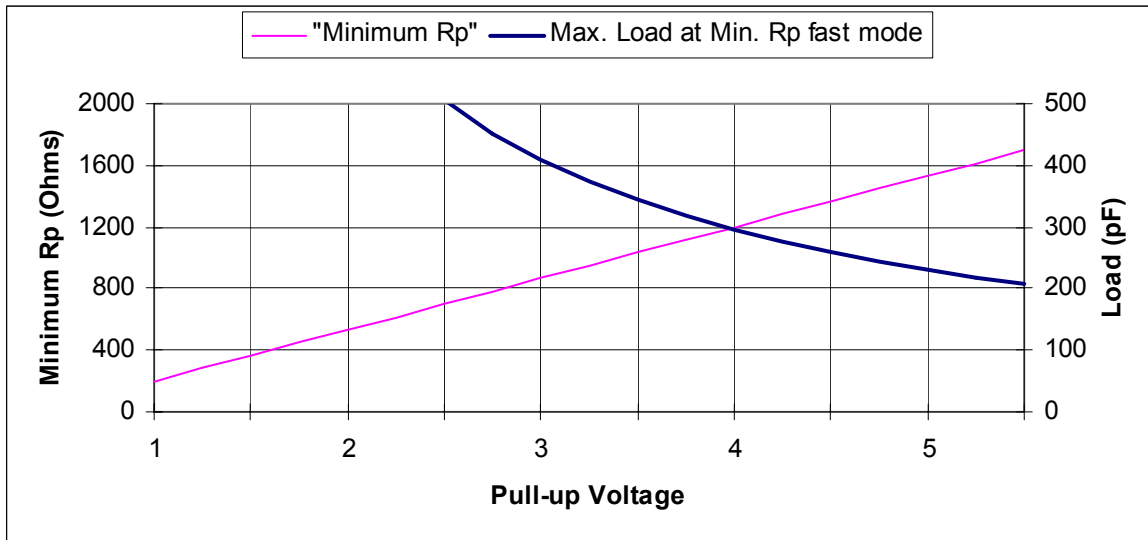
For I<sup>2</sup>C systems, the rise time and fall time are measured from 30% to 70% of the pullup voltage. The maximum bus capacitance  $C_B$  is 400pF. The maximum rise time at standard speed must not exceed 1000ns and 300ns at fast speed. Assuming maximum rise time, the maximum resistor value at any given capacitance  $C_b$  is calculated as:  $R_{pmaxs} = 1000ns/(C_B * \ln(7/3))$  (standard speed) and  $R_{pmaxf} = 300ns/(C_B * \ln(7/3))$  (fast speed). For a bus

capacitance of 400pF the maximum pullup resistor values are 2.95k $\Omega$  at standard speed and 885 $\Omega$  at fast speed. **A value between of 1.7k $\Omega$  and 2.95k $\Omega$  meets all requirements at standard speed.**

Since a 885 $\Omega$  pullup resistor, as would be required to meet the rise time specification at fast speed and 400pF bus capacitance, is lower than  $R_{pmin}$  at 5.5V, a different approach is necessary. The "Max. Load..." line in Figure 12 is generated by first calculating the minimum pullup resistor at any given operating voltage ("Minimum Rp" line) and then calculating the respective bus capacitance that yields a rise time of 300ns.

Only for pullup voltages of 3V and lower can the maximum permissible bus capacitance of 400pF be maintained. A reduced bus capacitance of 300pF is acceptable for pullup voltages of 4V and lower. For fast speed operation at any pullup voltage, the bus capacitance must not exceed 200pF. The corresponding pullup resistor value at the voltage is indicated by the "Minimum Rp" line.

**Figure 12. I<sup>2</sup>C Fast Speed Pullup Resistor Selection Chart**



## PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/DallasPackInfo](http://www.maxim-ic.com/DallasPackInfo).)