# Digital Comb Filter (NTSC/PAL)

Description

The CXD2024AQ is an adaptive comb filter compatible with both NTSC and PAL systems, and can provide high-precision Y/C separation with a single chip.

Features

- Y/C separation by adaptive processing
- Four 1H delay lines
- 8-bit A/D converter (1-channel)
- 8-bit D/A converter (2-channel)
- Clock 4fsc

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

- Supply voltage DV_{DD} Vss−0.5 to +7.0 V
- $AAVD$ Vss−0.5 to +7.0 V
- $ADVD$ Vss−0.5 to +7.0 V
- YV_{DD} Vss−0.5 to +7.0 V
- CV_{DD} Vss−0.5 to +7.0 V
- Input voltage V_I Vss−0.5 to V_{DD}+0.5 V
- Output voltage V_O Vss−0.5 to V_{DD}+0.5 V
- Operating temperature
  Topr −20 to +75 °C
- Storage temperature
  Tstg −55 to +150 °C

80 pin QFP (Plastic)
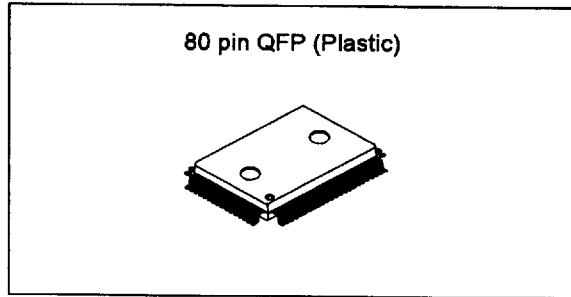
Recommended Operating Conditions

- Supply voltage DV_{DD} 5.0 ±0.25 V
- $AAVD$ 5.0 ±0.25 V
- $ADVD$ 5.0 ±0.25 V
- YV_{DD} 5.0 ±0.25 V
- CV_{DD} 5.0 ±0.25 V
- Analog input $ADIN$ 1.8 Vpp
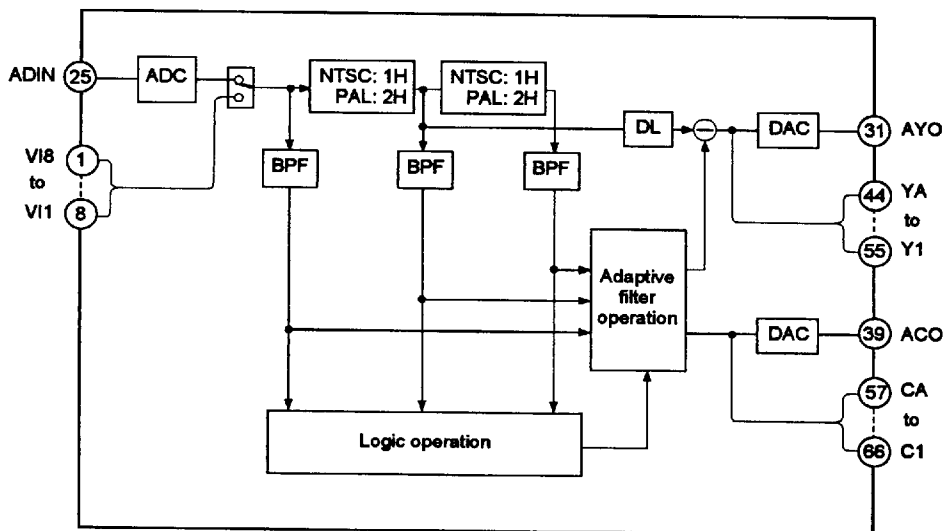- Operating temperature
  Topr −20 to +75 °C

Applications
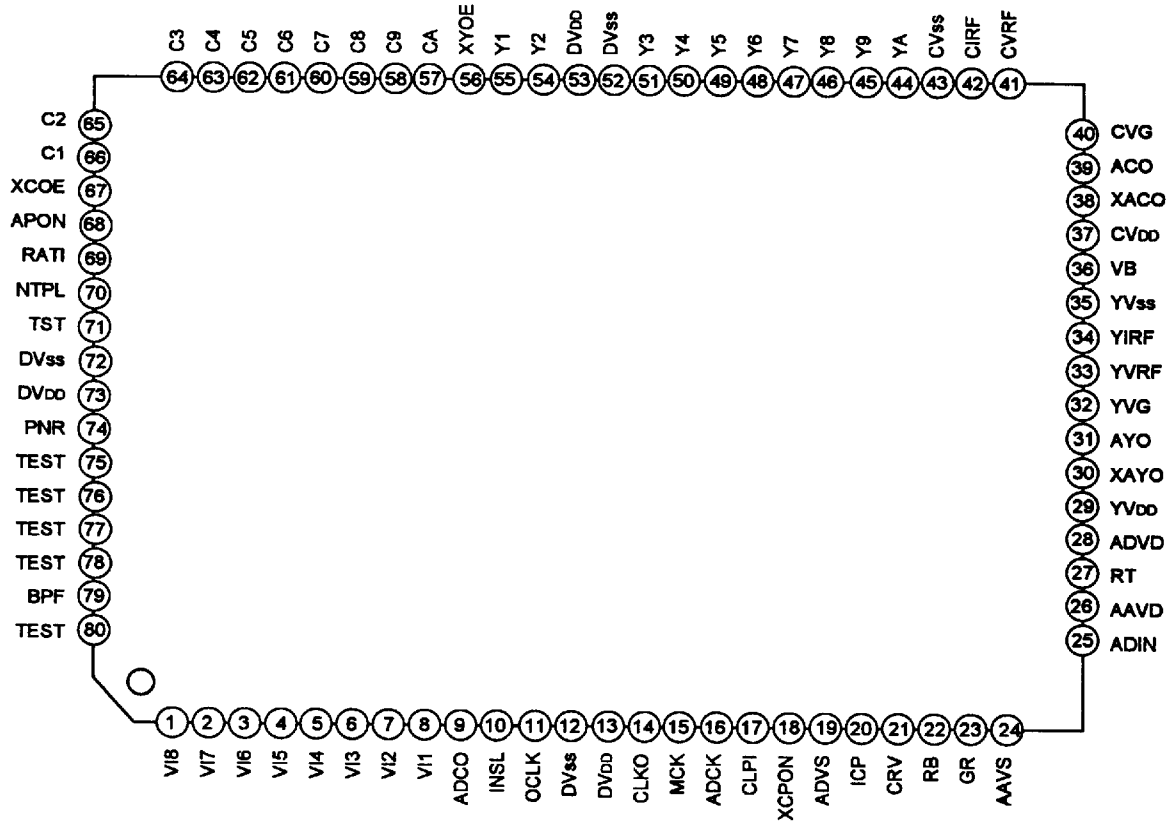
Y/C separation for color TVs and VCRs

Structure

Silicon gate CMOS IC

Block Diagram

E94814-PK

8382383 0009460 134

Pin Configuration

Top row (pins 64–41, left to right): C3 (64), C4 (63), C5 (62), C6 (61), C7 (60), C8 (59), C9 (58), CA (57), XYOE (56), Y1 (55), Y2 (54), DVDD (53), DVss (52), Y3 (51), Y4 (50), Y5 (49), Y6 (48), Y7 (47), Y8 (46), Y9 (45), YA (44), CVss (43), CIRF (42), CVRF (41)

Left column (top to bottom): C2 (65), C1 (66), XCOE (67), APON (68), RATI (69), NTPL (70), TST (71), DVss (72), DVDD (73), PNR (74), TEST (75), TEST (76), TEST (77), TEST (78), BPF (79), TEST (80)

Right column (top to bottom): CVG (40), ACO (39), XACO (38), CVDD (37), VB (36), YVss (35), YIRF (34), YVRF (33), YVG (32), AYO (31), XAYO (30), YVDD (29), ADVD (28), RT (27), AAVD (26), ADIN (25)

Bottom row (pins 1–24, left to right): VI8 (1), VI7 (2), VI6 (3), VI5 (4), VI4 (5), VI3 (6), VI2 (7), VI1 (8), ADCO (9), INSL (10), OCLK (11), DVss (12), DVDD (13), CLKO (14), MCK (15), ADCK (16), CLPI (17), XCPON (18), ADVS (19), ICP (20), CRV (21), RB (22), GR (23), AAVS (24)

Pin Description

Pin No.	Symbol	I/O	Description
1	VI8	I	Digital input (MSB). Connect to DVss or DVDD when not in use.
2	VI7	I	Digital input. Connect to DVss or DVDD when not in use.
3	VI6	I	Digital input. Connect to DVss or DVDD when not in use.
4	VI5	I	Digital input. Connect to DVss or DVDD when not in use.
5	VI4	I	Digital input. Connect to DVss or DVDD when not in use.
6	VI3	I	Digital input. Connect to DVss or DVDD when not in use.
7	VI2	I	Digital input. Connect to DVss or DVDD when not in use.
8	VI1	I	Digital input (LSB). Connect to DVss or DVDD when not in use.

Pin No.	Symbol	I/O	Description
9	ADCO	I	A/D converter output through mode High : Video signals taken in from A/D converter (input pin: ADIN) are output without change from the Y output pins (YA to Y3) as 8-bit digital data with a 3.5 clock delay. Low : Standard mode
10	INSL	I	Input switching. Switching input data of comb filter. High : Digital input Low : Analog input
11	OCLK	I	Clock amplifier input. Input 0.8Vp-p or more by eliminating DC components with a capacitor .
12	DVss	—	Digital ground
13	DVDD	—	Digital power supply (5V)
14	CLKO	O	Clock amplifier output
15	MCK	I	Master clock input. Input 4fsc clock locked to the color burst. Normally connect clock amplifier output (CLKO: Pin 14).
16	ADCK	I	Clock input for A/D converter. Input the same clock as master clock (MCK: Pin 15). Normally connect clock amplifier output (CLKO: Pin 14).
17	CLPI	I	Clamp pulse input for A/D converter. Clamps the signal voltage of the clamp pulse during the low interval. When the clamp function is off, connect to digital power supply (DVDD).
18	XCPON	I	Clamp setting for A/D converter. High : Clamp function is set to off, and normal A/D converter function is only enabled. Low : Clamp function is enabled.
19	ADVS	—	Digital ground for A/D converter
20	ICP	I	Clamp control voltage integration pin. Connect capacitor of approximately 0.01µF. When not using clamp, connect to analog ground (ADVS).
21	CRV	I	Clamp reference voltage input. Operates for the clamp interval input voltage to be equal to the reference voltage. When not using clamp, connect to analog ground (ADVS).
22	RB	O	Reference voltage (bottom): 0.5V (typ.)
23	GR	—	Guard ring. Connect to analog ground (AAVS).
24	AAVS	—	Analog ground for A/D converter
25	ADIN	I	Comb filter analog input (A/D converter input)
26	AAVD	—	Analog power supply for A/D converter (5V)
27	RT	O	Reference voltage (top): 2.6V (typ.)
28	ADVD	—	Digital power supply for A/D converter (5V)
29	YVDD	—	Analog power supply for Y D/A converter (5V)
30	XAYO	I	AYO inverted current output. Connect to analog ground (YVss).
31	AYO	O	Analog luminance signal output. Output can be obtained by connecting resistance.

Pin No.	Symbol	I/O	Description
32	YVG	O	Connect capacitor of approximately 0.1µF.
33	YVRF	I	Sets the full-scale value of the analog luminance signal.
34	YIRF	O	Connect resistance of "16R" (16 times the output resistance "R" of AYO pin).
35	YVss	—	Analog ground for Y D/A converter
36	VB	O	Connect capacitor of approximately 0.1µF.
37	CV$_{DD}$	—	Analog power supply for C D/A converter (5V)
38	XACO	I	ACO inverted current output. Connect to analog ground (CVss).
39	ACO	O	Analog chroma signal output. Output can be obtained by connecting resistance.
40	CVG	O	Connect capacitor of approximately 0.1µF.
41	CVRF	I	Sets the full-scale value of the analog chroma signal.
42	CIRF	O	Connect a resistance of 16 times "16R" against the output resistance "R" of ACO pin.
43	CVss	—	Analog ground for C D/A converter
44	YA	O	Digital luminance signal output (MSB)
45	Y9	O	Digital luminance signal output
46	Y8	O	Digital luminance signal output
47	Y7	O	Digital luminance signal output
48	Y6	O	Digital luminance signal output
49	Y5	O	Digital luminance signal output
50	Y4	O	Digital luminance signal output
51	Y3	O	Digital luminance signal output
52	DVss	—	Digital ground
53	DV$_{DD}$	—	Digital power supply (5V)
54	Y2	O	Digital luminance signal output
55	Y1	O	Digital luminance signal output (LSB)
56	XYOE	I	Digital luminance signal output control High : High impedance Low : Standard output
57	CA	O	Digital chroma signal output (MSB)
58	C9	O	Digital chroma signal output
59	C8	O	Digital chroma signal output
60	C7	O	Digital chroma signal output
61	C6	O	Digital chroma signal output
62	C5	O	Digital chroma signal output
63	C4	O	Digital chroma signal output
64	C3	O	Digital chroma signal output
65	C2	O	Digital chroma signal output
66	C1	O	Digital chroma signal output (LSB)

Pin No.	Syymbol	I/O	Description
67	XCOE	I	Digital chroma signal output control. High : High impedance Low : Standard output
68	APCN	I	Aperture compensation. High : Compensates for the aperture-induced frequency response characteristics degradation. Even in through mode (TST: ON), aperture compensation is performed for the Y output. Low : Standard mode
69	RATI	I	Ratio setting High : PAL When PNR: ON, compulsively fix to Low internally. Low : NTSC
70	NTPL	I	NTSC/PAL mode setting High : PAL Low : NTSC
71	TST	I	Y output through mode. High : Outputs the input composite video signal from the Y output. At this time, there is 1H (for NTSC, 2H for PAL) +18 clock delay for input (for digital input). For C output, Y/C separated chroma signal is output. Low : Y/C separation mode
72	DVss	—	Digital ground
73	DVDD	—	Digital power supply (5V)
74	PNR	I	PAL High : Small dot interference Low : Before improving dot interference NTSC Fix to "Low".
75	TEST	I	Test. Fix to "Low".
76	TEST	I	Test. Fix to "Low".
77	TEST	I	Test. Fix to "Low".
78	TEST	I	Test. Fix to "Low".
79	BPF	I	Y/C separation processing mode setting. High : Fix to BPF separation mode Low : Adaptive processing mode
80	TEST	I	Test. Fix to "Low".

Electrical Characteristics

DC Characteristics

$(V_{DD} = 4.75$ to $5.25V$, $V_{SS} = 0V$, $Ta = -20$ to $+75°C)$

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit	Applied pins
Supply voltage	V_{DD}	—	4.75	5.0	5.25	V	*1
	AAVD						
	ADVD						
	YV_{DD}						
	CV_{DD}						
Operating temperature	Topr	—	−20		+75	°C	
Input and output voltage	V_I, V_O	—	V_{SS}		V_{DD}	V	*2
Input voltage	V_{IH}	CMOS level input	$0.7V_{DD}$			V	*3
	V_{IL}				$0.3V_{DD}$		
Input leak current	I_I	$V_{IN} = V_{SS}$ or V_{DD}	−10		10	µA	*1
Input rise/fall time	tr, tf	—	0		500	ns	*1
Output voltage	V_{OH}	$I_{OH} = -2mA$	V_{DD}−0.8			V	*4
		$I_{OH} = -4mA$					*5
	V_{OL}	$I_{OL} = 4mA$			0.4		*4
		$I_{OL} = 8mA$					*5
Logical Vth	LVth			$V_{DD}/2$		V	*6
Input voltage	V_{IH}	—	$0.7V_{DD}$			V	
	V_{IL}				$0.3V_{DD}$		
Input amplitude	V_{IN}	fmax = 50MHz sine wave	0.8			Vpp	
Feedback resistor	R_{FB}	$V_{IN} = V_{SS}$ or V_{DD}	250K	1M	2.5M	Ω	
Clock amplifier output delay	—	—	3.0	9.0	18.0	ns	*5

*1 Entire pins

*2 Entire pins other than *6
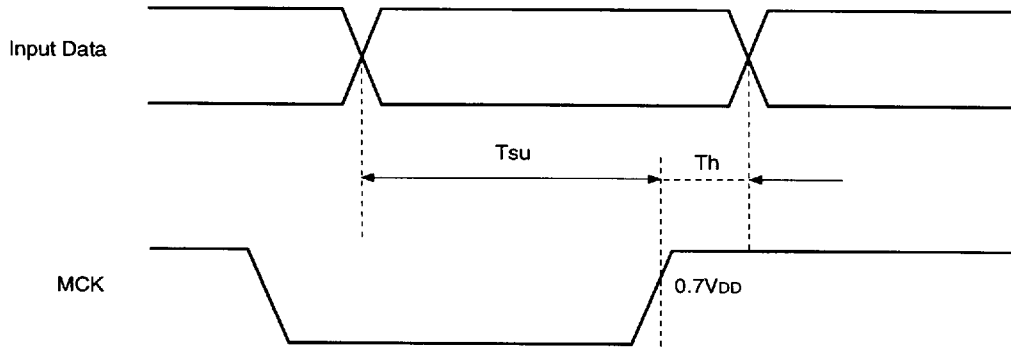
*3 Entire input pins other than *6

*4 Entire output pins other than *5
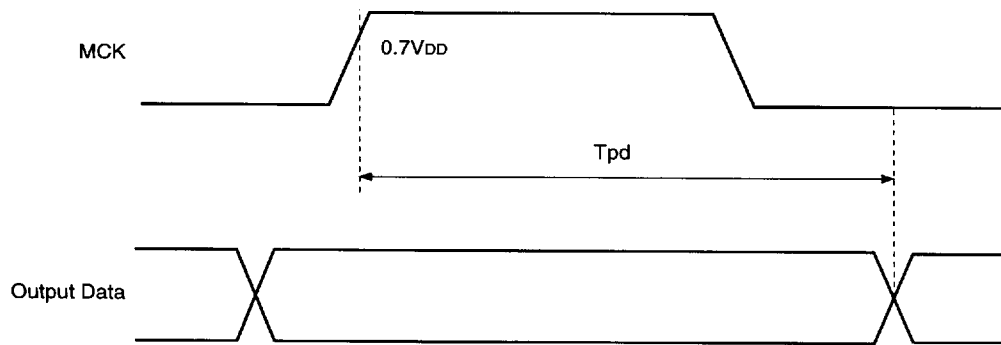
*5 CLKO (Pin 14)

*6 OCLK (Pin 11)

AC Characteristics

Input Interface Timing

(VDD = 4.75 to 5.25V, Vss = 0V, Ta = −20 to +75°C)

Input pins	Pin No.	Min.		Unit	Remarks
		Tsu	Th		
VI8 to VI1	8 to 1	20.00	10.00	ns	Rising edge of MCK is as a reference.

Output Interface Timing

(VDD = 4.75 to 5.25V, Vss = 0V, Ta = −20 to +75°C)

Output pins	Symbol	Tpd (output load capacitance 20 [pF])		Unit	Remarks
YA to Y1	44 to 55	Max.	35.0	ns	Rising edge of MCK is as a reference. Excluding Pins 52 and 53.
		Min.	6.0		
CA to C1	57 to 66	Max.	35.0	ns	Rising edge of MCK is as a reference.
		Min.	6.0		

Clock Frequency   (V$_{DD}$ = 4.75 to 5.25V, V$_{SS}$ = 0V, Ta = −20 to +75°C)

Input pins	Pin No.	Symbol	Min.	Typ.	Max.	Unit
OCLK, MCK, ADCK	11, 15, 16	f	14	4fsc	15	MHz

Pin Capacitance   (Ta = 25°C, f = 1MHz, V$_{IN}$ = V$_{OUT}$ = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C$_{IN}$	—	—	9	pF
Output pin capacitance	C$_{OUT}$	—	—	11	

Internal 8-bit ADC Characteristics   (V$_{DD}$ = 5V, Ta = 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		18	—	—	MSPS
Analog input bandwidth	BW	−3dB	—	18	—	MHz
Self bias	VRB		0.48	0.52	0.56	V
	VRT–VRB		1.96	2.08	2.22	V
Propagation delay time	tpd		—	—	45	ns
Differential linearity error	E$_D$		|1.0	—	+1.0	LSB
Integral linearity error	E$_L$		|3.0	—	+3.0	LSB
Clamp offset voltage	E$_{OC}$	V$_{REF}$ = VRB	|20	0	+20	mV
		V$_{REF}$ = VRT	|30	|10	+10	mV

Internal 8-bit DAC Characteristics   (V$_{DD}$ = 5V, V$_{REF}$ = 2V, R = 200Ω, Ta 25°C, f = 10MHz)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	n		—	8	—	bit
Max. conversion speed	fmax		18	—	—	MSPS
Differential linearity error	E$_D$		−1.0	—	+1.0	LSB
Integral linearity error	E$_L$		−3.0	—	+3.0	LSB
Output full-scale voltage	V$_{FS}$		1.9	2.0	2.1	V
Output full-scale current	I$_{FS}$		—	10	15	mA
Output offset voltage	V$_{OS}$		—	—	1.0	mV
Glitch energy	G$_E$	When R = 75Ω	—	30	—	pV-s

Description of Operation

The CXD2024AQ is an NTSC and PAL compatible IC which, through adaptive (two-dimensional) processing, offers higher performance digital Y/C separation than conventional line combs.
Moreover, two-dimensional processing permits systems to be implemented at a far lower cost than is possible with three-dimensional processing.

In the case of NTSC, a conventional simple line comb always causes an error in vertical non-correlated section because it calculates non-correlated signal together as shown in Fig.1. In order to avoid the occurrences of calculating non-correlated signals together, the CXD2024AQ is provided with two line combs for Y/C separation of a line signal. One line comb calculates its line signals and the signals of the line upper that one (referred to as the upper line comb for the sake of convenience), while the other line comb calculates its line signals and the signals of the line lower that one (contrastingly referred to as the lower line comb). These line combs are used according to the signal correlation.
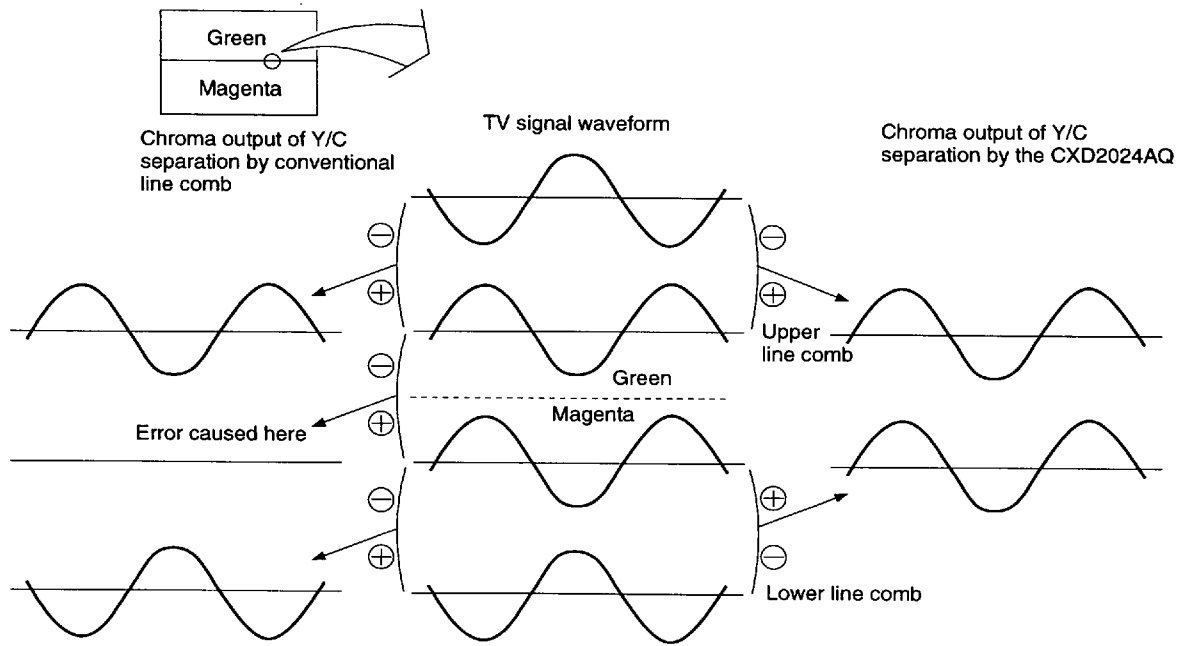
Fig. 1

When, as is the case in Fig.2 for example, only a single line is colored, an error is caused on both the upper and the lower line combs. In the case like this where the vertical frequency is high but the horizontal frequency is low, Y/C separation is performed with band-pass filter and trap.
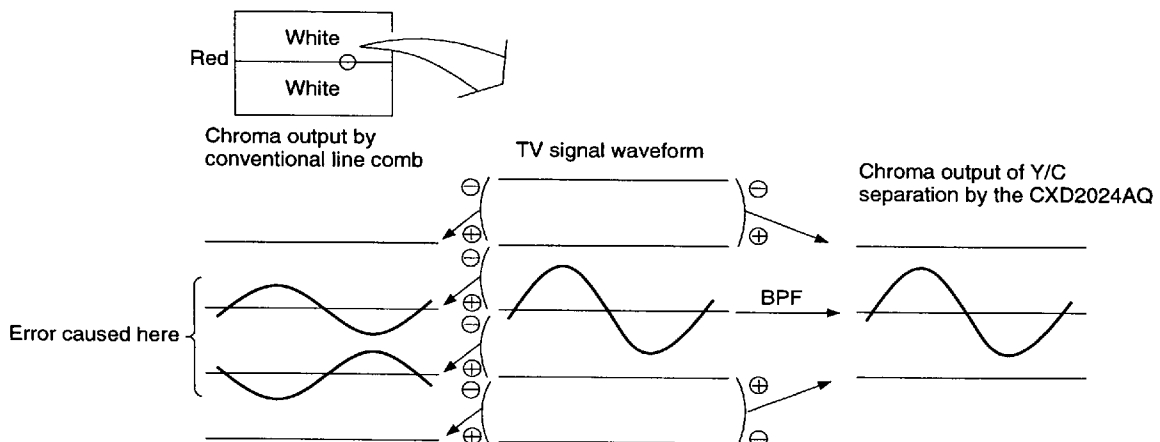

Fig. 2

When both the vertical and horizontal frequencies are high, and the vertical correlation is strong, the 2H comb output is derived by averaging the upper and lower comb outputs.

In this manner, by determining and selecting the optimum output among the upper comb, lower comb, 2H comb and band-pass filter on the basis of signal correlation, much higher precision in Y/C separation can be achieved than that in conventional line combs.

In addition, digital implementation eliminates ringing and others that used to occur in conventional glass delay lines.

In the case of PAL, Y/C separation with conventional band-pass filter and trap filtering exhibited problems such as considerable cross color and degraded frequency response characteristics. The use of the CXD2024AQ solves these problems without any side effects.

Summary of Advantages Offered by the CXD2024AQ
(1) Reduces the number of parts because of the built-in A/D (one-channel) and D/A (two-channel) converters.
(2) Achieves much higher precision in Y/C separation than that in conventional line combs.
(3) Reduces the number of parts in general sets for overseas because of NTSC/PAL compatibility.
(4) Reduces cross color and improves frequency response characteristics when used with PAL.
(5) Digital implementation eliminates ringing encountered in glass delay lines.
(6) Lightens the burden on manufacturing lines by eliminating the need for comb adjustment.

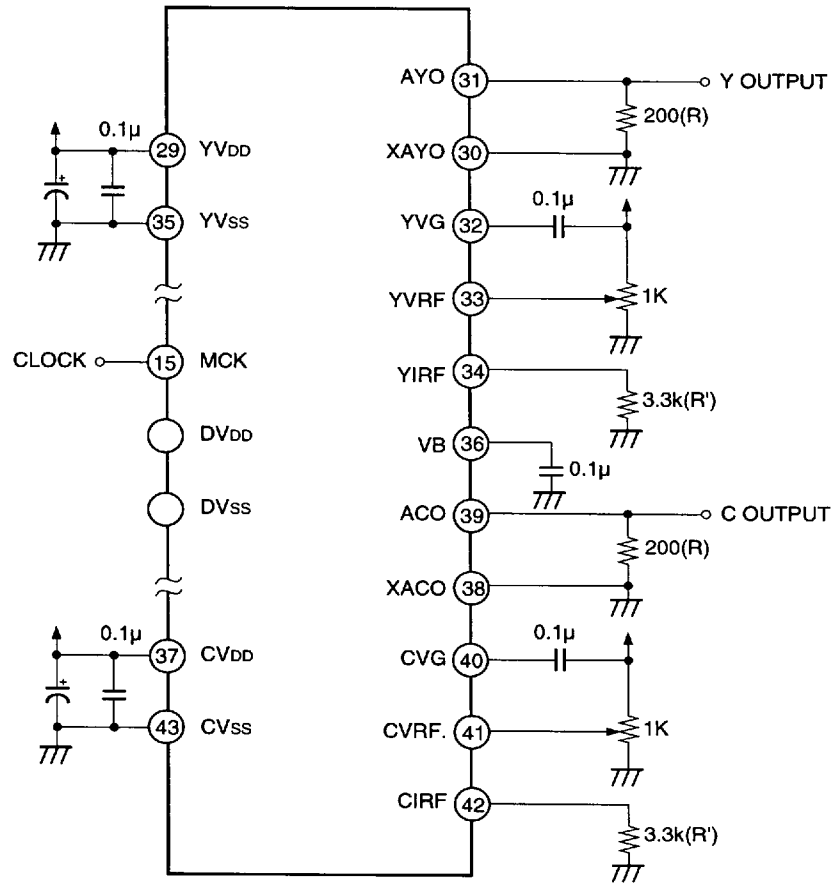## Application Circuit of A/D Converter Block

(1) In the case of inputting clamp pulse directly
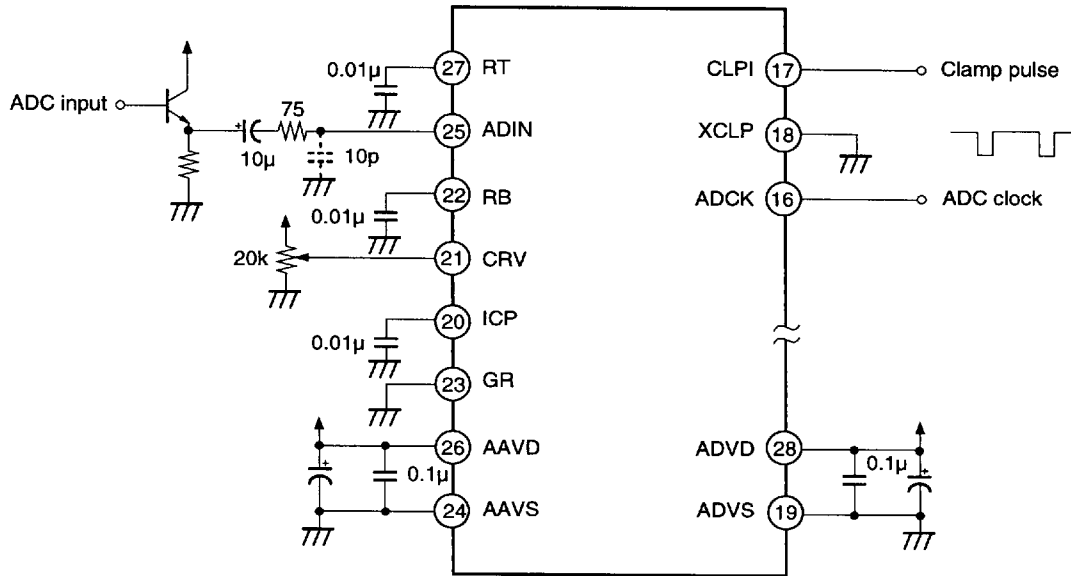
(2) In the case of not using the internal clamp circuit
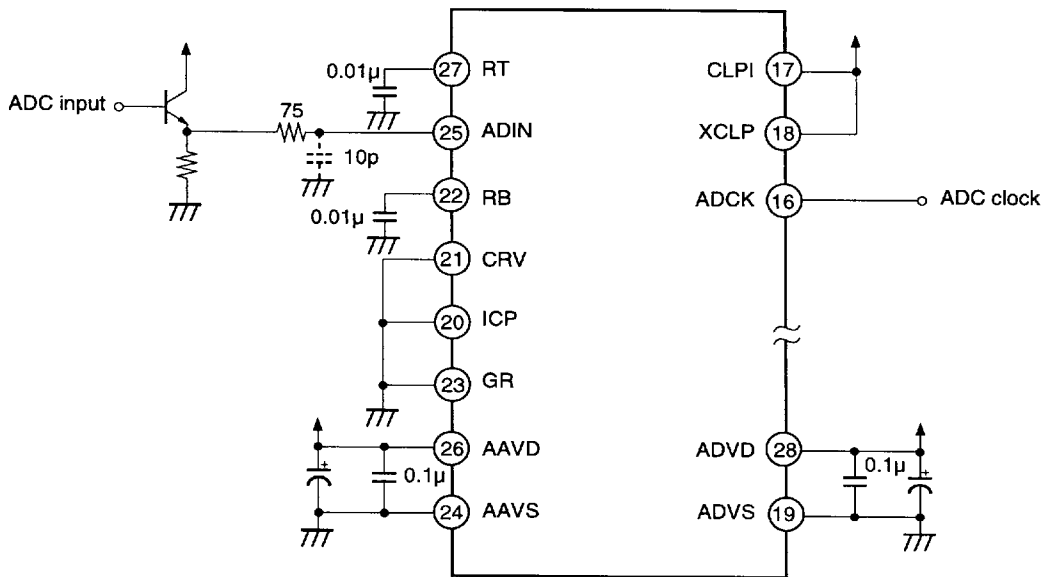
Application Circuit of D/A Converter Block

• **Method of selecting output resistance**

The CXD2024AQ has a built-in current output type D/A converter. To obtain the output voltages, connect resistances to AYO and ACO pins.

The voltage and current specs are as follows.

   Output full-scale voltage: V_{FS} = 0.5 to 2.0V

   Output full-scale current: I_{FS} = 0 to 15mA

Calculate the output using the relationship V_{FS} = I_{FS} × R. In addition, connect a resistance of 16 times the output resistance to the reference current pin (I_{REF}). In the case where the value comes to be impractical, use a value of resistance as close to the calculated value as possible.

Note that, at this time, V_{FS} = V_{RF} × 16R/R' (V_{RF}: Pin voltage of YVRF and CVRF).

Where, R is the resistance connected to I/O, and R' is the resistance connected to I_{RF}. Power consumption can be reduced by using higher resistance values, but glitch energy and data settling time increase contrastingly. Set the optimum values according to the system applications.

• **V_{DD}, V_{SS}**

Separate the analog and digital systems around the device to reduce noise effect. YV_{DD} and CV_{DD} are respectively by-passed to YV_{SS} and CV_{SS} as close to each other as possible through ceramic capacitor of approximately 0.1μF.
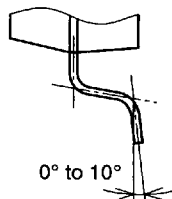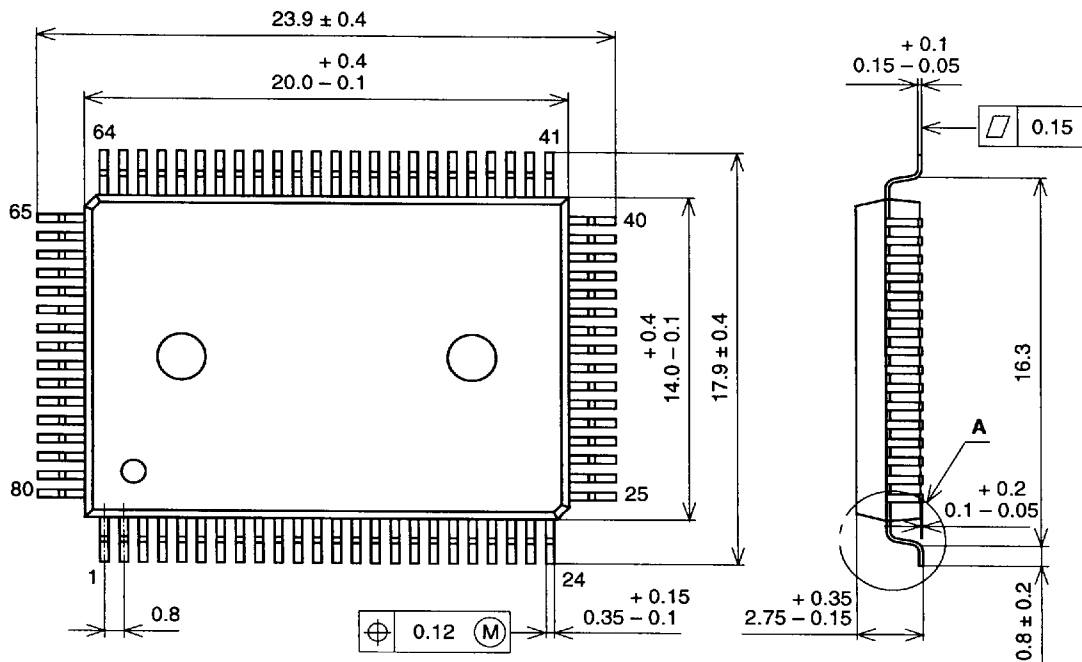
Application Circuit
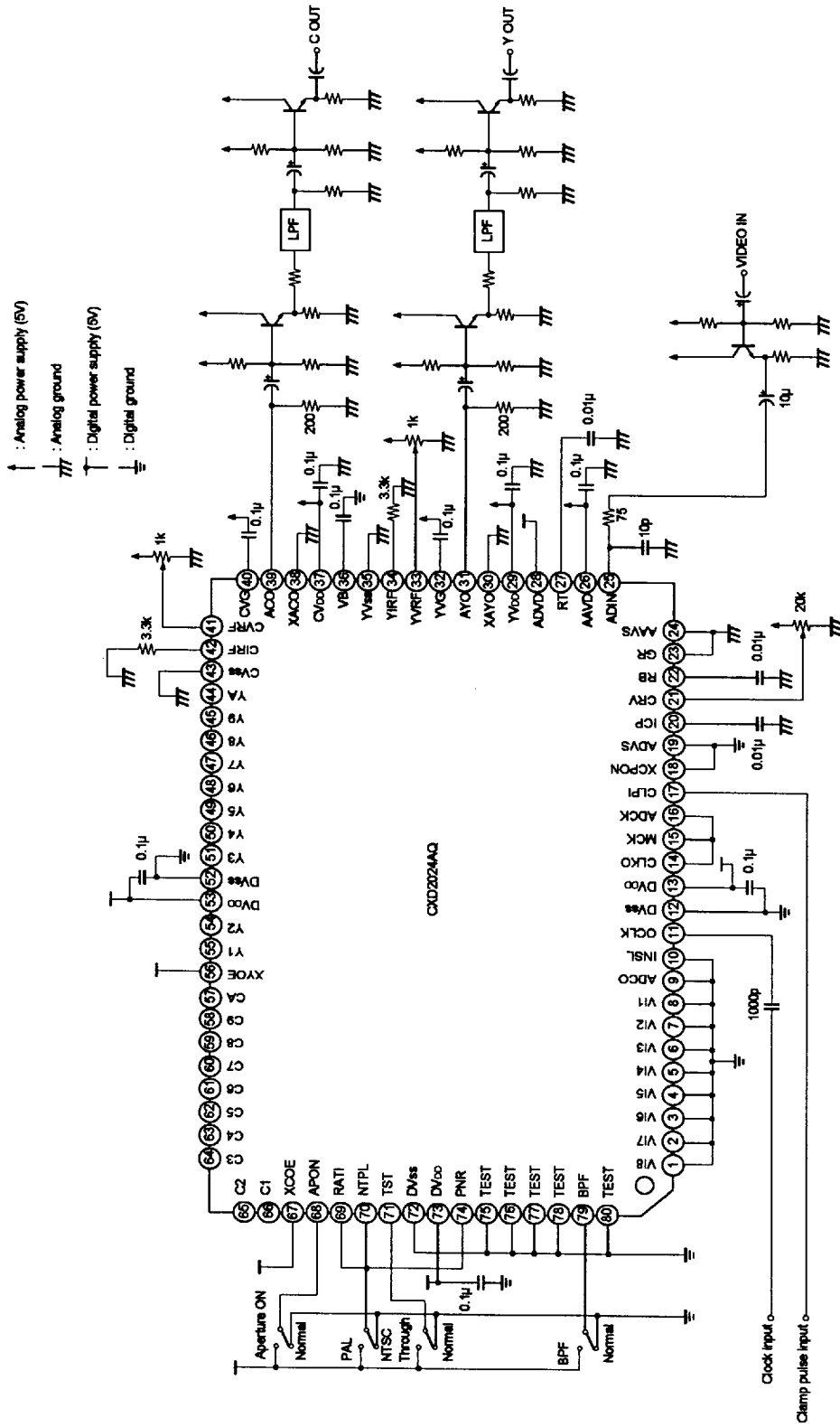
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline   Unit: mm

80PIN QFP (PLASTIC)

DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g