SKY73126-31: 161.92 MHz High Performance VCO/Synthesizer

Applications

- 3GPP Long-Term Evolution systems
- General purpose RF systems

Features

- Fixed 161.92 MHz operation frequency
- Integer N synthesizer
- Reference frequency selection: 10 MHz or 32 MHz
- Integrated voltage regulator, 3.3 V
- Typical +10 dBm output power
- Three-wire serial interface
- Integrated harmonic filter
- Integrated metal shield provides high EMI protection
- MCM (16-pin, 11.4 x 15 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

NEW ▶ Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

Description

Skyworks SKY73126-31 Voltage-Controlled Oscillator (VCO)/Synthesizer is a fully integrated, high performance signal source for base station transceivers. The device provides low phase-noise performance for 3G base station transceivers and general RF system applications.

The SKY73126-31 VCO/Synthesizer is a key building block for high performance radio system designs that require low power and low phase noise. The device provides a fixed 161.92 MHz frequency source output. A 10 MHz or 32 MHz reference clock frequency could be used for this device.

The integer-N Phase Locked Loop (PLL), loop filter, VCO, varactor, frequency divider and output buffer are integrated inside the device. An integrated 3.3 V voltage regulator provides superior phase-noise performance. The SKY73126-31 is programmed through a three-wire Serial Peripheral Interface (SPI).

The SKY73126-31 VCO/Synthesizer is provided in a compact, 16-pin Multi-Chip Module (MCM). The device package and pinout are shown in Figure 1. A functional block diagram is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.
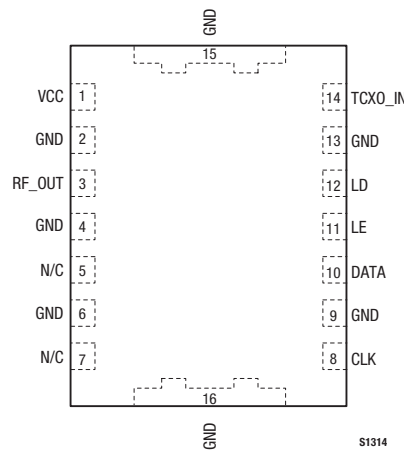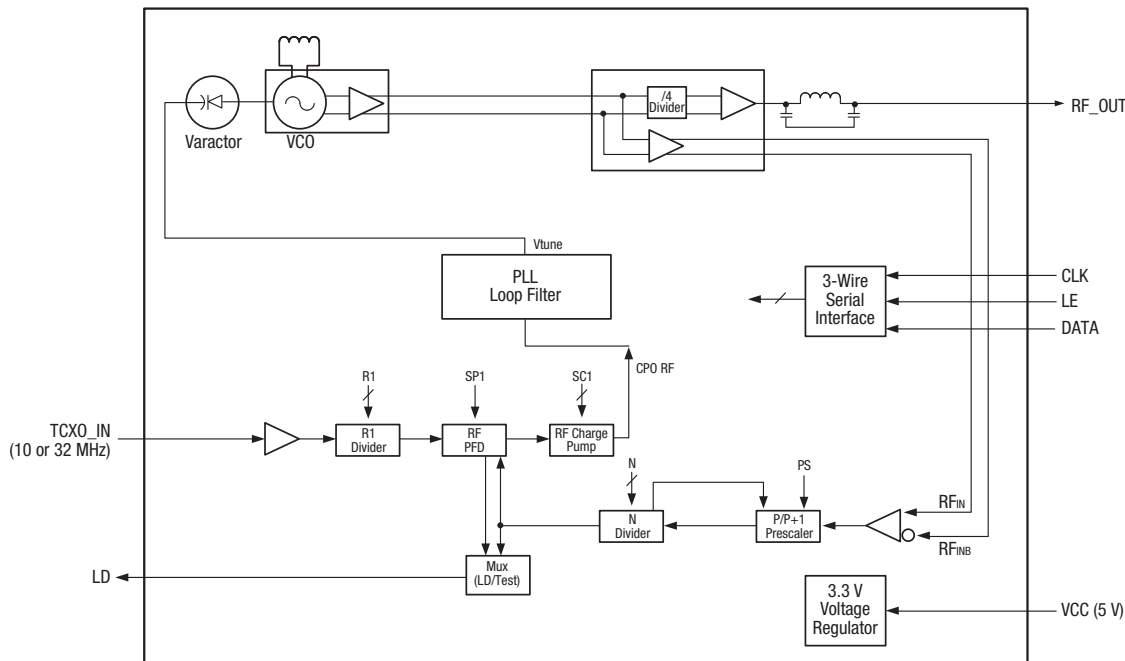

Figure 1. SKY73126-31 Pinout– 17-Pin MCM Package (Top View)

Figure 2. SKY73126-31 Functional Block Diagram

Table 1. SKY73126-31 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	VCC	+5 V DC power supply	9	GND	Ground
2	GND	Ground	10	DATA	Serial port SPI data input (master out slave in)
3	RF_OUT	RF output	11	LE	Serial port latch enable
4	GND	Ground	12	LD	Lock detect output
5	N/C	No connection	13	GND	Ground
6	GND	Ground	14	TCXO_IN	Frequency reference input
7	N/C	No connection	15	GND	Ground
8	CLK	Serial port clock	16	GND	Ground

Technical Description

The SKY73126-31 is a BiCMOS integer-N synthesizer that offers high performance, low cost, and low power consumption. The device also provides programmable charge pump gain.

Serial I/O Control Interface

The SKY73126-31 is programmed through a three-wire serial bus control interface. The three-wire interface consists of three signals: CLK (pin 8), LE (pin 11), and the bit serial data line DATA (pin 10). A serial data input timing diagram is shown in Figure 3. Timing parameter values are provided in Table 2.

Figure 4 depicts the serial bus, which consists of one 32-bit load register and four separate 28-bit hold registers. Data is initially clocked into the load register starting with the Most Significant Bit (MSB) and ending with the Least Significant Bit (LSB).

The LE signal is used to gate the clock to the load register, requiring the LE signal to be brought low before the data load. Data is shifted on the rising edge of CLK. The falling edge of LE latches the data into the appropriate hold register from the load register. This programming sequence must be repeated to fill all four hold registers.

The specific hold register addresses are determined by the wd_0, wd_1, wd_2, and wd_3 parameters in the load register. These are the four LSBs (bits [3:0]) as shown in Figure 4. Table 3 lists the four hold registers and their respective addresses as determined in the load register.

The contents of each word in the load register are used to program the four hold registers described in Tables 4 through 7. Loading new data into a hold register not associated with the synthesizer frequency programming does not reset or change the synthesizer. The synthesizer should not lose lock before, during, or after a new serial word load that does not change the programmed frequency.

Vendor ID Read-Back

The SKY73126-31 includes a read-back function that provides the vendor ID. This information is stored in register word 0 and is provided by the lock detect output signal (LD, pin 12).

Vendor ID read-back is initiated by setting the MSB of a 32-bit data word and writing the word to device word address 0 (all other bits of the data word are "don't care"). After the LE signal transitions from low to high, the rising edge of CLK gates the Word 0 register data (vendor ID) to the lock detect pin, MSB first.

The vendor ID for the SKY73126-31 is 0x100 (equal to 100000000b or 256 decimal).

Figure 5 shows the Serial Peripheral Interface (SPI) timing diagram for vendor ID read-back. Figure 6 defines the word used to initiate the vendor ID read-back function.
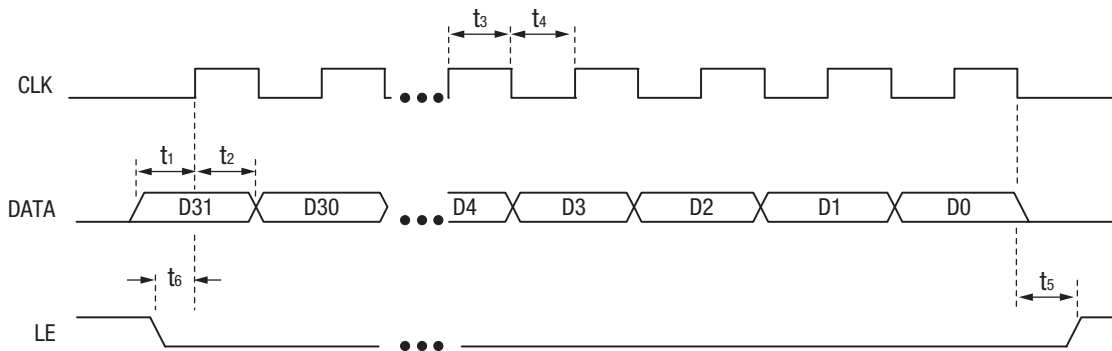
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Figure 3. SKY73126-31 Serial Data Input Timing Diagram (MSB First)

Table 2. CLK, DATA, LE Timing Parameters

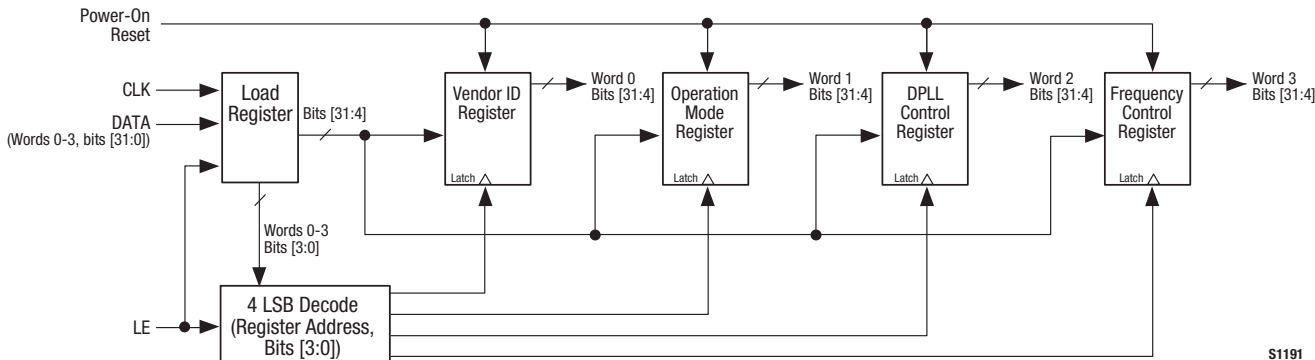| Parameter	Value
DATA to CLK setup time (t1)	>10 ns
DATA to CLK hold time (t2)	>10 ns
CLK high duration (t3)	>25 ns
CLK low duration (t4)	>25 ns
CLK to LE hold time (t5)	>10 ns
LE to CLK setup time (t6)	>10 ns
Read-back clock to output time (tdOUT)	<25 ns

Figure 4. Serial Bus Block Diagram

Table 3. SKY73126-31 Hold Registers and Addresses

Hold Register Name	Hold Register Address (Binary) in Load Register Words			
	Bit [3]	Bit [2]	Bit [1]	Bit [0]
Vendor ID	0	0	0	0
Operation Mode	0	0	0	1
DPLL Control	0	0	1	0
Frequency Control	0	0	1	1

Table 4. Word 0: Vendor ID Hold Register

Parameter	Function	State Description	Recommended Operational Value (Binary)	Default Value (Binary)
wd_3, wd_2, wd_1, wd_0	Address bits [3:0]. Must be set to 0000b (see Table 3).		0000	0000
vendor id	Vendor ID read-back [31:4]	Bits [31:4]: Bit [31] Bits [30:4] 0 x = vendor ID 1 x = vendor ID initial read-back	Application dependent	10000

Table 5. Word 1: Operation Mode Hold Register (1 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)	Default Value (Binary)
wd_3, wd_2, wd_1, wd_0	Address bits [3:0]. Must be set to 0001b (see Table 3).		0001	0001
cp_output	Charge pump setting [6:4]	Bits [6:4]: 0 0 0 = 800 μA 0 0 1 = 1600 μA 0 1 0 = 2400 μA 0 1 1 = 3200 μA 1 0 0 = 4000 μA 1 0 1 = 4800 μA 1 1 0 = 5600 μA 1 1 1 = 6400 μA	Application dependent	000
rsvd	Reserved [8:7]	Reserved	00	00

Table 5. Word 1: Operation Mode Hold Register (2 of 2)

| Parameter	Function	State Description	Recommended Operational Value (Binary)	Default Value (Binary)
pd_polar	Polarity of the phase detector [9]	Bit [9]: 0 = negative 1 = positive	0	0
cp_tristate	Tri-states the transmit PLL charge pump [10]	Bit [10]: 0 = charge pump functional 1 = charge pump disabled/tri-stated	0	0
nr_sel	Internal operating voltage control bit for the N-counter and R-divider [11] Note: this bit needs to be programmed together with Word 1, bit [12], and Word 2, bit [25].	Word 1 Word 1 Word 2 Bit [12] Bit [11] Bit [25]: N-Cntr/R-Divider Voltage Mod Dig Voltage 0 X X = 0 V 0 V 1 0 0 = 1.8 V 1.8 V 1 0 1 = 1.8 V 2.4 V 1 1 0 = 2.4 V 1.8 V 1 1 1 = 2.4 V 2.4 V	0	0
pll_en	Internal operating voltage control bit for the PLL [12] Note: this bit needs to be programmed together with Word 1, bit [11], and Word 2, bit [25].	See nr_sel parameter (bit [11])	1	0
ref_bw_sel	Reference buffer bandwidth [14:13]	Bits [14:13]: 0 0 = 20 MHz 0 1 = 30 MHz 1 0 = 40 MHz 1 1 = 50 MHz	Application dependent	00
pre_curr_sel	Prescaler current bias [16:15]	Bits [16:15]: 0 0 = 20 μA 0 1 = 22 μA 1 0 = 24 μA 1 1 = 26 μA	00	00
prescale_sel	Prescaler mode select [17]	Bit [17]: 0 = Prescaler in 8/9 divide mode 1 = Prescaler in 16/17 divide mode	Application dependent	0
rdiv	Reference divider ratio [27:18]	Bits [27:18]: represents the 10-bit reference divider, R1 [9:0]. Refer to the Synthesizer Programming section of this Data Sheet for information.	Application dependent	0000000000
rsvd	Reserved [31:28]	Reserved	0000	0000

Table 6. Word 2: DPLL Control Hold Register

Parameter	Function	State Description	Recommended Operational Value (Binary)	Default Value (Binary)
wd_3, wd_2, wd_1, wd_0	Address bits [3:0]. Must be set to 0010b (see Table 3).		0010	0010
dpll_ctrl	DPLL control [21:4]	Reserved	–	00000000000 0000000
test_mux	Lock detect and diagnostic output select [24:22] Note: Logic output is via LD signal (pin 12)	Bits [24:22]: 0 0 0 = lock detect output or vendor ID read-back 0 0 1 = R-divider output 0 1 0 = N-divider output 0 1 1 = capacitor overflow 1 0 0 = capacitor underflow 1 0 1 = VCO high comparator 1 1 0 = VCO low comparator 1 1 1 = DPLL test Note: When test_mux = 000, the vendor ID is output to pin 12 if vendor ID read-back has been initialized. Otherwise, when test_mux = 000, pin 12 outputs the lock detect signal.	000	000
sd_sel	Internal operating voltage control bit for the synthesizer [25] Note: this bit needs to be programmed together with Word 1, bit [11], and Word 1, bit [12].	See nr_sel parameter (Word 1, bit [11])	0	0
rsvd	Reserved [31:26]	Reserved	000000	000000

Table 7. Word 3: Frequency Control Hold Register (1 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)	Default Value (Binary)
wd_3, wd_2, wd_1, wd_0	Address bits [3:0]. Must be set to 0011b (see Table 3).		0011	0011
dpll_en	VCO auto tuning enable flag [4]	Bit [4]: 0 = disable VCO auto tuning 1 = enable VCO auto tuning	Refer to Figure 7	0

ndiv	N-divider/prescaler mode for control of M and A counters [20:5]	Bits [20:5]:
		
		For 8/9 prescaler mode:
		  bits [7:5] = A-counter bits [2:0] (bit [3] = 0)
		  bits [19:8] = M-counter bits [11:0]
		  bit [20] = 0
		
		For 16/17 prescaler mode:
		  bits [8:5] = A-counter bits [3:0]
		  bits [20:9] = M-counter bits [11:0]
			Application dependent	00000000000 00000

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Table 7. Word 3: Frequency Control Hold Register (2 of 2)

Parameter	Function	State Description	Recommended Operational Value (Binary)	Default Value (Binary)
cp_delay	Charge pump delay [23:21]	Bits [23:21]: 0 0 0 = 0.5 ns 0 0 1 = 0.7 ns 0 1 0 = 0.9 ns 0 1 1 = 1.2 ns 1 0 0 = 1.4 ns 1 0 1 = 1.7 ns 1 1 0 = 2.0 ns 1 1 1 = 3.0 ns	000	000
rsvd	Reserved [31:24]	Reserved	00000000	00000000
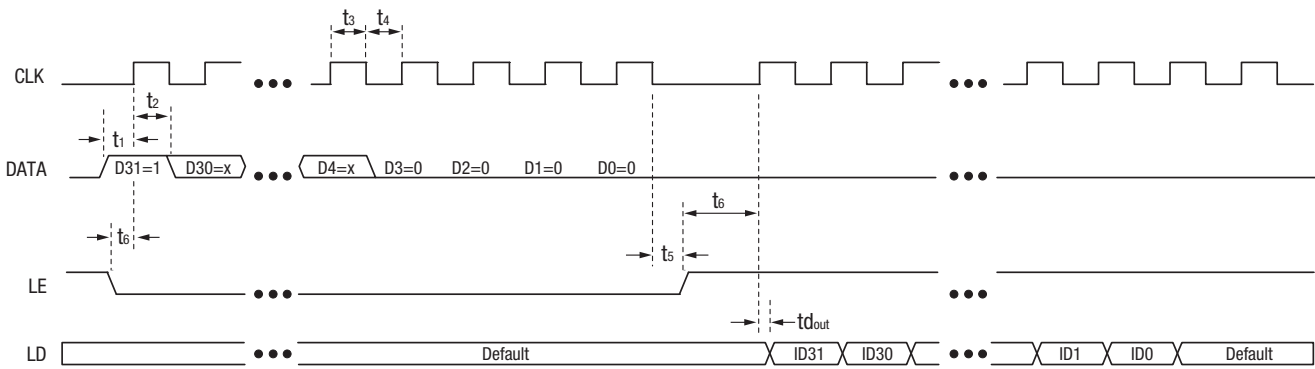
Figure 5. Vendor ID Read-Back Timing Diagram

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Figure 6. Vendor ID Read-Back Initialization Word

VCO Prescalers

The VCO prescalers divide the VCO output signal by either 16/17 or 8/9. The modulus control signal from the N-counter determines whether to divide by 16 or 17 in 16/17 mode, or whether to divide by 8 or 9 in 8/9 mode. The prescaler mode is determined by bit [17] of Word 1 (Operation Mode Register). The maximum prescaler input frequency is 2000 MHz for 8/9 mode, and 3100 MHz for 16/17 mode.

N-Counter

The N-counter consists of two asynchronous ripple counters, a 12-bit M-counter and a 4-bit A-counter. The M-counter determines the counts using the lower division ratio in the prescaler (8 or 16); the A-counter determines the counts using the upper division ratio (9 or 17).

The value of the N-counter is determined by the equation:

$$(M \times P) + A$$

where M and A are the values of the M-counter and A-counter, and P = 8 for 8/9 mode or 16 for 16/17 mode.

In 16/17 mode, the M-counter (bits [11:0]) value is determined by the 12 highest order bits of the N-counter (bits [15:4]). The A-counter value (bits [3:0]) is determined by the 4 lowest order bits of the N-counter (bits [3:0]).

In 8/9 mode, the M-counter value is determined by bits [14:3] of the N-counter and the A-counter value is determined by the three lowest order bits of the N-counter (bits [2:0]). In this case, bit [15] of the N-counter is always cleared.

Phase Detector and Charge Pump

The phase detector and charge pump detect and integrate the phase and frequency errors of the divided-down VCO output versus the reference clock. This results in a feedback adjustment of the control voltage for the VCO.

Lock Detect

Lock detection circuitry provides a CMOS logic level indication when the PLL is frequency locked (high when locked).

Reference Input Divider

The R-counter (reference input clock divider) consists of 10-bit dividers controlled by the rdiv parameter in Word 1 (Operation Mode Register, bits [27:18]). The R-counter divides the clock signal from the reference input buffer by 1, 2, 4, or 1023 (approx.) and sends the rdiv output to the Phase Frequency Detector (PFD).

Synthesizer Programming

The SKY73126-31 has selectable VCO prescalers to divide the VCO output signal by either 16/17 or 8/9. The prescaler mode is determined by the prescale_sel parameter (Word 1, bit [17], of the Operation Mode Register).

To program the synthesizer to the correct frequency, the N-divider and R-divider ratios need to be determined. The N-divider ratio is the result of dividing the VCO output frequency by the phase comparison frequency:

$$Ndiv = \frac{f_{VCO}}{f_{PFD}}$$

The VCO output frequency is four times greater than the synthesizer RF output frequency. The value of Ndiv is rounded to the nearest integer and then converted into a binary number which is written to the serial bus. The maximum Ndiv for the 8/9 prescaler mode is 2^{15} or 32768. For the 16/17 prescaler mode, the maximum Ndiv is 2^{16} or 65536.

The R-divider ratio is the result of dividing the reference input frequency by the phase comparison frequency:

$$Rdiv = \frac{f_{ref}}{f_{PFD}}$$

Example:

A synthesizer frequency of 161.92 MHz is required using a crystal frequency of 10 MHz. The minimum frequency step is 80 kHz. Determine the R-divider ratio:

$$Rdiv[9:0] = 10\ MHz/80\ kHz = 125 = 1111101b$$

Divide the VCO output frequency, which is four times the RF output frequency, by the phase comparison frequency (minimum frequency step in this example) to obtain the N-divider ratio:

$$Ndiv[15:0] = (161.92\ MHz \times 4)/80\ kHz = 8096$$

Round the value of Ndiv to the nearest integer and then convert to binary:

$$Ndiv[15:0] = 19384 = 0001111110100000b$$

Since the VCO output frequency (f_{VCO}) is lower than 2000 MHz and Ndiv is less than 2^{15}, the 8/9 prescaler mode could be used.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY73126-31 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks Application Note, *Tape and Reel*, document number 101568.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration

1. Paths to ground should be made as short and as low impedance as possible.

2. The ground pad of the SKY73126-31 provides critical electrical grounding requirements. Design the connection to the ground pad to provide the best electrical connection to the circuit board. Multiple vias to the grounding layer are recommended to connect the top layer ground area to the main ground layer.

3. Skyworks recommends including external bypass capacitors on the VCC voltage input (pin 1) of the device. These capacitors should be placed as close as possible to the VCC input pin.

4. A 50 Ω impedance trace is needed for the RF_OUT (pin 3) line.

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Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY73126-31 are provided in Table 8. The recommended operating conditions are specified in Table 9 and electrical specifications are provided in Table 10. Measurement plots for single sideband phase noise and frequency settling time are shown in Figures 7 and 8, respectively.

A typical application schematic for the SKY73126-31 is provided in Figure 9. Figure 10 shows the package dimensions for the 16-pin MCM and Figure 11 provides the tape and reel dimensions.

Table 8. SKY73126-31 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	VCC	0		5.5	V
Operating temperature, full performance	T_{OP}	−40		+85	°C
Storage temperature	T_{ST}	−40		+150	°C

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. The SKY73126-31 ESD threshold level is 2500 VDC using Human Body Model (HBM) testing. This level applies to RF signal lines >100 MHz, analog and RF lines <100 MHz, digital lines, power supply lines, and ground pins.

Table 9. SKY73126-31 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units
Supply voltage	VCC	4.75	5.00	5.25	V

Input voltage (CLK, DATA, LE):
    Low level
    High level
		
		1.4
				
				0.6
				
					V
					V

Output voltage (LD) with 18 kΩ load from VCC PLL:
    Low level, unlocked
    High level, unlocked
		
		2.4
				
				0.4
				
					V
					V

Load connected to RF output	50 Ω, maximum VSWR (load input) 2.0:1, all phases				

Table 10. SKY73126-31 Electrical Characteristics (Note 1) (Note 2)
(VCC = 5 V, T$_C$ = 25 °C, cp_output = 3200 μA, TCXO_IN = 10 MHz, f = 161.92 MHz, f$_{PFD}$ = 80 kHz, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Units
Oscillation frequency	f$_{OSC}$			161.92		MHz
Oscillation frequency range		PLL must be programmed for desired frequency (Note 3)	160		165	MHz
Reference frequency	f$_{REF}$			10 or 32		MHz
Reference input voltage (Note 4)			2.0	2.5	2.7	Vpp
Output level				10		dBm
Output impedance				50		Ω
Output VSWR					2.0:1	–
Reference frequency (f$_{REF}$) input impedance (Note 4)			5			kΩ
Harmonic suppression	H2, H3			−40.9		dBc
PLL reference spurious suppression around f$_{OSC}$: 　@ 80 kHz 　@ 160 kHz 　sum @ 240 kHz to 1 MHz 　sum @ 1 MHz to 2.4 MHz 　sum >2.4 MHz		f$_{REF}$ = 10 MHz		 −97 −103 −96 −100 −100	 −80 −85 −85 −85 −90	 dBc dBc dBc dBc dBc
Reference spurious suppression around f$_{OSC}$		f$_{REF}$ = 10 MHz		−110	−85	dBc
		f$_{REF}$ = 32 MHz		−98	−85	dBc
Other spurious suppression (not multiple of PLL reference) around f$_{OSC}$: 　sum @ 0.5 kHz to 50 kHz 　sum @ 50 kHz to 100 kHz 　sum @ 100 kHz to 10 MHz		f$_{REF}$ = 10 MHz		 −100.0 −100.0 −91.0	 −50.0 −64.0 −90.0	 dBc dBc dBc
Single sideband phase noise offset: 　@ 1 kHz 　@ 5 kHz 　@ 10 kHz 　@ 100 kHz 　@ 500 kHz 　@ 1 MHz 　@>2.7 MHz				 −87.7 −99.3 −109.2 −141.9 −151.6 −153.1 −153.8	 −80.0 −90.0 −100.0 −120.0 −132.0 −151.0 −152.0	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Settling time (Note 4)					5	ms
Pulling (Note 4)		2.0:1 VSWR			< ±100	kHz
Pushing (Note 4): 　200 Hz to 1 MHz 　1 MHz to 460 MHz					 −40 −90	 dBc dBc
Current consumption				72	119	mA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Characterized performance may change if the SKY73126-31 is configured differently than the test conditions specified here.

Note 3: Frequency range not tested in production.

Note 4: Guaranteed by design based on lab data. No production test.

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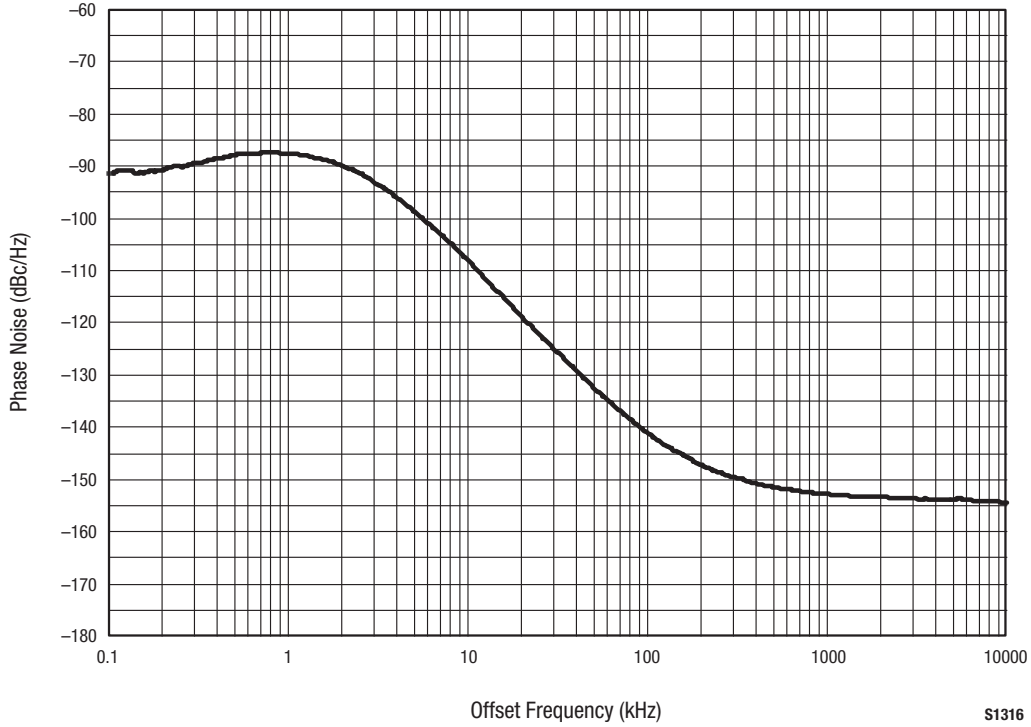
Figure 7. SKY73126-31 Single Sideband Phase Noise Measurements @ 161.92 MHz
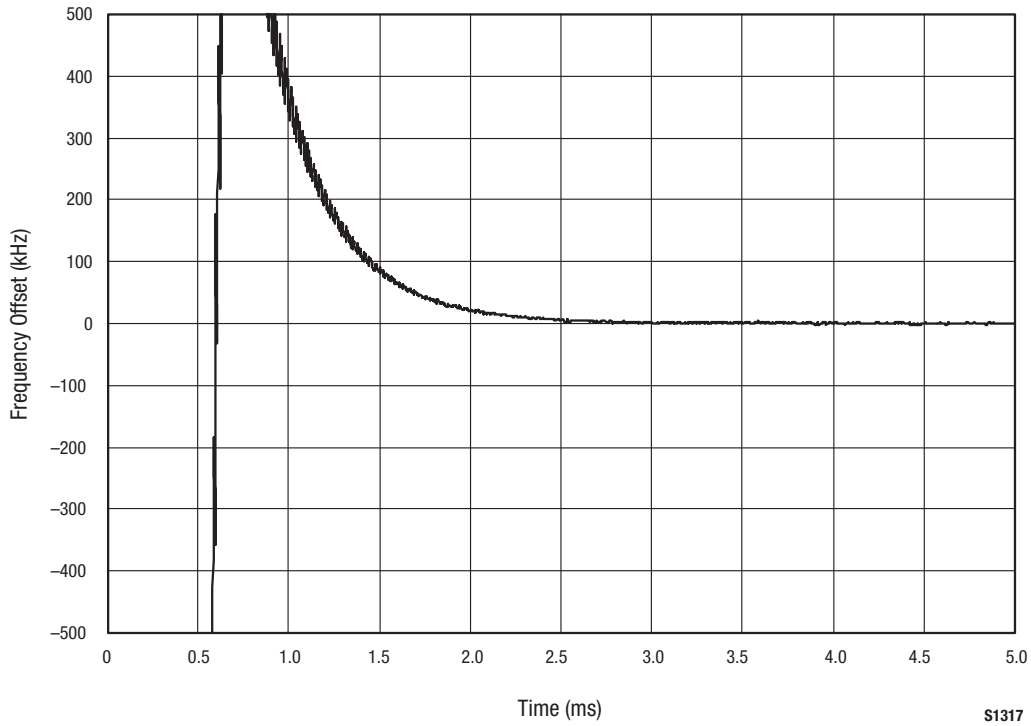
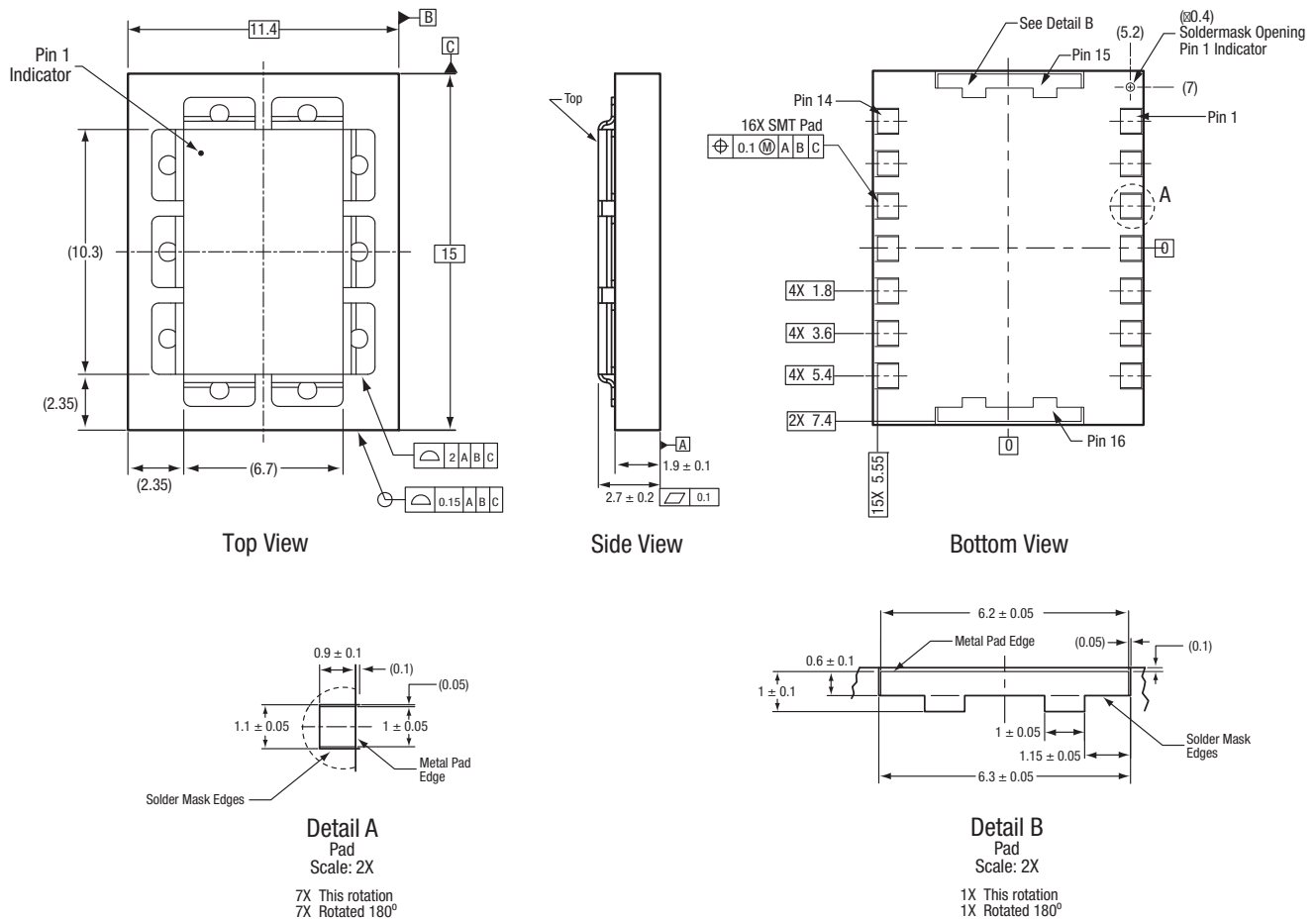**Figure 8. SKY73126-31 Frequency Settling Time @ 161.92 MHz**
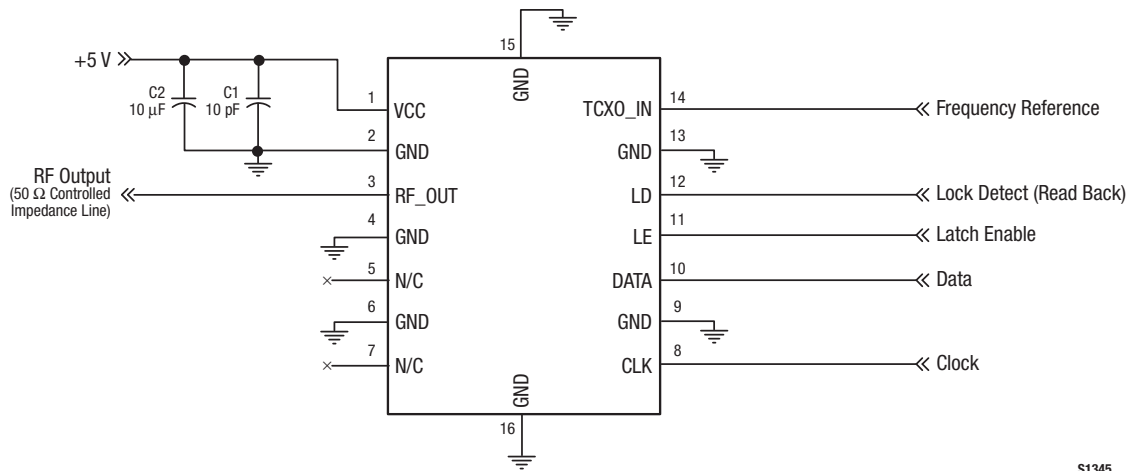
Figure 9. SKY73126-31 Typical Application Schematic

Top View

Side View

Bottom View

Detail A
Pad
Scale: 2X

7X This rotation
7X Rotated 180°

Detail B
Pad
Scale: 2X

1X This rotation
1X Rotated 180°

All measurements are in millimeters

Dimensioning and tolerancing according to ASME Y14.5M-1994

S1319

Figure 10. SKY73126-31 16-Pin MCM Package Dimensions

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Figure 11. SKY73126-31 Tape and Reel Dimensions
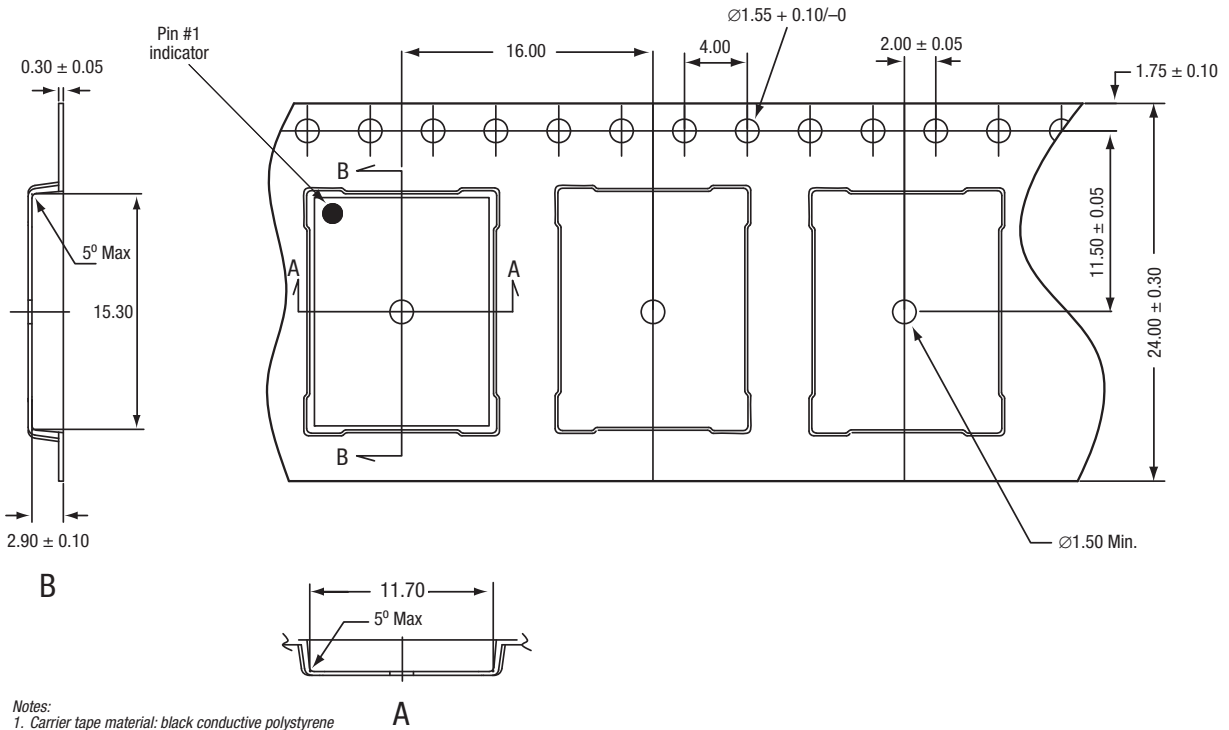
Notes:
1. Carrier tape material: black conductive polystyrene
2. Cover tape material: transparent conductive PSA
3. Cover tape size: 21.3 mm width
4. All measurements are in millimeters

S1318

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
SKY73126-31 161.92 MHz VCO/Synthesizer	SKY73126-31	TW17-D730

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