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PRODUCT OVERVIEW

OVERVIEW

The KS57C5532/P5532 single-chip CMOS microcontroller has been designed for high-performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers). The KS57P5532 is a microcontroller which has 32-kbyte one-time-programmable EPROM but its functions are same to KS57C5532.

With its DTMF generator, 8-bit serial I/O interface, and versatile 8-bit timer/counters, the KS57C5532/P5532 offers an excellent design solution for a wide variety of telecommunication applications.

Up to 55 pins of the 64-pin SDIP or QFP package can be dedicated to I/O. Seven vectored interrupts provide fast response to internal and external events. In addition, the KS57C5532/P5532's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

DEVELOPMENT SUPPORT

The Samsung Microcontroller Development System, SMDS, provides you with a complete PC-based development environment for KS57-series microcontrollers that is powerful, reliable, and portable. In addition to its window-based program development structure, the SMDS toolset includes versatile debugging, trace, instruction timing, and performance measurement applications.

The Samsung Generalized Assembler (SAMA) has been designed specifically for the SMDS environment and accepts assembly language sources in a variety of microprocessor formats. SAMA generates industry-standard hex files that also contain program control data for SMDS compatibility.

FEATURES SUMMARY

Memory

- 1 K × 4-bit RAM
- 32 K × 8-bit ROM

55 I/O Pins

- Input only: 4 pins
- I/O: 43 pins
- N-channel open-drain I/O (S/W): 8 pins

Memory-Mapped I/O Structure

- Data memory bank 15

DTMF Generator

- 16 dual-tone frequencies for tone dialing

8-bit Basic Timer

- Programmable internal timer
- Watchdog timer

Two 8-bit Timer/Counters

- Programmable interval timer
- External event counter function
- Timer/counters clock outputs to TCLO0 and TCLO1 pins
- External clock signal divider
- Serial I/O interface clock generator

Watch Timer

- Time interval generation:
0.5 s, 3.9 ms at 32.768 kHz
- 4 frequency outputs to the BUZ pin

8-bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive mode
- LSB-first or MSB-first transmission selectable

Bit Sequential Carrier

- Supports 8-bit serial data transfer in arbitrary format

Interrupts

- 3 external interrupt vectors
- 4 internal interrupt vectors
- 2 quasi-interrupts

Power-Down Modes

- Idle: Only CPU clock stops
- Stop: Main system clock stops
- Subsystem clock stop mode

Oscillation Sources

- Crystal, ceramic for main system clock
- Crystal oscillator for subsystem clock
- Main system clock frequency:
3.579545 MHz (typical)
- Subsystem clock frequency: 32.768 kHz (typical)
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.67, 1.33, 10.7 μ s at 6.0 MHz
- 1.12, 2.23, 17.88 μ s at 3.579545 MHz
- 122 μ s at 32.768 kHz

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V (at 3 MHz)
- 2.7 V to 5.5 V (at 6 MHz)

Package Types

- 64 SDIP, 64 QFP

BLOCK DIAGRAM

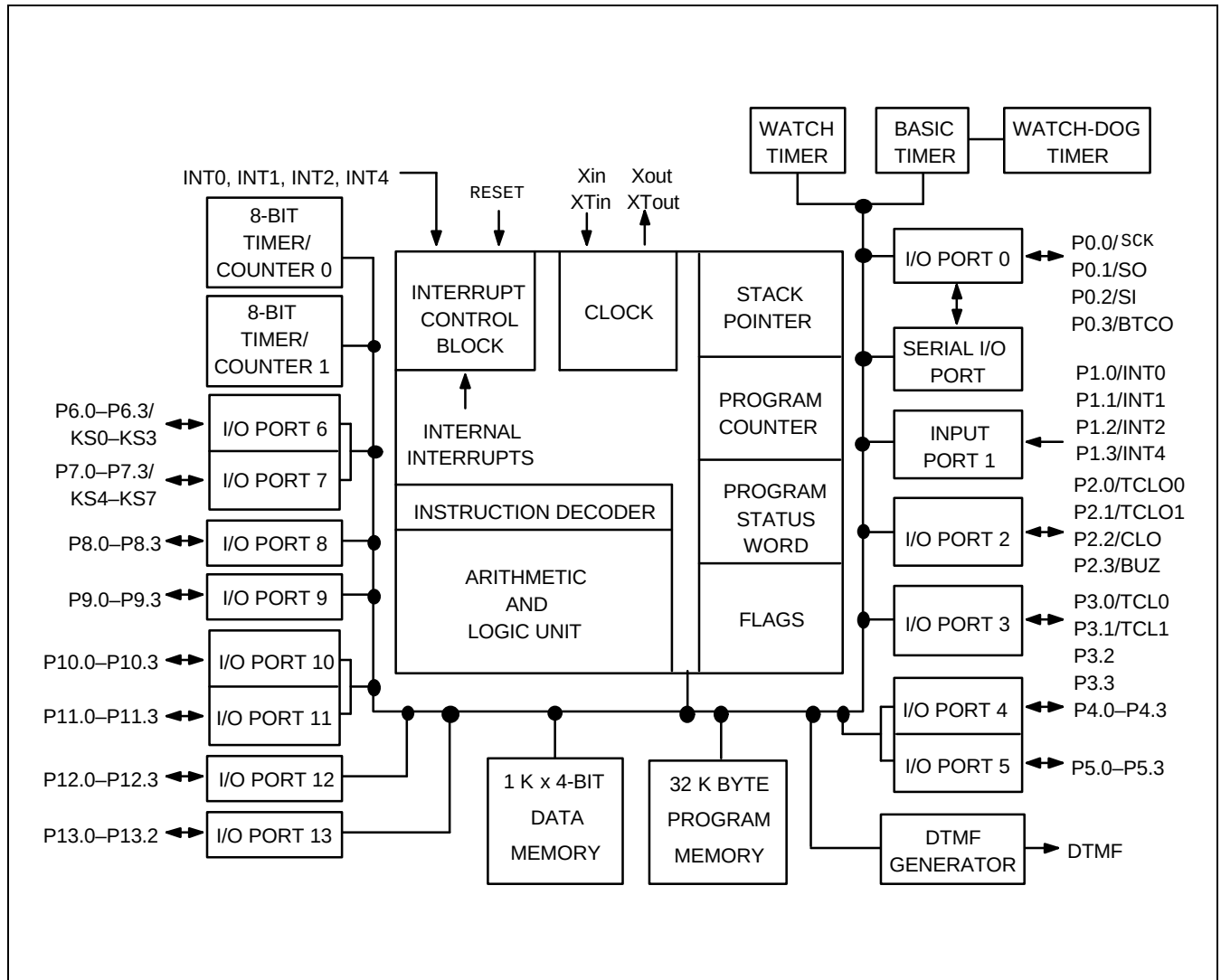


Figure 1-1. KS57C5532/P5532 Simplified Block Diagram

PIN ASSIGNMENTS

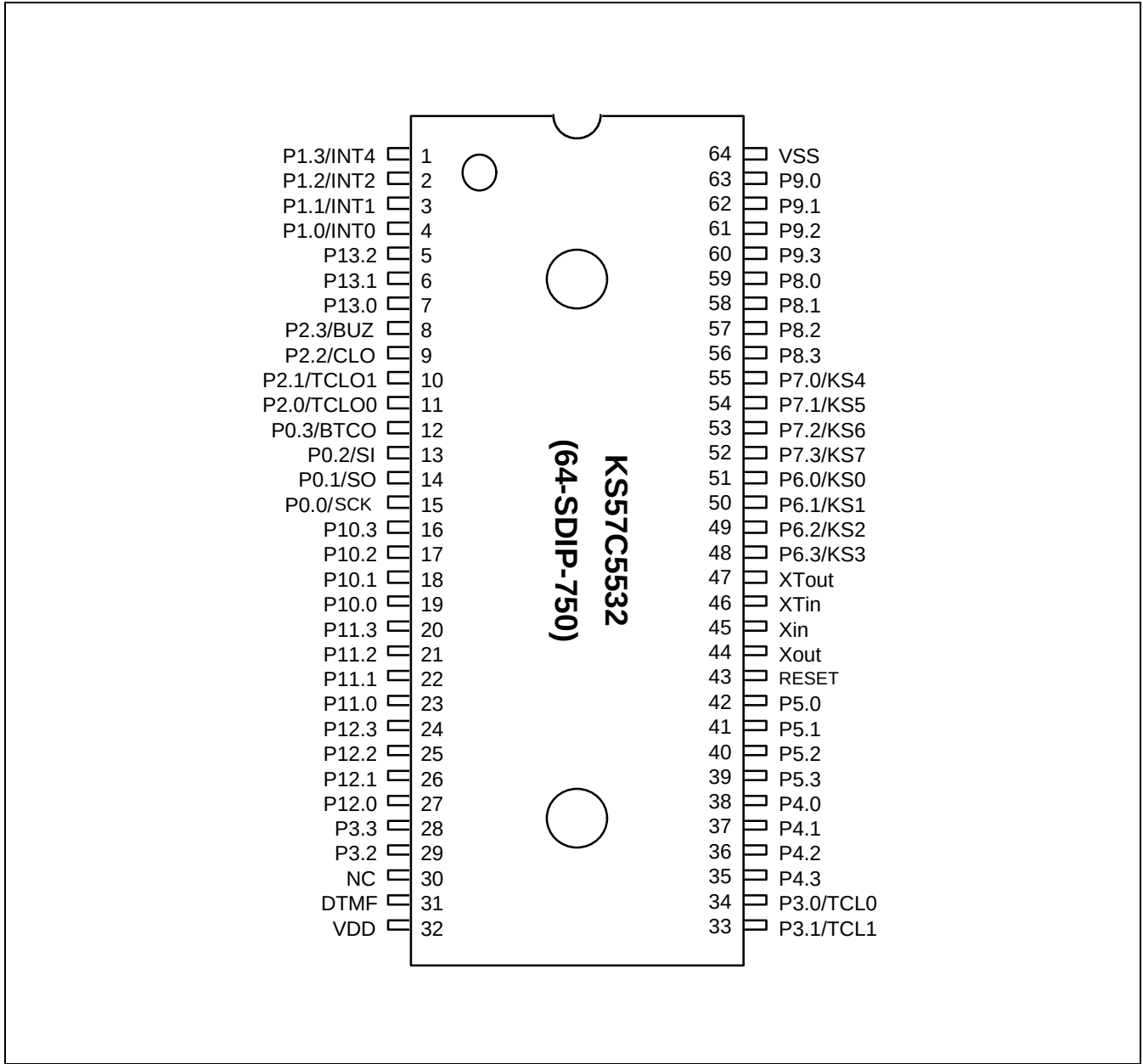


Figure 1-2. KS57C5532/P5532 Pin Assignment Diagrams

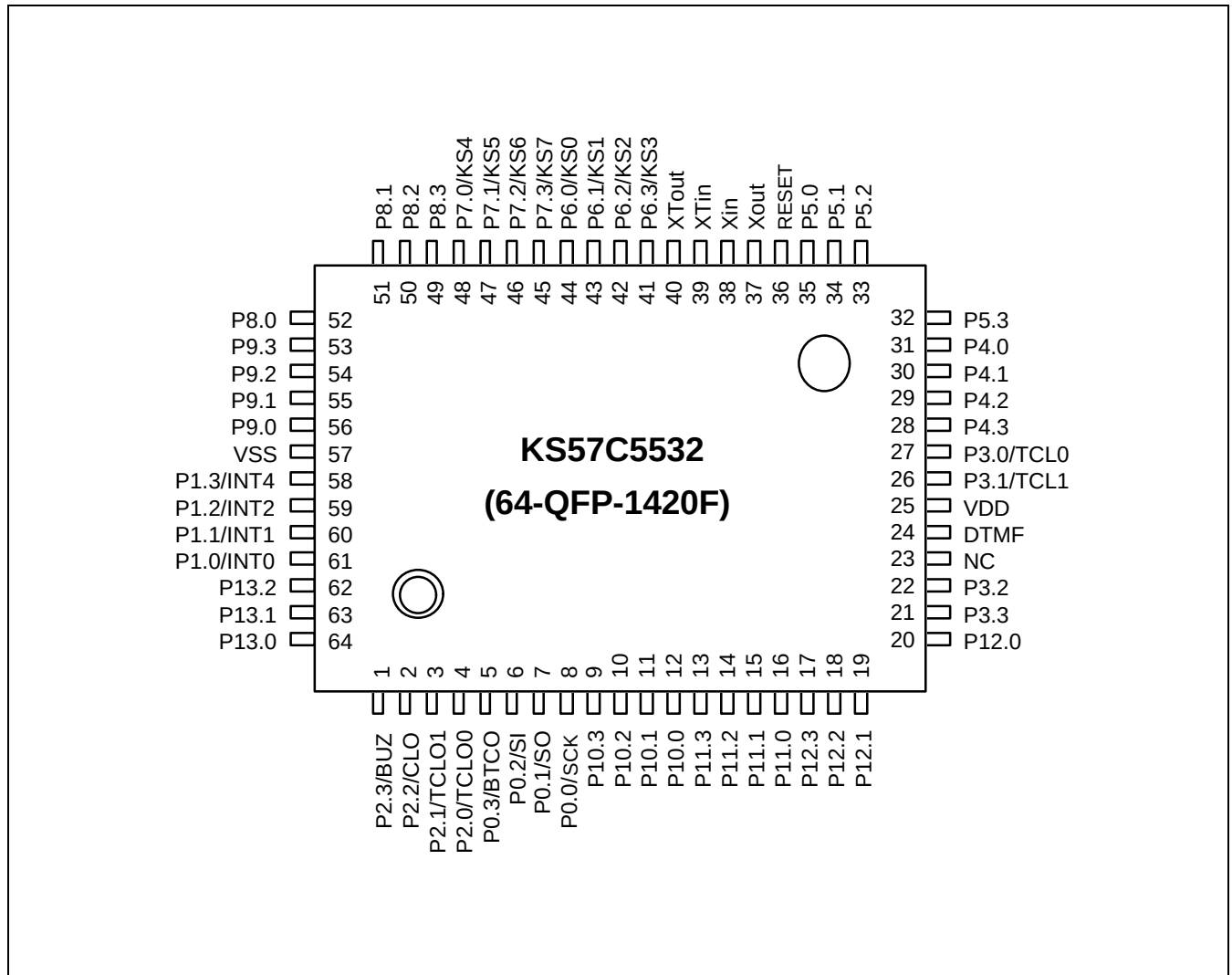


Figure 1-2. KS57C5532/P5532 Pin Assignment Diagrams (Continued)

PIN DESCRIPTIONS

Table 1-1. KS57C5532/P5532 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	15 (8) 14 (7) 13 (6) 12 (5)	SCK SO SI BTCO
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test is possible. 4-bit pull-up resistors are assignable by software to port 1.	1 (61) 2 (60) 3 (59) 4 (58)	INT0 INT1 INT2 INT4
P2.0 P2.1 P2.2 P2.3	I/O	Same as port 0.	11 (4) 10 (3) 9 (2) 8 (1)	TCLO0 TCLO1 CLO BUZ
P3.0 P3.1 P3.2 P3.3	I/O	Same as port 0.	34 (27) 33 (26) 29 (22) 28 (21)	TCL0 TCL1 SCLK ⁽¹⁾ SDAT ⁽¹⁾
P4.0–P4.3 P5.0–P5.3	I/O	4-bit I/O ports. 1-bit and 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable to input pins and are automatically disabled for output pins. N-channel open-drain or push-pull output can be selected by software. Port 4 and 5 can be paired to support 8-bit data transfer.	38–35 (31–28) 42–39 (35–32)	–
P6.0–P6.3 P7.0–P7.3	I/O	4-bit I/O ports. 1-bit or 4-bit read/write and test is possible. Port 6 pins are individually software configurable as input or output. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins. Ports 6 and 7 can be paired to enable 8-bit data transfer.	51–48 (44–41) 55–52 (48–45)	KS0–KS3 KS4–KS7
P8.0–P8.3	I/O	Same as port 0.	59–56 (52–49)	–
P9.0–P9.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. 4-bit pull-up resistors are software assignable; pull-up resistors are automatically disabled for output pins.	63–60 (56–53)	–

NOTES

1. SCLK and SDAT are used for KS57P5532 only.
2. Parentheses indicate pin number for 64 QFP package.

Table 1-1. KS57C5532/P5532 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin
P10.0–P10.3 P11.0–P11.3	I/O	Same as port 9. Ports 10 and 11 can be paired to support 8-bit data transfer.	19–16 (12–9) 23–20 (16–13)	–
P12.0–P12.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. Individual pins are software configurable as input or output. 4-bit <i>pull-down</i> resistors are software assignable; pull-down resistors are automatically disabled for output pins.	27–24 (20–17)	–
P13.0–P13.2	I/O	3-bit I/O port; characteristics are same as port 9.	7–5 (64–62)	–
DTMF	O	DTMF output.	31 (24)	–
SCK	I/O	Serial I/O interface clock signal	15 (8)	P0.0
SO	I/O	Serial data output	14 (7)	P0.1
SI	I/O	Serial data input	13 (6)	P0.2
BTCO	I/O	Basic timer clock output	12 (5)	P0.3
INT0, INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. INT0 is synchronized to system clock.	4, 3 (61, 60)	P1.0, P1.1
INT2	I	Quasi-interrupt with detection of rising edges	2 (59)	P1.2
INT4	I	External interrupt with detection of rising and falling edges.	1 (58)	P1.3
TCLO0	I/O	Timer/counter 0 clock output	11 (4)	P2.0
TCLO1	I/O	Timer/counter 1 clock output	10 (3)	P2.1
CLO	I/O	Clock output	9 (2)	P2.2
BUZ	I/O	2 kHz, 4 kHz, 8 kHz, or 16 kHz frequency output at the watch timer clock frequency of 32.768 kHz for buzzer sound	8 (1)	P2.3
TCL0	I/O	External clock input for timer/counter 0	34 (27)	P3.0
TCL1	I/O	External clock input for timer/counter 1	33 (26)	P3.1
KS0–KS3 KS4–KS7	I/O	Quasi-interrupt inputs with falling edge detection	51–48 (44–41) 55–52 (48–45)	P6.0–P6.3 P7.0–P7.3

NOTE: Parentheses indicate pin number for 64 QFP package.

Table 1-1. KS57C5532/P5532 Pin Descriptions (Concluded)

Pin Name	Pin Type	Description	Number	Share Pin
V _{DD}	–	Power supply	32 (25)	–
V _{SS}	–	Ground	64 (57)	–
RESET	I	Reset signal	43 (36)	–
X _{IN} , X _{OUT}	–	Crystal, ceramic, or R/C oscillator signal for main system clock. (For external clock input, use X _{IN} and input X _{IN} 's reverse phase to X _{OUT})	45, 44 (38, 37)	–
XT _{IN} , XT _{OUT}	–	Crystal oscillator signal for subsystem clock. (For external clock input, use XT _{IN} and input XT _{IN} 's reverse phase to XT _{OUT})	46, 47 (39, 40)	–
NC	–	No connection (must be connected to V _{SS})	30 (23)	–

NOTE: Parentheses indicate pin number for 64 QFP package.

Table 1-2. Overview of KS57C5532/P5532 Pin Data

Pin Names	Share Pins	I/O Type	Reset Value	Circuit Type
P0.0–P0.3	SCK, SO, SI, BTCO	I/O	Input	D-4
P1.0–P1.3	INT0, INT1, INT2, INT4	I	Input	A-1
P2.0–P2.3	TCLO0, TCLO1, CLO, BUZ	I/O	Input	D-2
P3.0–P3.1	TCL0, TCL1	I/O	Input	D-4
P3.2–P3.3	–	I/O	Input	D-2
P4.0–P4.3 P5.0–P5.3	–	I/O	Input	E-2
P6.0–P6.3 P7.0–P7.3	KS0–KS3 KS4–KS7	I/O	Input	D-4
P8.0–P8.3	–	I/O	Input	D-2
P9.0–P9.3	–	I/O	Input	D-2
P10.0–P10.3 P11.0–P11.3	–	I/O	Input	D-2
P12.0–P12.3	–	I/O	Input	D-6
P13.0–P13.2	–	I/O	Input	D-2
DTMF	–	O	High impedance	G-6
X _{in} , X _{out} X _{Tin} , X _{Tout}	–	–	–	–
RESET	–	I	–	B
NC	–	–	–	–
V _{DD} , V _{SS}	–	–	–	–