HM51W4400B Series
HM51W4400BL Series (Low Power Version)

1,048,576-word × 4-bit Dynamic Random Access Memory.

The Hitachi HM51W4400B/BL is a CMOS dynamic RAM organized 1,048,576 words x 4 bits. HM51W4400B/BL has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM51W4400B/BL offers Fast Page Mode as a high speed access mode. Multiplexed address input permits the HM51W4400B/BL to be packaged in standard 300-mil 20-pin plastic SOJ and 20-pin plastic TSOP II.

Features

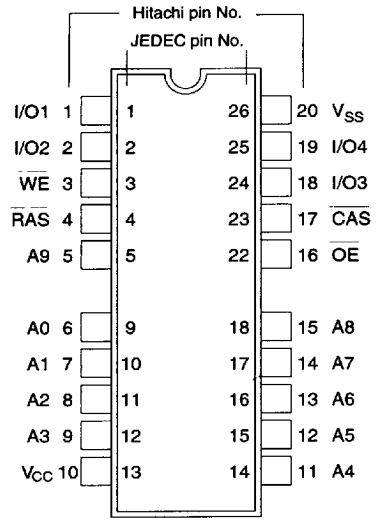
- Single 3.3 V (± 0.3 V)
- High speed
  - — Access time
    60 ns/70 ns/80 ns (max)
- Low power dissipation
  - — Active mode
    288 mW/252 mW/216 mW (max)
  - — Standby mode 3.6 mW (max)
    0.18 mW (max) (L-version)
- Fast page mode capability
- 1024 refresh cycles : 16 ms
  1024 refresh cycles : 128 ms (L-version)
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- Test function
- Battery back up operation
- Self refresh operation (L-version)

Ordering Information

Type No.	Access time	Package
HM51W4400BS-6	60 ns	300-mli 20-pin
HM51W4400BS-7	70 ns	plastic SOJ
HM51W4400BS-8	80 ns	(CP-20D)
HM51W4400BTT-6	60 ns	20-pin
HM51W4400BTT-7	70 ns	plastic TSOPII
HM51W4400BTT-8	80 ns	(TTP-20D)
HM51W4400BRR-6	60 ns	20-pin plastic
HM51W4400BRR-7	70 ns	TSOP II reverse
HM51W4400BRR-8	80 ns	(TTP-20DR)
HM51W4400BLS-6	60 ns	300-mli 20-pin
HM51W4400BLS-7	70 ns	plastic SOJ
HM51W4400BLS-8	80 ns	(CP-20D)
HM51W4400BLTT-6	60 ns	20-pin
HM51W4400BLTT-7	70 ns	plastic TSOPII
HM51W4400BLTT-8	80 ns	(TTP-20D)
HM51W4400BLRR-6	60 ns	20-pin plastic
HM51W4400BLRR-7	70 ns	TSOP II reverse
HM51W4400BLRR-8	80 ns	(TTP-20DR)

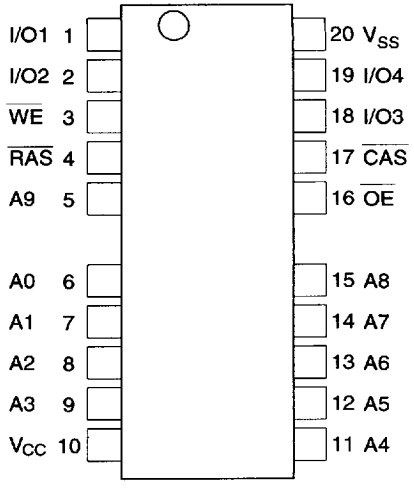
Pin Arrangement

HM51W4400BS/BLS Series



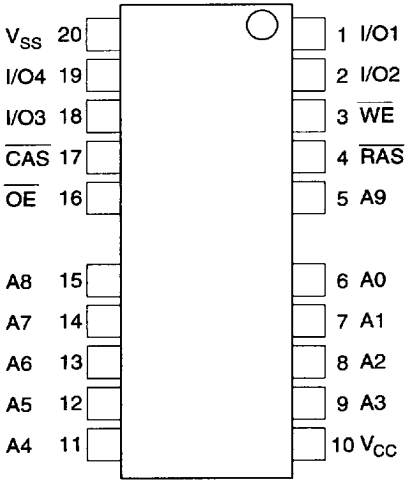
(Top view)

HM51W4400BTT/BLTT Series



(Top view)

HM51W4400BRR/BLRR Series

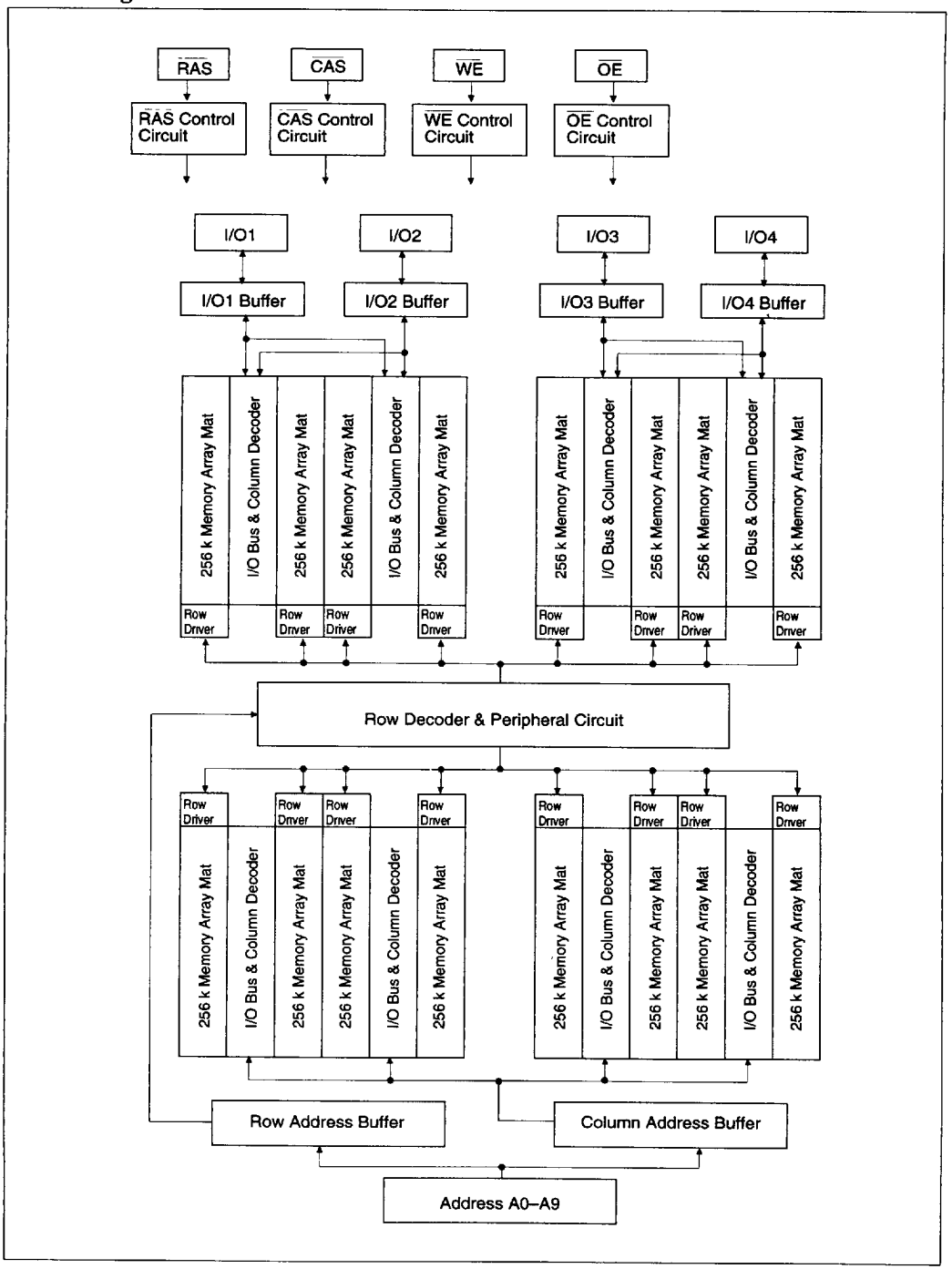


(Top view)

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
I/O1 – I/O4	Data-in/Data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+ 3.3 V typ)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note : 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Test condition	Notes
Operating current	I_{CC1}	—	80	—	70	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)		—	50	—	50	—	50	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, $\overline{OE}$, Address and Din = V_{IH} or V_{IL} Dout = High-Z	4
$\overline{RAS}$-only refresh current	I_{CC3}	—	80	—	70	—	60	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	4	—	4	—	4	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	80	—	70	—	60	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	70	—	60	—	50	mA	t_{PC} = min	1, 3
Battery back up operating current (Standby with CBR refresh) (L-version)	I_{CC10}	—	100	—	100	—	100	µA	t_{RC} = 125 µs $t_{\overline{RAS}}$ ≤ 1 µs, $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address and Din = V_{IH} or V_{IL} Dout = High-Z	4
Self-refresh current (L-version)	I_{CC11}	—	100	—	100	—	100	µA	$\overline{RAS}$, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address and Din = V_{IH} or V_{IL} , Dout = High-Z	4
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
4. $V_{IH} \geq V_{CC} - 0.2$ V, $0 \text{ V} \leq V_{IL} \leq 0.2$ V.

Capacitance (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *1, *14, *15, *16

Test Conditions
Input rise and fall times : 5 ns
Input timing reference levels : 0.8 V, 2.0 V
Output timing reference levels : 0.8 V, 2.0 V
Output load : 1 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W4400B /BL-6		HM51W4400B /BL-7		HM51W4400B /BL-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	19
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	20
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	15	—	20	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3, 17
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13, 17
Access time from $\overline{OE}$	t_{OAC}	—	15	—	20	—	20	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	18
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn–off time	t_{OFF1}	0	15	0	20	0	20	ns	6
Output buffer turn–off time to $\overline{OE}$	t_{OFF2}	0	15	0	20	0	20	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	20	—	20	—	ns	
$\overline{OE}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	

Write cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	—	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	11

Read-modify-write cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	150	—	180	—	200	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	—	95	—	105	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	35	—	45	—	45	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	50	—	60	—	65	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	

Refresh cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast page mode cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	35	—	40	—	45	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	—	40	—	45	—	ns	

Fast page mode Read-modify-write Cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{PCM}	80	—	95	—	100	—	ns	
Fast page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	55	—	65	—	70	—	ns	10

Test mode cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	10	—	10	—	10	—	ns	

Counter test cycle

Parameter	Symbol	HM51W4400B /BL-6 Min	HM51W4400B /BL-6 Max	HM51W4400B /BL-7 Min	HM51W4400B /BL-7 Max	HM51W4400B /BL-8 Min	HM51W4400B /BL-8 Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	40	—	40	—	ns	

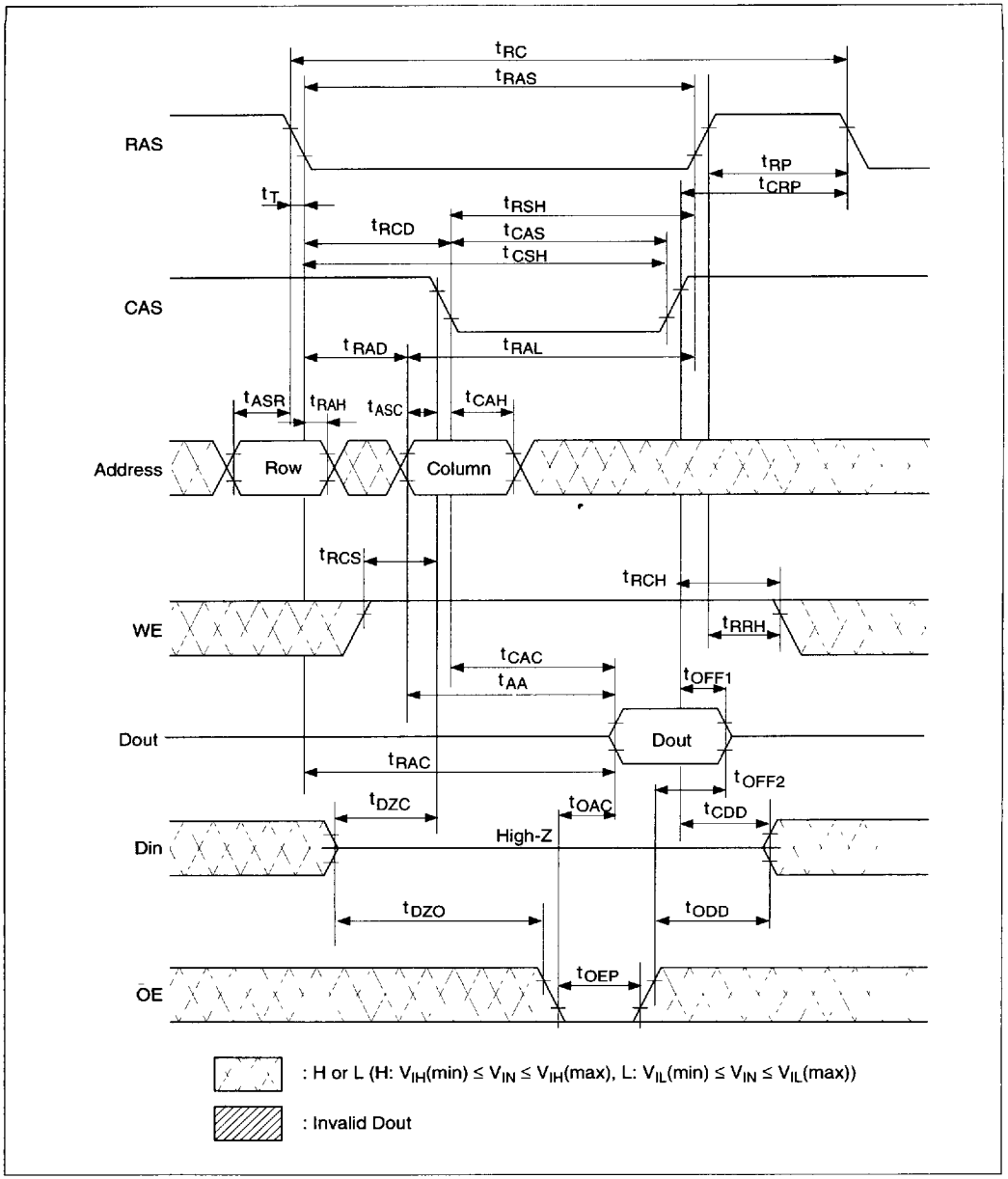
Self-refresh Mode (L-version)

Parameter	Symbol	HM51W4400BL -6 Min	HM51W4400BL -6 Max	HM51W4400BL -7 Min	HM51W4400BL -7 Max	HM51W4400BL -8 Min	HM51W4400BL -8 Max	Unit	Notes
$\overline{RAS}$ pulse width (self-refresh)	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{RAS}$ precharge time (self-refresh)	t_{RPS}	110	—	130	—	150	—	ns	
$\overline{CAS}$ hold time (self-refresh)	t_{CHS}	–50	—	–50	—	–50	—	ns	

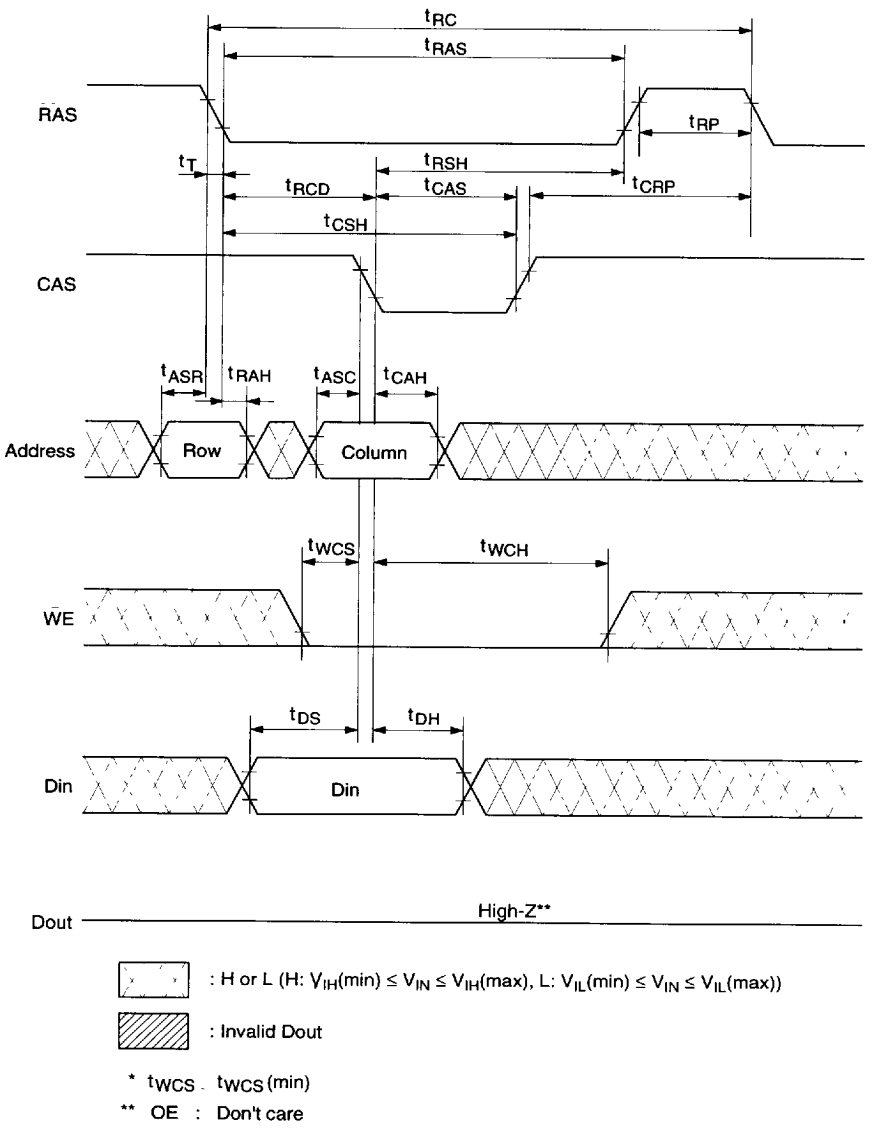
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$(max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{CPW} \geq t_{CPW}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits - - - CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. Either t_{RCH} or t_{RRH} must be satisfied
19. $t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T$ in read-modify-write cycle.
20. $t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T$ in read-modify-write cycle.

Timing Waveforms

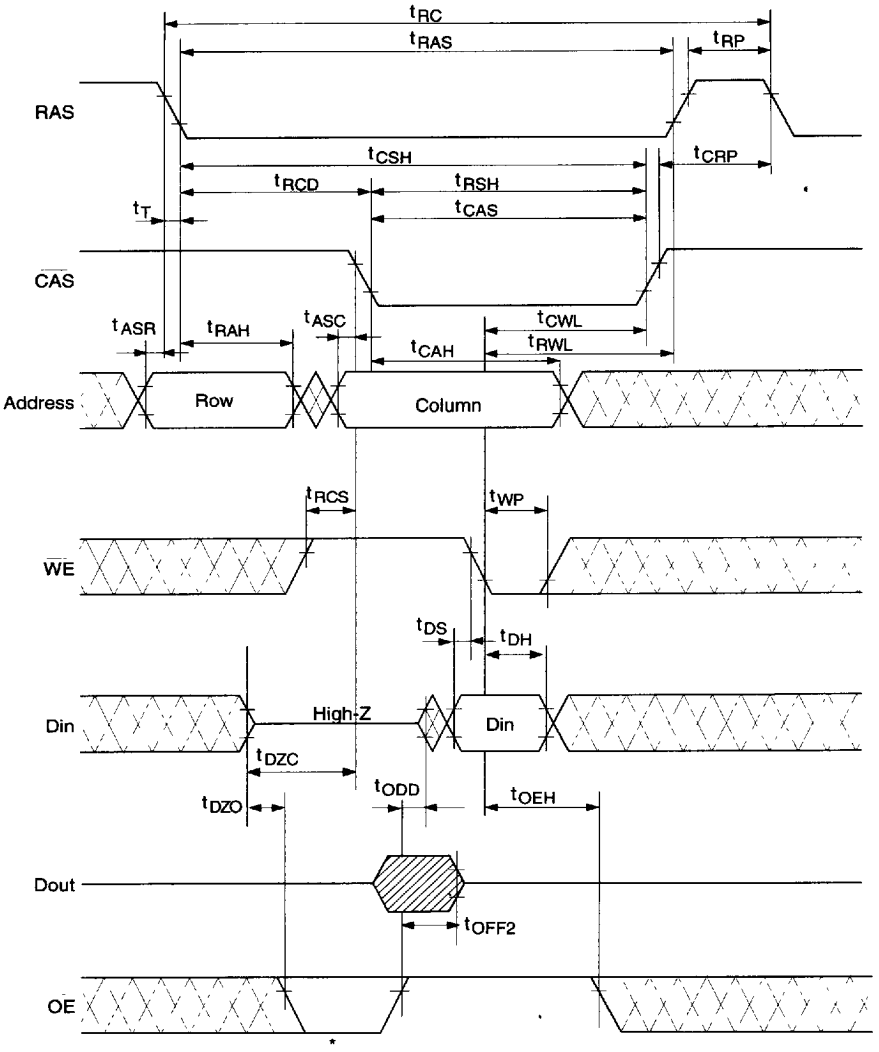
Read Cycle



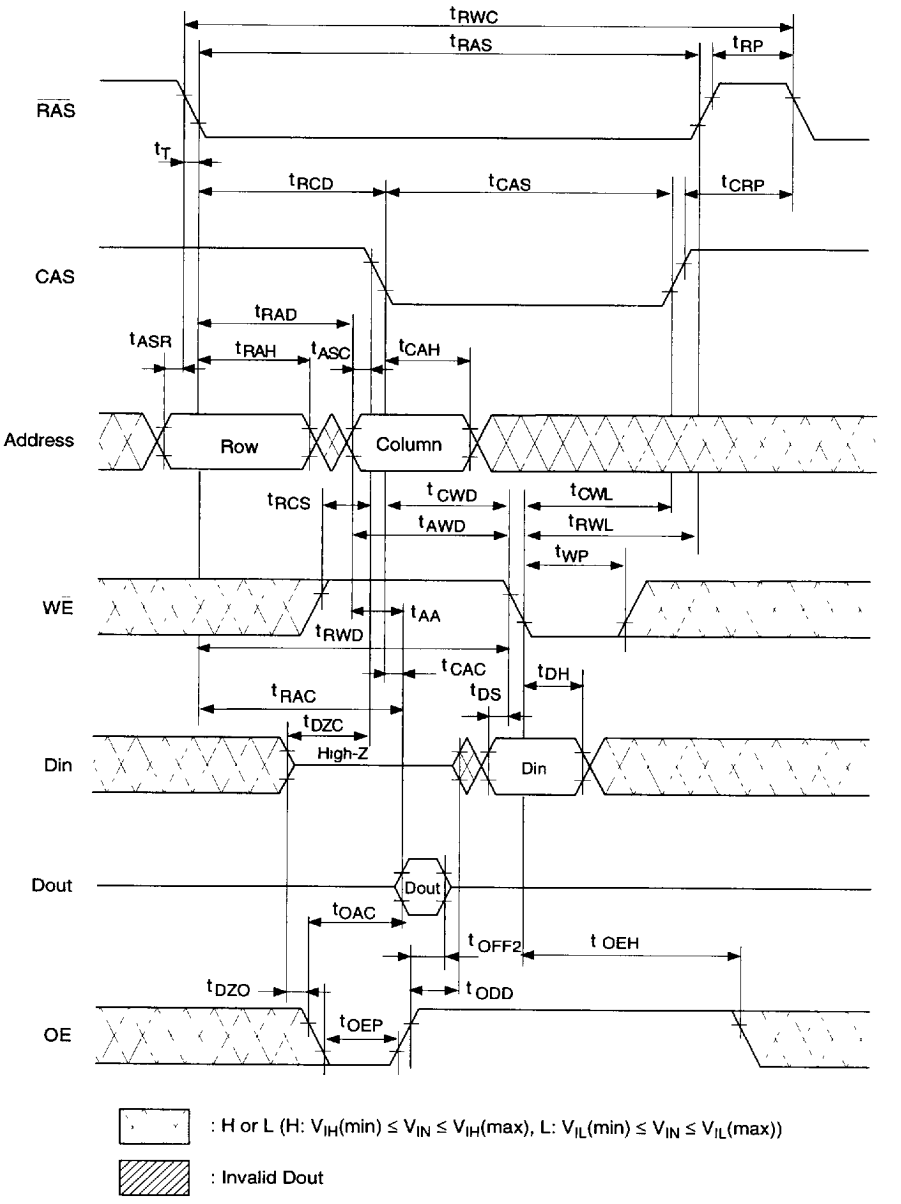
Early Write Cycle



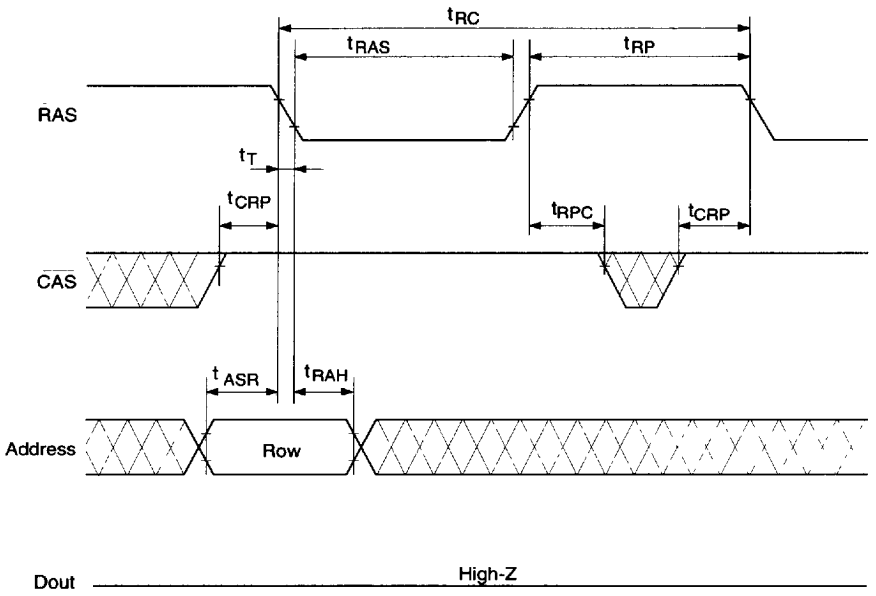
Delayed Write Cycle



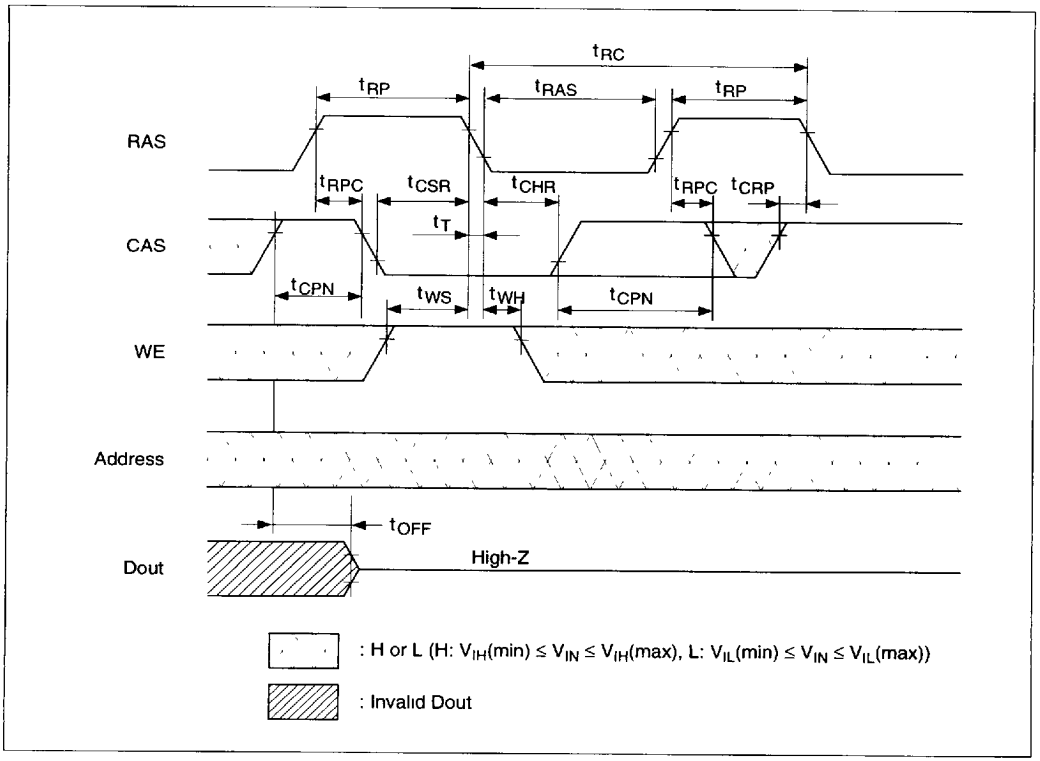
Read-Modify-Write Cycle



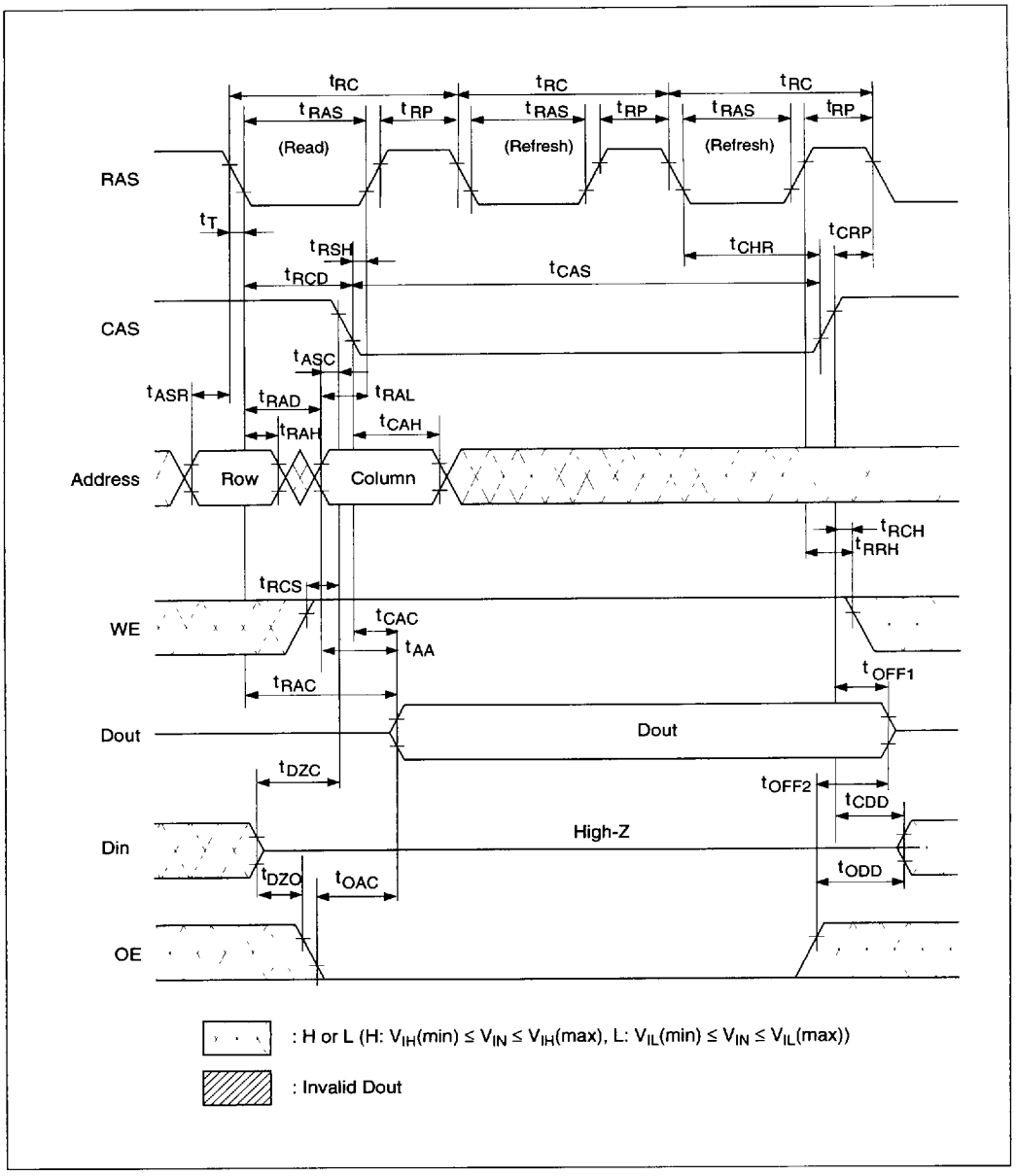
$\overline{\text{RAS}}$-Only Refresh Cycle



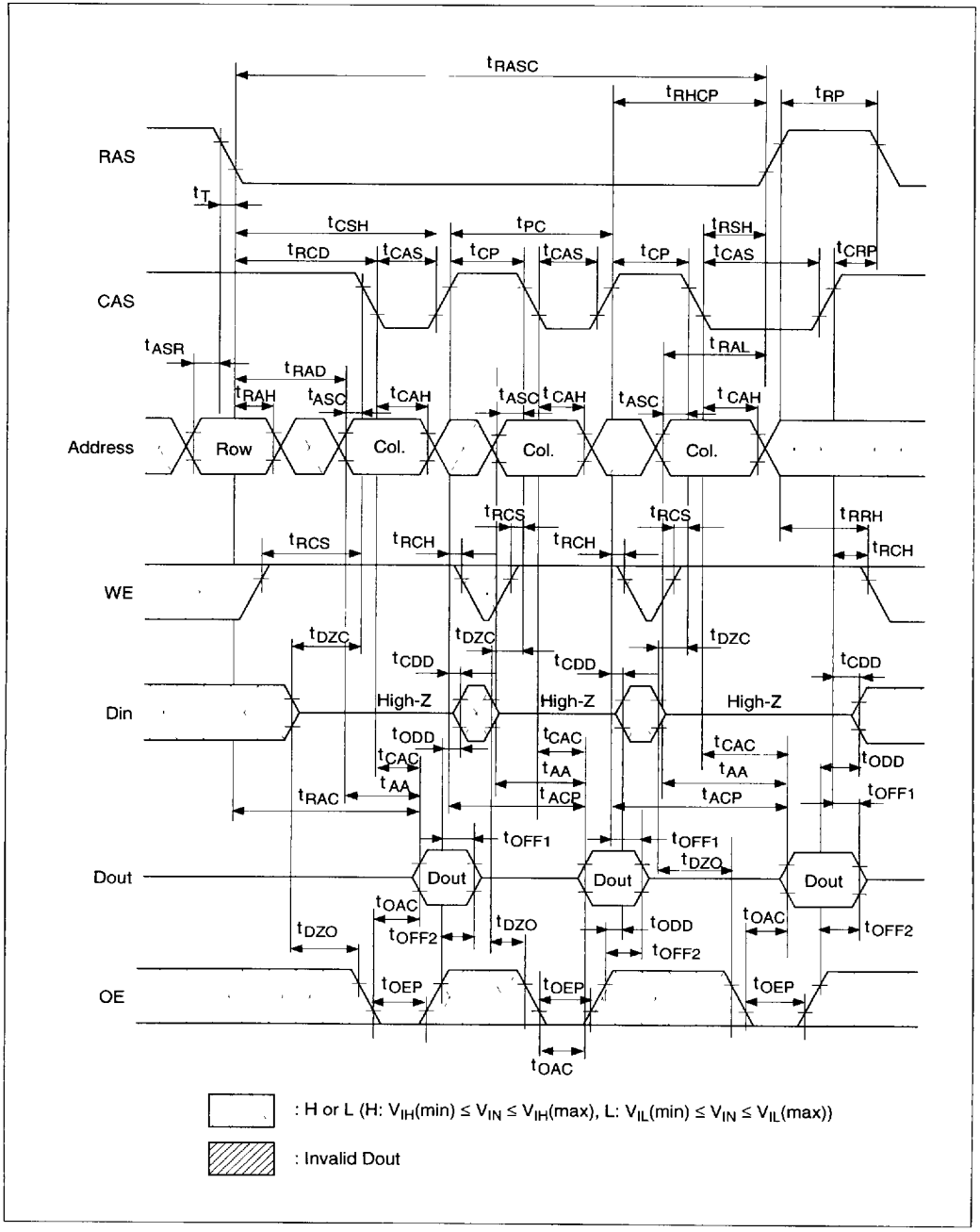
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



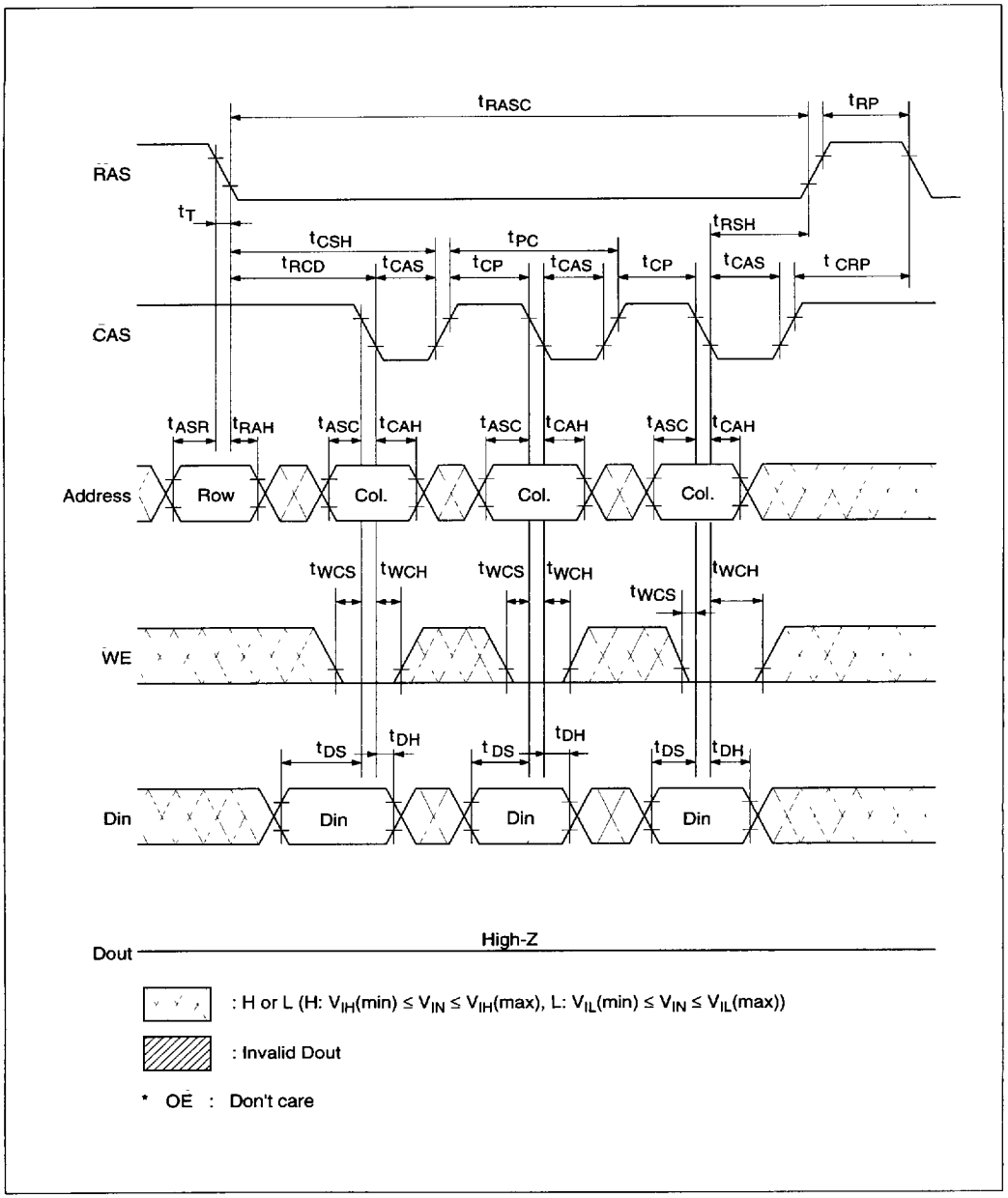
Hidden Refresh Cycle



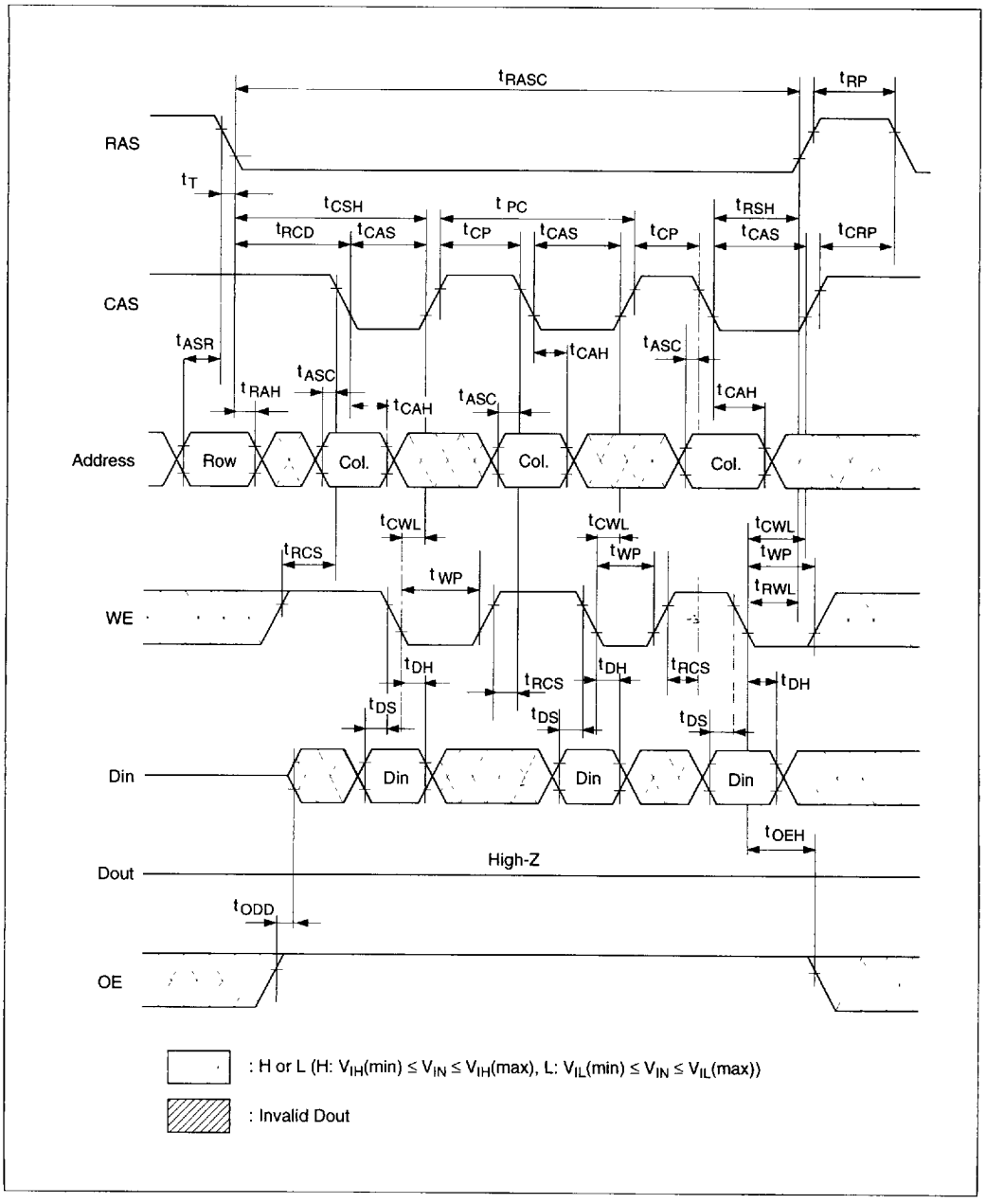
Fast Page Mode Read Cycle



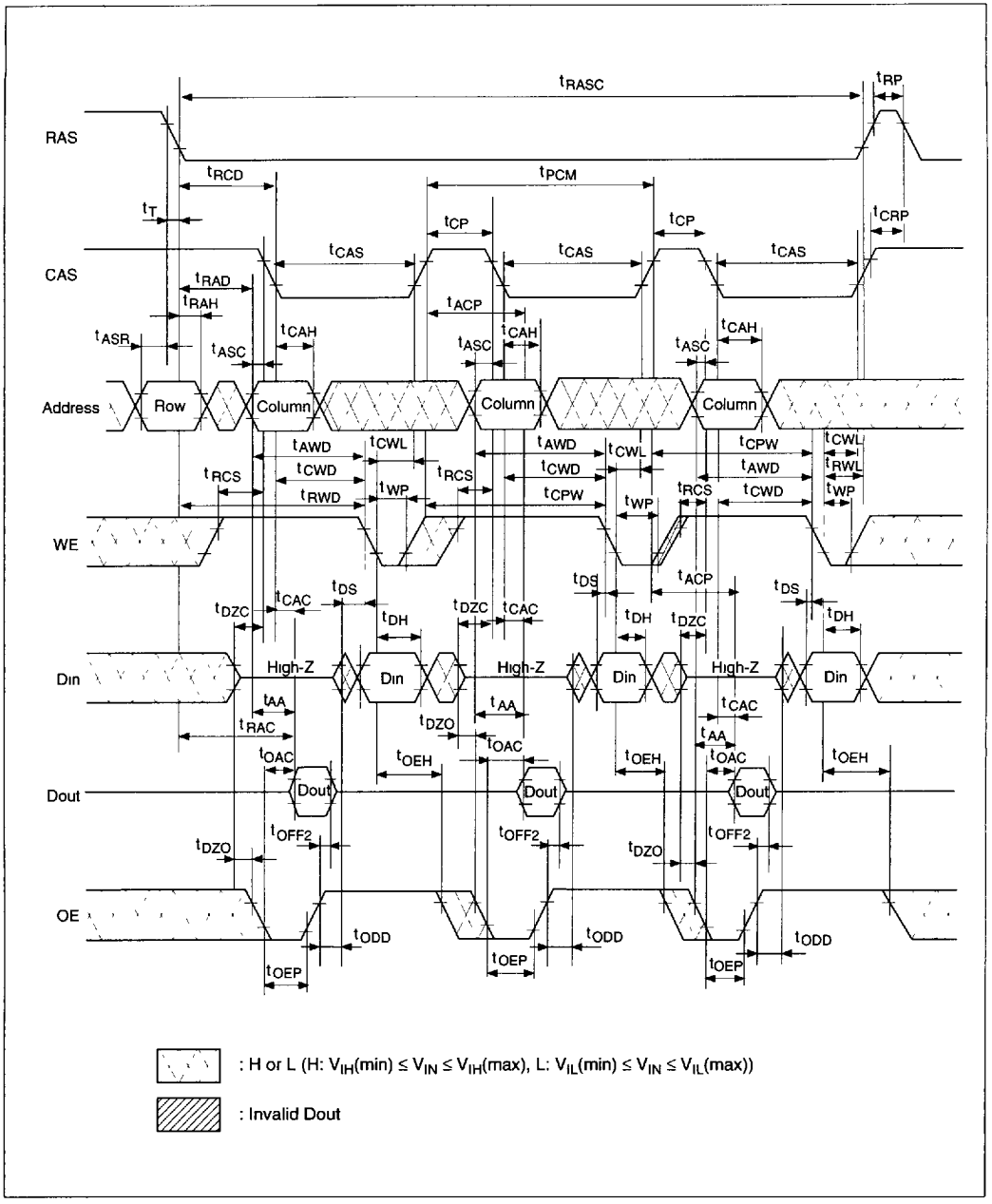
Fast Page Mode Early Write Cycle



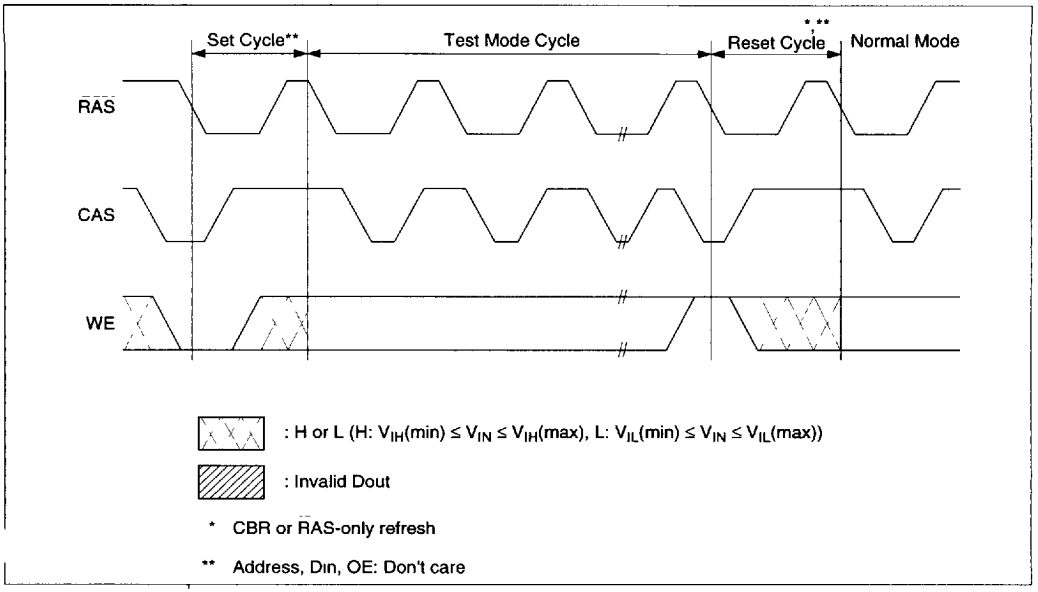
Fast Page Mode Delayed Write Cycle



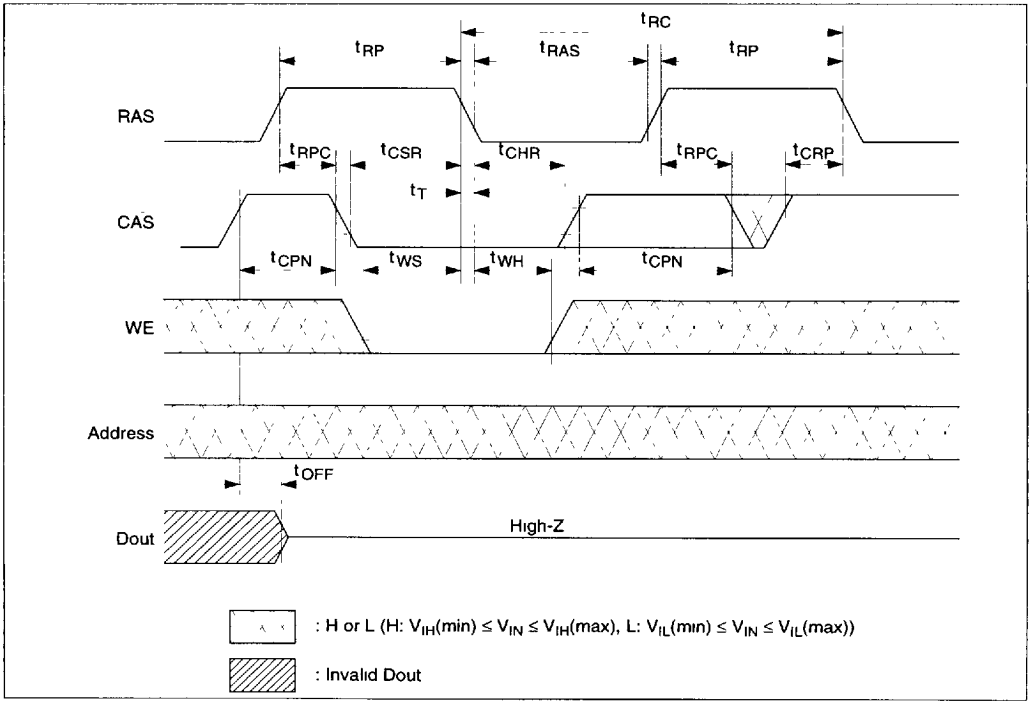
Fast Page Mode Read-Modify-Write Cycle



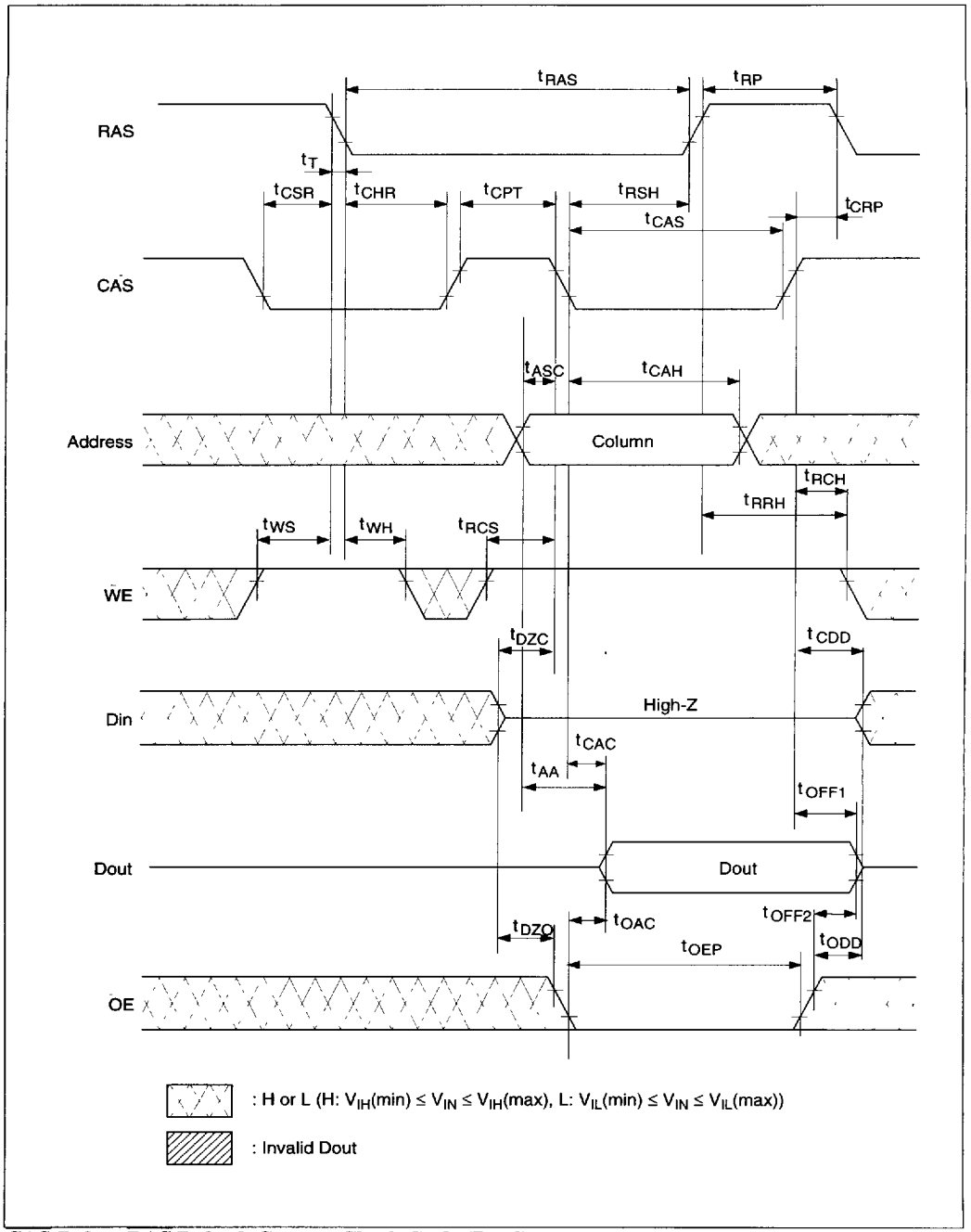
Test Mode Cycle



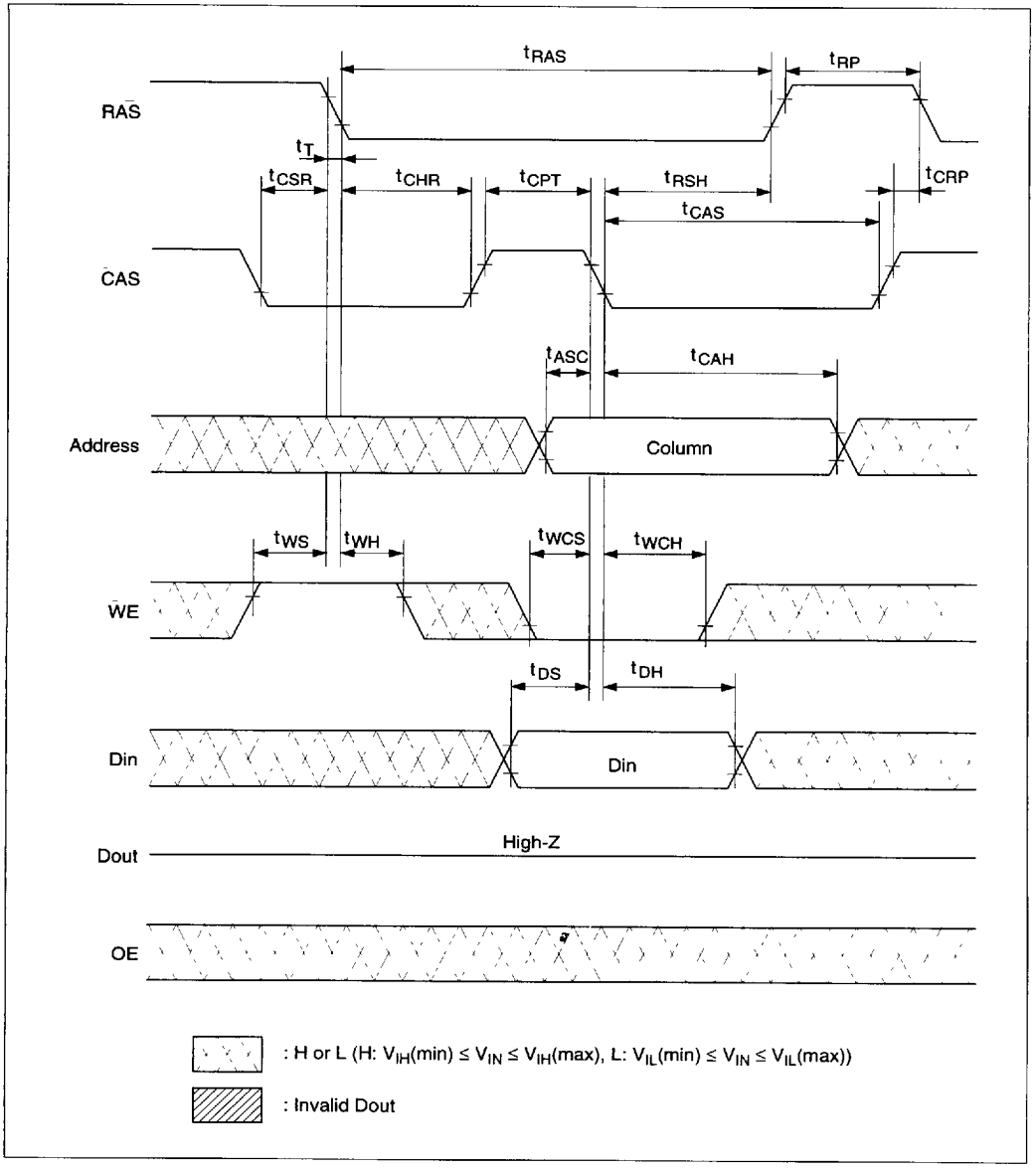
Test Mode Set Cycle



$\overline{WE}$-and-$\overline{CAS}$-Before $\overline{RAS}$-Refresh Cycle



CAS-Before-RAS Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)