Power management (dual transistors)

EMF32 / UMF32N

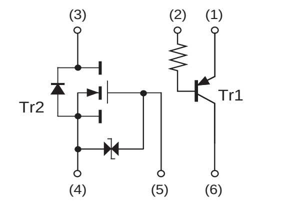
DTA143T and 2SK3019 are housed independently in a EMT6 package.

●Application
Power management circuit

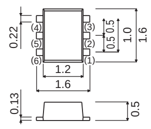
●Features
1) Power switching circuit in a single package.
2) Mounting cost and area can be cut in half.

●Structure
Silicon epitaxial planar transistor

●Inner circuits



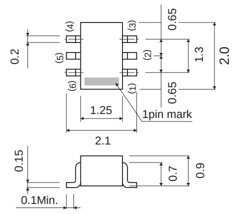
●Dimensions (Unit : mm)



ROHM : EMT6

Each lead has same dimensions

Abbreviated symbol : F32



ROHM : UMT6

Each lead has same dimensions

Abbreviated symbol : F32

●Packaging specifications

Type	EMF32	UMF32N
Package	EMT6	UMT6
Marking	F32	F32
Code	T2R	TR
Basic ordering unit (pieces)	8000	3000

●Absolute maximum ratings (Ta=25°C)

Tr1

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	–50	V
Collector-emitter voltage	V_{CEO}	–50	V
Emitter-base voltage	V_{EBO}	–5	V
Collector current	I_C	–100	mA
Power dissipation	P_C	150(TOTAL)	mW *1
Junction temperature	Tj	150	°C
Range of storage temperature	Tstg	–55 to +150	°C

*1 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

Tr2

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	100	mA
	Pulsed	I_{DP}	200	mA *1
Reverse drain current	Continuous	I_{DR}	100	mA
	Pulsed	I_{DRP}	200	mA *1
Total power dissipation		P_D	150(TOTAL)	mW *2
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	–55 to +150	°C

*1 PW≤10ms Duty cycle≤50%
*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

●Electrical characteristics (Ta=25°C)

Tr1

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	–50	–	–	V	I_C= –50μA
Collector-emitter breakdown voltage	BV_{CEO}	–50	–	–	V	I_C= –1mA
Emitter-base breakdown voltage	BV_{EBO}	–5	–	–	V	I_E= –50μA
Collector cutoff current	I_{CBO}	–	–	–0.5	μA	V_{CB}= –50V
Emitter cutoff current	I_{EBO}	–	–	–0.5	μA	V_{EB}= –4V
Collector-emitter saturation voltage	$V_{CE(sat)}$	–	–	–0.3	V	I_C/I_B= –5mA/ –0.25mA
DC current transfer ratio	h_{FE}	100	250	600	–	I_C= –1mA, V_{CE}= –5V
Input resistance	R_1	3.29	4.7	6.11	kΩ	–
Transition frequency	f_T	–	250	–	MHz	V_{CE}= –10V, I_E=5mA, f=100MHz *

* Transition frequency of the device

Tr2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±1	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	I_D=10μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1.0	μA	V_{DS}=30V, V_{GS}=0V
Gate-threshold voltage	$V_{GS(th)}$	0.8	–	1.5	V	V_{DS}=3V, I_D=100μA
Static drain-source on-state resistance	$R_{DS(on)}$	–	5	8	Ω	I_D=10mA, V_{GS}=4V
		–	7	13	Ω	I_D=1mA, V_{GS}=2.5V
Forward transfer admittance	$\|Y_{fs}\|$	20	–	–	ms	V_{DS}=3V, I_D=10mA
Input capacitance	C_{iss}	–	13	–	pF	V_{DS}=5V, V_{GS}=0V, f=1MHz
Output capacitance	C_{oss}	–	9	–	pF	
Reverce transfer capacitance	C_{rss}	–	4	–	pF	
Turn-on delay time	$t_{d(on)}$	–	15	–	ns	I_D=10mA, V_{DD} ≒5V, V_{GS}=5V, R_L=500Ω, R_{GS}=10Ω
Rise time	t_r	–	35	–	ns	
Turn-off delay time	$t_{d(off)}$	–	80	–	ns	
Fall time	t_f	–	80	–	ns	

●Electrical characteristic curves

Tr1

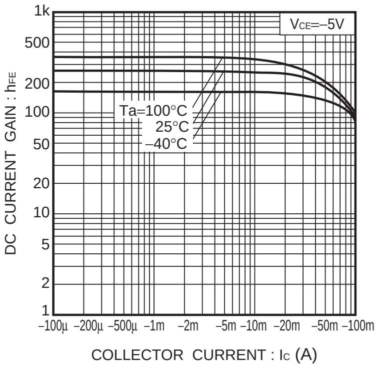


Fig.1 DC current gain vs. collector current

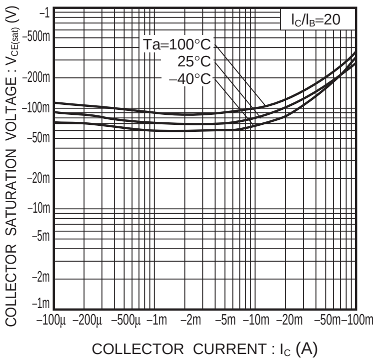


Fig.2 Collector-emitter saturation voltage vs. collector current

Tr2

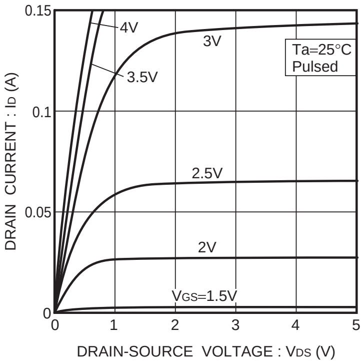


Fig.3 Typical output characteristics

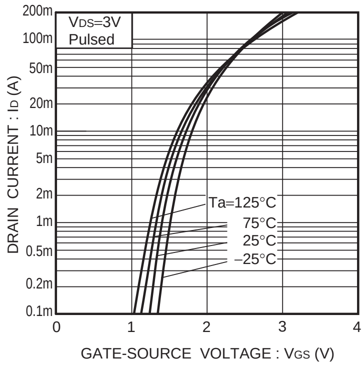


Fig.4 Typical transfer characteristics

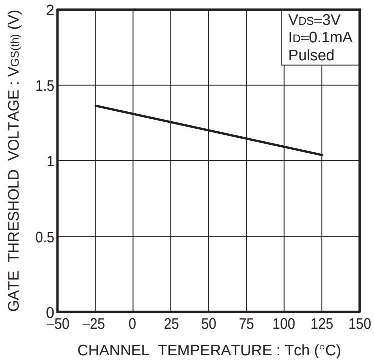


Fig.5 Gate threshold voltage vs. channel temperature

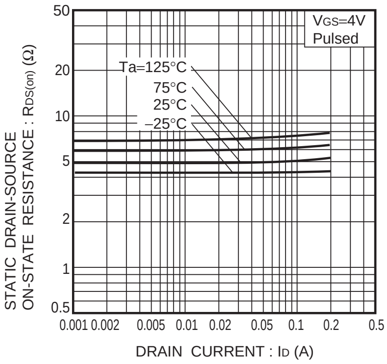


Fig.6 Static drain-source on-state resistance vs. drain current (I)

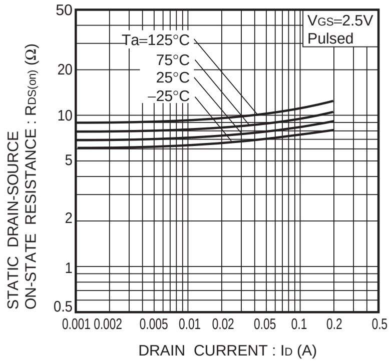


Fig.7 Static drain-source on-state resistance vs. drain current (II)

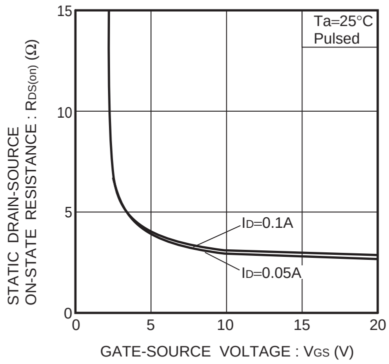


Fig.8 Static drain-source on-state resistance vs. gate-source voltage

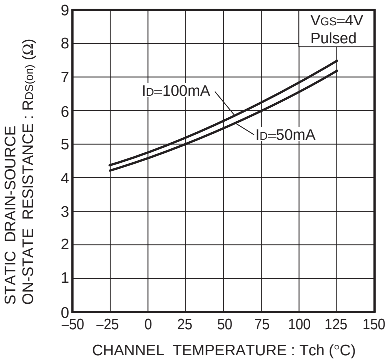


Fig.9 Static drain-source on-state resistance vs. channel temperature

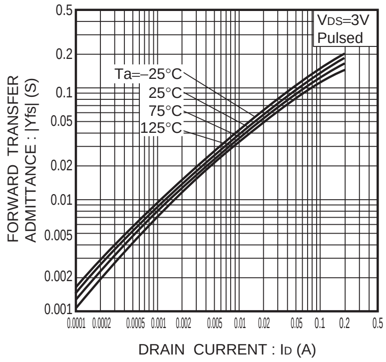


Fig.10 Forward transfer admittance vs. drain current

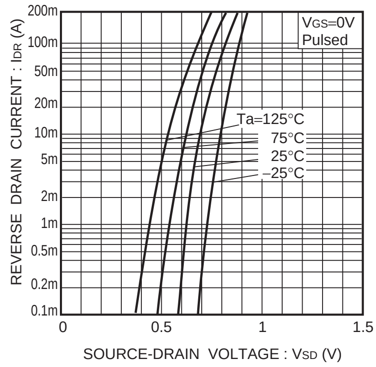


Fig.11 Reverse drain current vs. source-drain voltage (I)

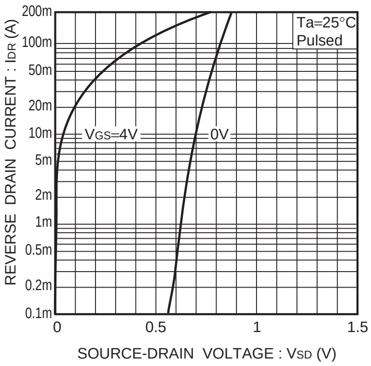


Fig.12 Reverse drain current vs. source-drain voltage (II)

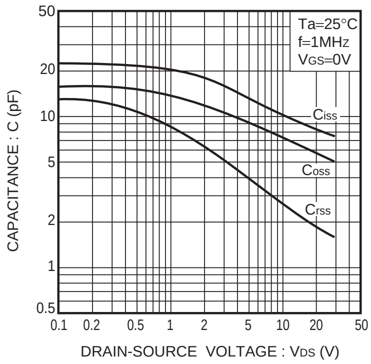


Fig.13 Typical capacitance vs. drain-source voltage

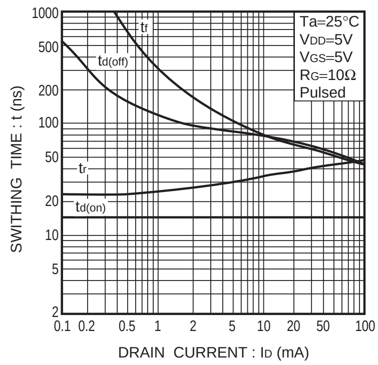


Fig.14 Switching characteristics

Notes

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