

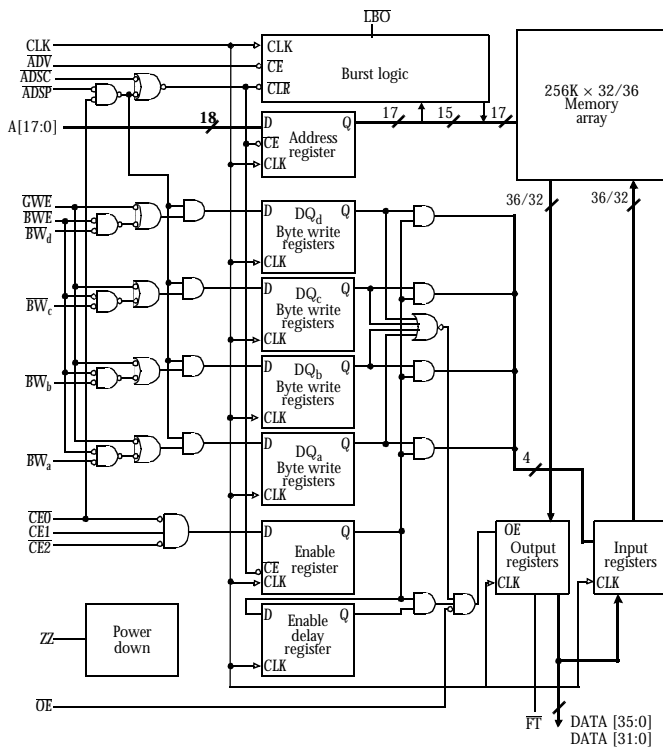


3.3V 256K × 32/36 pipeline burst synchronous SRAM

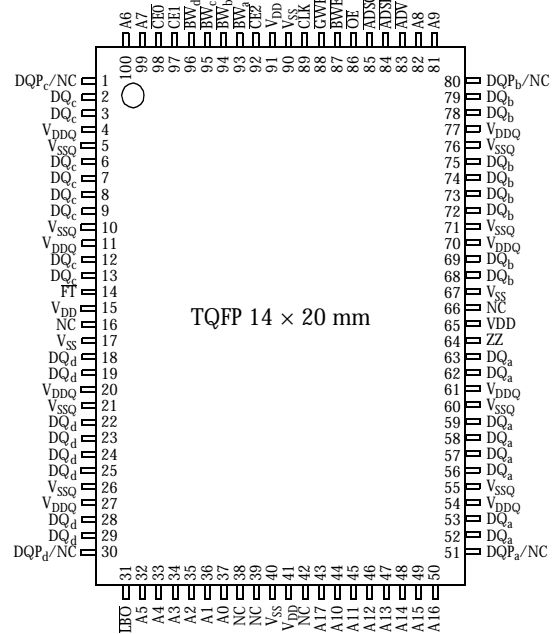
Features

- Organization: 262,144 words x 32 or 36 bits
- Fast clock speeds to 166 MHz in LVTTTL/LVCMOS
- Fast clock to data access: 3.5/3.8/4.0/5.0 ns
- Fast OE access time: 3.5/3.8/4.0/5.0 ns
- Fully synchronous register-to-register operation
- Single register “Flow-through” mode
- Single-cycle deselect
- Dual-cycle deselect also available (AS7C33256PFD32A/ AS7C33256PFD36A)
- Pentium®* compatible architecture and timing
- Asynchronous output enable control
- Economical 100-pin TQFP package
- Byte write enables
- Multiple chip enables for easy expansion
- 3.3V core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- 30 mW typical standby power in power down mode
- NTD™* pipeline architecture available (AS7C33256NTD32A/ AS7C33256NTD36A)

Logic block diagram



Pin arrangement



Note: Pins 1,30,51,80 are NC for ×32

Selection guide

	AS7C33256PFS32A -166	AS7C33256PFS32A -150	AS7C33256PFS32A -133	AS7C33256PFS32A -100	Units
Minimum cycle time	6	6.7	7.5	10	ns
Maximum clock frequency	166.7	150	133.3	100	MHz
Maximum pipelined clock access time	3.5	3.8	4	5	ns
Maximum operating current	475	450	425	325	mA
Maximum standby current	130	110	100	90	mA
Maximum CMOS standby current (DC)	30	30	30	30	mA

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Functional description

The AS7C33256PFS32A and AS7C33256PFS36A are high-performance CMOS 8-Mbit synchronous Static Random Access Memory (SRAM) devices organized as 262,144 words x 32 or 36 bits, and incorporate a two-stage register-register pipeline for highest frequency on any given technology.

Timing for these devices is compatible with existing Pentium® synchronous cache specifications. This architecture is suited for ASIC, DSP (TMS320C6X), and PowerPC™-based systems in computing, datacomm, instrumentation, and telecommunications systems.

Fast cycle times of 6/6.7/7.5/10 ns with clock access times (t_{CD}) of 3.5/3.8/4.0/5.0 ns enable 167, 150, 133 and 100 MHz bus frequencies. Three chip enable (CE) inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe (ADSC), or the processor address strobe (ADSP). The burst advance pin (ADV) allows subsequent internally generated burst addresses.

Read cycles are initiated with ADSP (regardless of WE and ADSC) using the new external address clocked into the on-chip address register when ADSP is sampled Low, the chip enables are sampled active, and the output buffer is enabled with OE. In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers and driven on the output pins on the next positive edge of CLK. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when ADV is sampled Low, and both address strobes are High. Burst operation is selectable with the LBO input. With LBO unconnected or driven High, burst operations use a Pentium® count sequence. With LBO driven LOW, the device uses a linear count sequence suitable for PowerPC™ and many other applications.

Write cycles are performed by disabling the output buffers with OE and asserting a write command. A global write enable GWE writes all 32/36 bits regardless of the state of individual BW[a:d] inputs. Alternately, when GWE is High, one or more bytes may be written by asserting BWE and the appropriate individual byte BWn signal(s).

BWn is ignored on the clock edge that samples ADSP Low, but is sampled on all subsequent clock edges. Output buffers are disabled when BWn is sampled LOW (regardless of OE). Data is clocked into the data input register when BWn is sampled Low. Address is incremented internally to the next burst address if BWn and ADV are sampled Low.

Read or write cycles may also be initiated with ADSC instead of ADSP. The differences between cycles initiated with ADSC and ADSP follow.

- ADSP must be sampled HIGH when ADSC is sampled LOW to initiate a cycle with ADSC.
- WE signals are sampled on the clock edge that samples ADSC LOW (and ADSP High).
- Master chip enable CEO blocks ADSP, but not ADSC.

AS7C33256PFS32A and AS7C33256PFS36A family operates from a core 3.3V power supply. I/Os use a separate power supply that can operate at 2.5V or 3.3V. These devices are available in a 100-pin 14 × 20 mm TQFP package.

*PowerPC™ is a trademark International Business Machines Corporation.

Capacitance

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	$V_{IN} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	$V_{IN} = V_{OUT} = 0V$	7	pF

Write enable truth table (per byte)

GWE	BWE	BWn	WEn
L	X	X	T
H	L	L	T
H	H	X	F*
H	L	H	F*

Key:

X = Don't Care, L = Low, H = High, T = True, F = False; * = Valid read; n = a, b, c, d; WE, WEn = internal write signal.



Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except \overline{OE} , \overline{FT} , \overline{ZZ} , \overline{LBO} are synchronous to this clock.
A0–A17	I	SYNC	Address. Sampled when all chip enables are active and \overline{ADSP} or \overline{ADSC} are asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and \overline{OE} is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when \overline{ADSP} or \overline{ADSC} is active. When $\overline{CE0}$ is inactive, \overline{ADSP} is blocked. Refer to the Synchronous Truth Table for more information.
$\overline{CE1}$, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active Low, respectively. Sampled on clock edges when \overline{ADSC} is active or when $\overline{CE0}$ and \overline{ADSP} are active.
\overline{ADSP}	I	SYNC	Address strobe processor. Asserted LOW to load a new bus address or to enter standby mode.
\overline{ADSC}	I	SYNC	Address strobe controller. Asserted LOW to load a new address or to enter standby mode.
\overline{ADV}	I	SYNC	Advance. Asserted LOW to continue burst read/write.
\overline{GWE}	I	SYNC	Global write enable. Asserted LOW to write all 32/36 bits. When High, \overline{BWE} and $\overline{BW[a:d]}$ control write enable.
\overline{BWE}	I	SYNC	Byte write enable. Asserted LOW with $\overline{GWE} = \text{HIGH}$ to enable effect of $\overline{BW[a:d]}$ inputs.
$\overline{BW[a,b,c,d]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE} = \text{HIGH}$ and $\overline{BWE} = \text{Low}$. If any of $\overline{BW[a:d]}$ is active with $\overline{GWE} = \text{HIGH}$ and $\overline{BWE} = \text{LOW}$ the cycle is a write cycle. If all $\overline{BW[a:d]}$ are inactive the cycle is a read cycle.
\overline{OE}	I	ASYNCR	Asynchronous output enable. I/O pins are driven when \overline{OE} is active and the chip is in read mode.
\overline{LBO}	I	STATIC default = HIGH	Count mode. When driven High, count sequence follows Intel XOR convention. When driven Low, count sequence follows linear convention. This signal is internally pulled High. ¹⁸
\overline{FT}	I	STATIC	Flow-through mode. When low, enables single register flow-through mode. Connect to V_{DD} if unused or for pipelined operation.
\overline{ZZ}	I	ASYNCR	Sleep. Places device in low power mode; data is retained. Connect to GND if unused.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD} , V_{DDQ}	-0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	-0.5	$V_{DD} + 0.5$	V
Input voltage relative to GND (I/O pins)	V_{IN}	-0.5	$V_{DDQ} + 0.5$	V
Power dissipation	P_D	–	1.8	W
DC output current	I_{OUT}	–	50	mA
Storage temperature (plastic)	T_{stg}	-65	+150	°C
Temperature under bias	T_{bias}	-65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.



Synchronous truth table

CE0	CE1	CE2	ADSP	ADSC	ADV	WEN ¹	OE	Address accessed	CLK	Operation	DQ
H	X	X	X	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	L	X	L	X	X	X	X	NA	L to H	Deselect	Hi-Z
L	L	X	H	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	X	H	L	X	X	X	X	NA	L to H	Deselect	Hi-Z
L	X	H	H	L	X	X	X	NA	L to H	Deselect	Hi-Z
L	H	L	L	X	X	X	L	External	L to H	Begin read	Hi-Z ²
L	H	L	L	X	X	X	H	External	L to H	Begin read	Hi-Z
L	H	L	H	L	X	F	L	External	L to H	Begin read	Hi-Z ²
L	H	L	H	L	X	F	H	External	L to H	Begin read	Hi-Z
X	X	X	H	H	L	F	L	Next	L to H	Cont. read	Q
X	X	X	H	H	L	F	H	Next	L to H	Cont. read	Hi-Z
X	X	X	H	H	H	F	L	Current	L to H	Suspend read	Q
X	X	X	H	H	H	F	H	Current	L to H	Suspend read	Hi-Z
H	X	X	X	H	L	F	L	Next	L to H	Cont. read	Q
H	X	X	X	H	L	F	H	Next	L to H	Cont. read	Hi-Z
H	X	X	X	H	H	F	L	Current	L to H	Suspend read	Q
H	X	X	X	H	H	F	H	Current	L to H	Suspend read	Hi-Z
L	H	L	H	L	X	T	X	External	L to H	Begin write	D ³
X	X	X	H	H	L	T	X	Next	L to H	Cont. write	D
H	X	X	X	H	L	T	X	Next	L to H	Cont. write	D
X	X	X	H	H	H	T	X	Current	L to H	Suspend write	D
H	X	X	X	H	H	T	X	Current	L to H	Suspend write	D

Key: X = Don't Care, L = Low, H = High.

¹See "Write enable truth table" on page 2 for more information.

²Q in flow through mode.

³For write operation following a READ, OE must be HIGH before the input data set up time and held HIGH throughout the input hold time.

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V _{DD}	3.135	3.3	3.6	V
		V _{SS}	0.0	0.0	0.0	
3.3V I/O supply voltage		V _{DDQ}	3.135	3.3	3.6	V
		V _{SSQ}	0.0	0.0	0.0	
2.5V I/O supply voltage		V _{DDQ}	2.35	2.5	2.9	V
		V _{SSQ}	0.0	0.0	0.0	
Input voltages [†]	Address and control pins	V _{IH}	2.0	-	V _{DD} + 0.3	V
		V _{IL}	-0.5*	-	0.8	
	I/O pins	V _{IH}	2.0	-	V _{DDQ} + 0.3	V
		V _{IL}	-0.5*	-	0.8	
Ambient operating temperature		T _A	0	-	70	°C



* V_{IL} min = -2.0V for pulse width less than $0.2 \times t_{RC}$.

† Input voltage ranges apply to 3.3V I/O operation. For 2.5V I/O operation, contact factory for input specifications.

TQFP thermal resistance

Description	Conditions		Symbol	Typical	Units
Thermal resistance (junction to ambient)*	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	1-layer	θ_{JA}	40	°C/W
		4-layer	θ_{JA}	22	°C/W
Thermal resistance (junction to top of case)*			θ_{JC}	8	°C/W

* This parameter is sampled.

DC electrical characteristics

Parameter	Symbol	Test conditions	-166		-150		-133		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current*	$ I_{LI} $	$V_{DD} = \text{Max}, V_{IN} = \text{GND to } V_{DD}$	-	2	-	2	-	2	-	2	μA
Output leakage current	$ I_{LO} $	$\overline{OE} \geq V_{IH}, V_{DD} = \text{Max}, V_{OUT} = \text{GND to } V_{DD}$	-	2	-	2	-	2	-	2	μA
Operating power supply current	I_{CC}	$\overline{CE0} = V_{IL}, \overline{CE1} = V_{IH}, \overline{CE2} = V_{IL}, f = f_{Max}, I_{OUT} = 0 \text{ mA}$	-	475	-	450	-	425	-	325	mA
Standby power supply current	I_{SB}	Deselected, $f = f_{Max}, ZZ \leq V_{IL}$	-	130	-	110	-	100	-	90	mA
	I_{SB1}	Deselected, $f = 0, ZZ \leq 0.2V$ all $V_{IN} \leq 0.2V$ or $\geq V_{DD} - 0.2V$	-	30	-	30	-	30	-	30	
	I_{SB2}	Deselected, $f = f_{Max}, ZZ \geq V_{DD} - 0.2V$ All $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$	-	30	-	30	-	30	-	30	
Output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{DDQ} = 3.465V$	-	0.4	-	0.4	-	0.4	-	0.4	V
	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{DDQ} = 3.135V$	2.4	-	2.4	-	2.4	-	2.4	-	

* \overline{LBO} pin has an internal pull-up and input leakage = $\pm 10 \mu A$.

Note: I_{CC} given with no output loading. I_{CC} increases with faster cycles times and greater output loading.

DC electrical characteristics for 2.5V I/O operation

Parameter	Symbol	Test conditions	-166		-150		-133		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Output leakage current	$ I_{LO} $	$\overline{OE} \geq V_{IH}, V_{DD} = \text{Max}, V_{OUT} = \text{GND to } V_{DD}$	-1	1	-1	1	-1	1	-1	1	μA
Output voltage	V_{OL}	$I_{OL} = 2 \text{ mA}, V_{DDQ} = 2.65V$	-	0.7	-	0.7	-	0.7	-	0.7	V
	V_{OH}	$I_{OH} = -2 \text{ mA}, V_{DDQ} = 2.35V$	1.7	-	1.7	-	1.7	-	1.7	-	

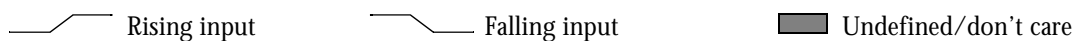


Timing characteristics over operating range

Parameter	Symbol	-166		-150		-133		-100		Unit	Notes*
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock frequency	f _{Max}	-	166	-	150	-	133	-	100	MHz	
Cycle time (pipelined mode)	t _{CYC}	6	-	6.6	-	7.5	-	10	-	ns	
Cycle time (flow-through mode)	t _{CYCF}	10	-	10	-	12	-	12	-	ns	
Clock access time (pipelined mode)	t _{CD}	-	3.5	-	3.8	-	4.0	-	5.0	ns	
Clock access time (flow-through mode)	t _{CDF}	-	9	-	10	-	10	-	12	ns	
Output enable LOW to data valid	t _{OE}	-	3.5	-	3.8	-	4.0	-	5.0	ns	
Clock HIGH to output Low Z	t _{LZC}	0	-	0	-	0	-	0	-	ns	2,3,4
Data output invalid from clock HIGH	t _{OH}	1.5	-	1.5	-	1.5	-	1.5	-	ns	2
Output enable LOW to output Low Z	t _{LZOE}	0	-	0	-	0	-	0	-	ns	2,3,4
Output enable HIGH to output High Z	t _{HZOE}	-	3.5	-	3.8	-	4.0	-	4.5	ns	2,3,4
Clock HIGH to output High Z	t _{HZC}	-	3.5	-	3.8	-	4.0	-	5.0	ns	2,3,4
Output enable HIGH to invalid output	t _{OHOE}	0	-	0	-	0	-	0	-	ns	
Clock HIGH pulse width	t _{CH}	2.4	-	2.5	-	2.5	-	3.5	-	ns	5
Clock LOW pulse width	t _{CL}	2.4	-	2.5	-	2.5	-	3.5	-	ns	5
Address setup to clock HIGH	t _{AS}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6
Data setup to clock HIGH	t _{DS}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6
Write setup to clock HIGH	t _{WS}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6,7
Chip select setup to clock HIGH	t _{CSS}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6,8
Address hold from clock HIGH	t _{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6
Data hold from clock HIGH	t _{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6
Write hold from clock HIGH	t _{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6,7
Chip select hold from clock HIGH	t _{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6,8
\overline{ADV} setup to clock HIGH	t _{ADV\overline{S}}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6
\overline{ADSP} setup to clock HIGH	t _{ADSP\overline{S}}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6
\overline{ADSC} setup to clock HIGH	t _{ADSC\overline{S}}	1.5	-	1.5	-	1.5	-	2.0	-	ns	6
\overline{ADV} hold from clock HIGH	t _{ADV\overline{H}}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6
\overline{ADSP} hold from clock HIGH	t _{ADSP\overline{H}}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6
\overline{ADSC} hold from clock HIGH	t _{ADSC\overline{H}}	0.5	-	0.5	-	0.5	-	0.5	-	ns	6

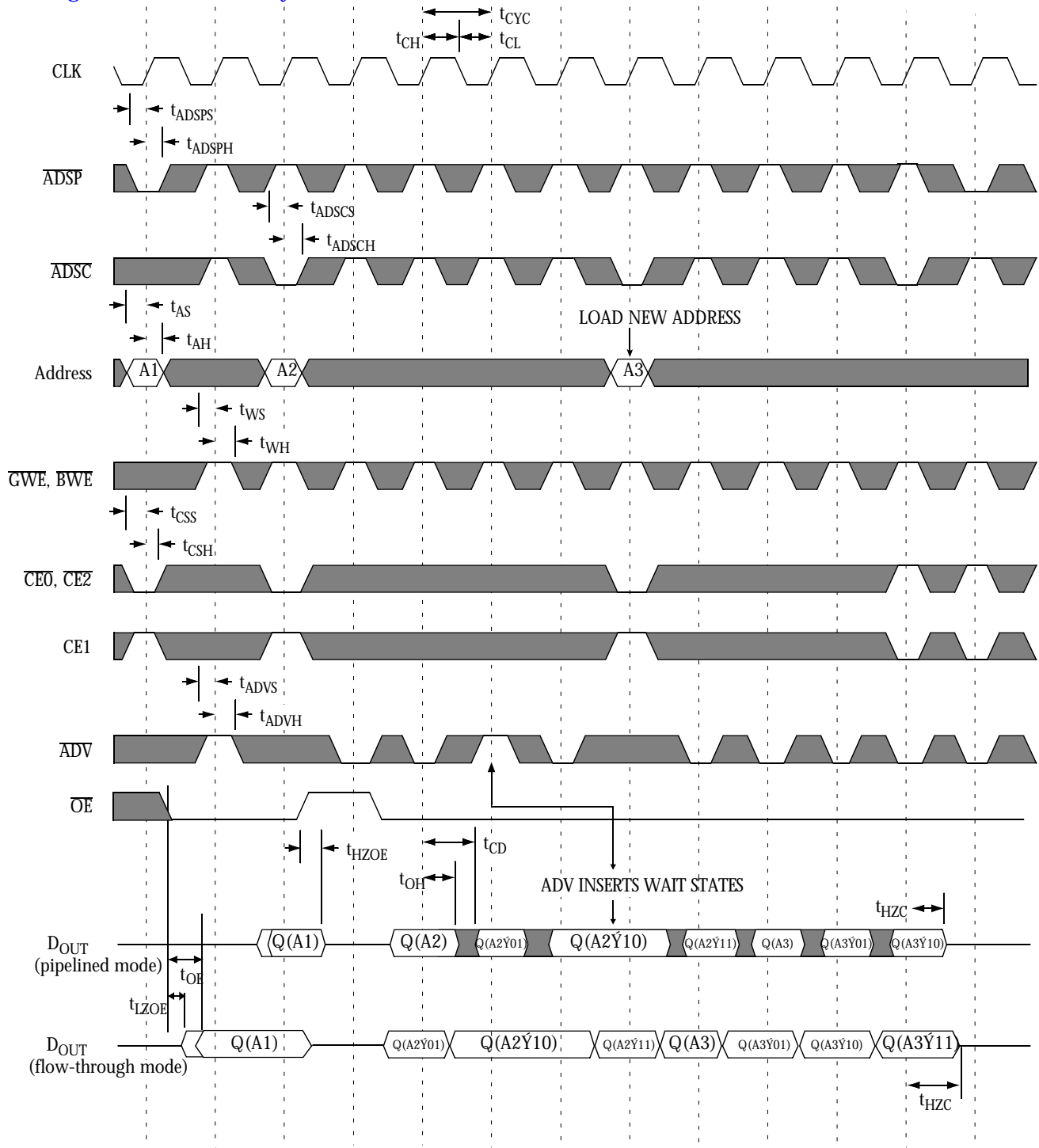
*See "Notes" on page 10.

Key to switching waveforms





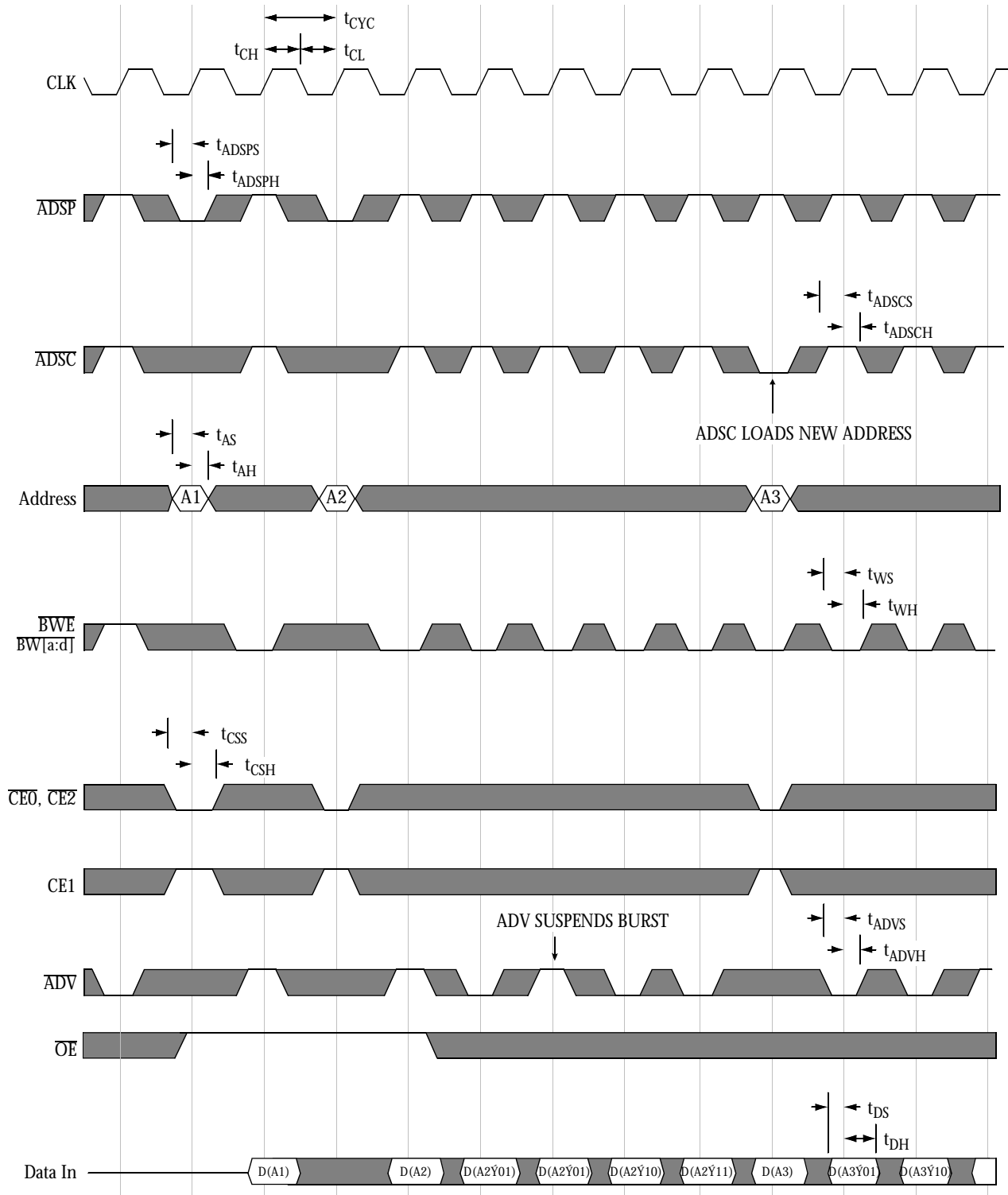
Timing waveform of read cycle



Note: \hat{Y} = XOR when MODE = HIGH/No Connect; \check{Y} = ADD when MODE = LOW.
BW[a:d] is don't care.



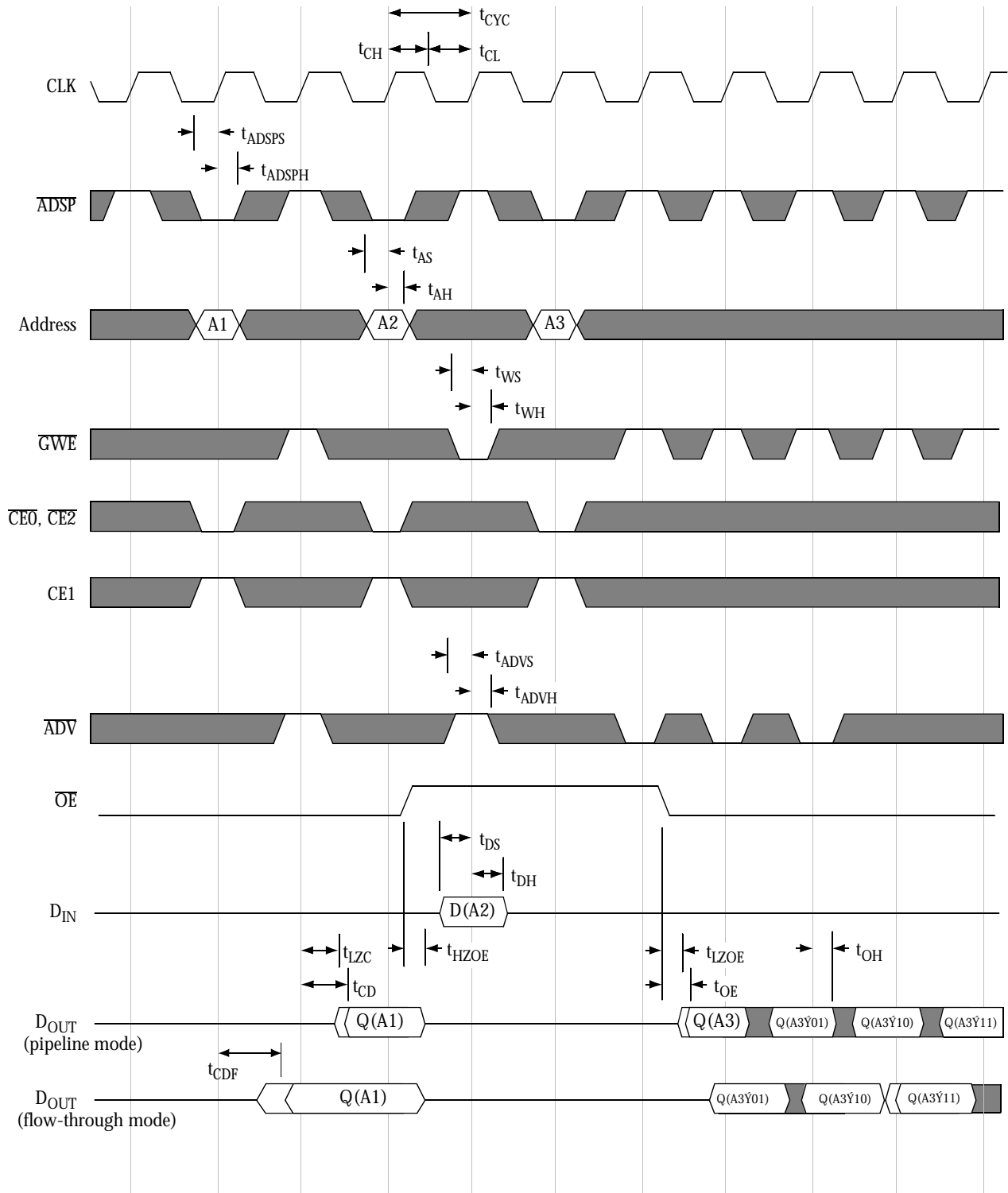
Timing waveform of write cycle



Note: \bar{Y} = XOR when MODE = HIGH/No Connect; \bar{Y} = ADD when MODE = LOW.



Timing waveform of read/write cycle



Note: Y = XOR when MODE = HIGH/No Connect; Y = ADD when MODE = LOW.



AC test conditions

- Output load: see Figure B, except for t_{LZC} , t_{LZOE} , t_{HZOE} , t_{HZC} , see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

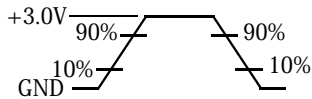


Figure A: Input waveform

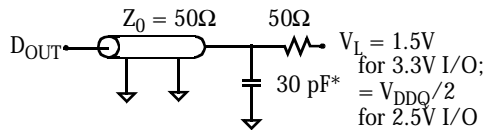


Figure B: Output load (A)

Thevenin equivalent:

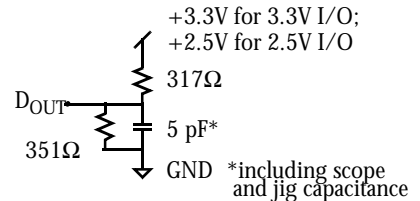


Figure C: Output load(B)

Notes

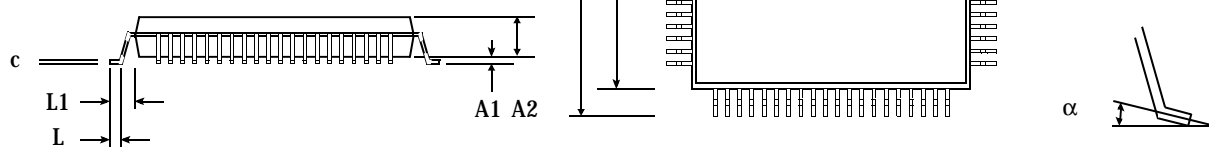
- 1 For test conditions, see AC Test Conditions, Figures A, B, C.
- 2 This parameter measured with output load condition in Figure C.
- 3 This parameter is sampled, but not 100% tested.
- 4 t_{HZOE} is less than t_{LZOE} ; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
- 5 t_{CH} measured as HIGH above V_{IH} and t_{CL} measured as LOW below V_{IL} .
- 6 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times for all rising edges of CLK when chip is enabled.
- 7 Write refers to \overline{GWE} , \overline{BWE} , $\overline{BW[a:d]}$.
- 8 Chip select refers to $\overline{CE0}$, $\overline{CE1}$, $\overline{CE2}$.

Package Dimensions

100-pin quad flat pack (TQFP)

	TQFP	
	Min	Max
A1	0.05	0.15
A2	1.35	1.45
b	0.22	0.38
c	0.09	0.20
D	13.90	14.10
E	19.90	20.10
e	0.65 nominal	
Hd	15.90	16.10
He	21.90	22.10
L	0.45	0.75
L1	1.00 nominal	
α	0°	7°

Dimensions in millimeters





Ordering information

-166 MHz	-150 MHz	-133 MHz	-100 MHz
AS7C33256PFS32A-166TQC	AS7C33256PFS32A-150TQC	AS7C33256PFS32A-133TQC	AS7C33256PFS32A-100TQC
AS7C33256PFS32A-166TQI	AS7C33256PFS32A-150TQI	AS7C33256PFS32A-133TQI	AS7C33256PFS32A-100TQI
AS7C33256PFS36A-166TQC	AS7C33256PFS36A-150TQC	AS7C33256PFS36A-133TQC	AS7C33256PFS36A-100TQC
AS7C33256PFS36A-166TQI	AS7C33256PFS36A-150TQI	AS7C33256PFS36A-133TQI	AS7C33256PFS36A-100TQI

Part numbering guide

AS7C	33	256	PF	S	32/36	A	-XXX	TQ	C/I
1	2	3	4	5	6	7	8	9	10

1. Alliance Semiconductor SRAM prefix
2. Operating voltage: 33=3.3V
3. Organization: 256=256K
4. Pipeline-Flowthrough (each device works in both modes)
5. Deselect: S=Single cycle deselect
6. Organization: 32=x32; 36=x36
7. Production version: A=first production version
8. Clock speed (MHz)
9. Package type: TQ=TQFP
10. Operating temperature: C=Commercial (0° C to 70° C); I=Industrial (-40° C to 85° C)