THV3543

2 channel Buck/Boost 2 channel Charge Pump Controller

Description

THV3543 is a controller IC for multi-channel power supply system which includes 2 channel DC/DC converter with built-in power MOSFETs and 2 channel charge pump circuits.
THV3543 has internal soft start, under voltage protection, over voltage protection and over current protection.
CH-1 is a Boost DC/DC converter which can provide two optional modes of output voltage: the adjustable mode with external resistor or the fixed 15.6V mode requires no external resistors.
CH-2 is a Buck DC/DC converter. Its output voltage is fixed at 3.3V.
Positive charge pump (VGH) and negative charge pump (VGL) can provide two optional modes of output voltage: the adjustable mode with external resistor or the fixed mode (VGH at 35.6V, VGL at -6V) requires no external resistors.
THV3543 has LDO and operational amplifier which can be used for Half AVDD or Vcom.
Thus THV3543 can produce various necessary voltages for LCD panels and ideal for constructing TFT-LCD Bias power supply system.

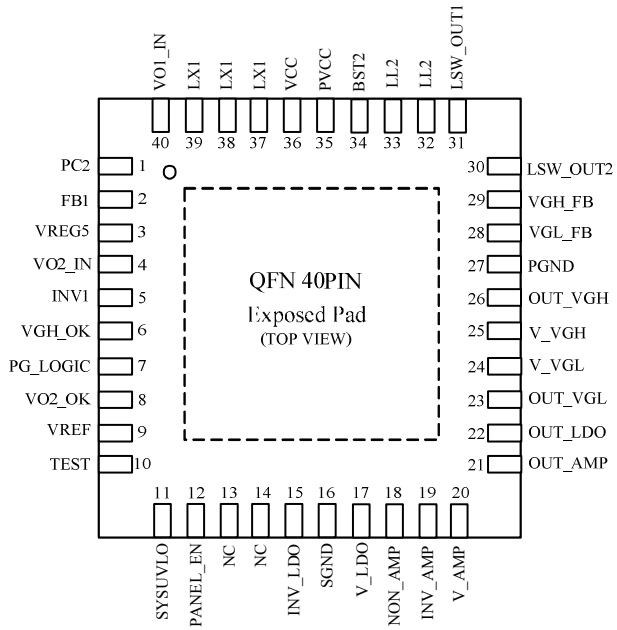
Applications

・LCD TV Bias Power Supply
・LCD Monitor Bias Power Supply

Features

・QFN40 package
・Input Voltage Range : 4.2～15V
・Boost Converter with built-in Power MOSFET
・Buck Converter with built-in Power MOSFET
  500kHz Switching Frequency
  Under Voltage Protection
  Over Voltage Protection
  Over Current Protection
・Positive/Negative Charge Pumps
・LDO
・Operational Amplifier

Pin Assignment

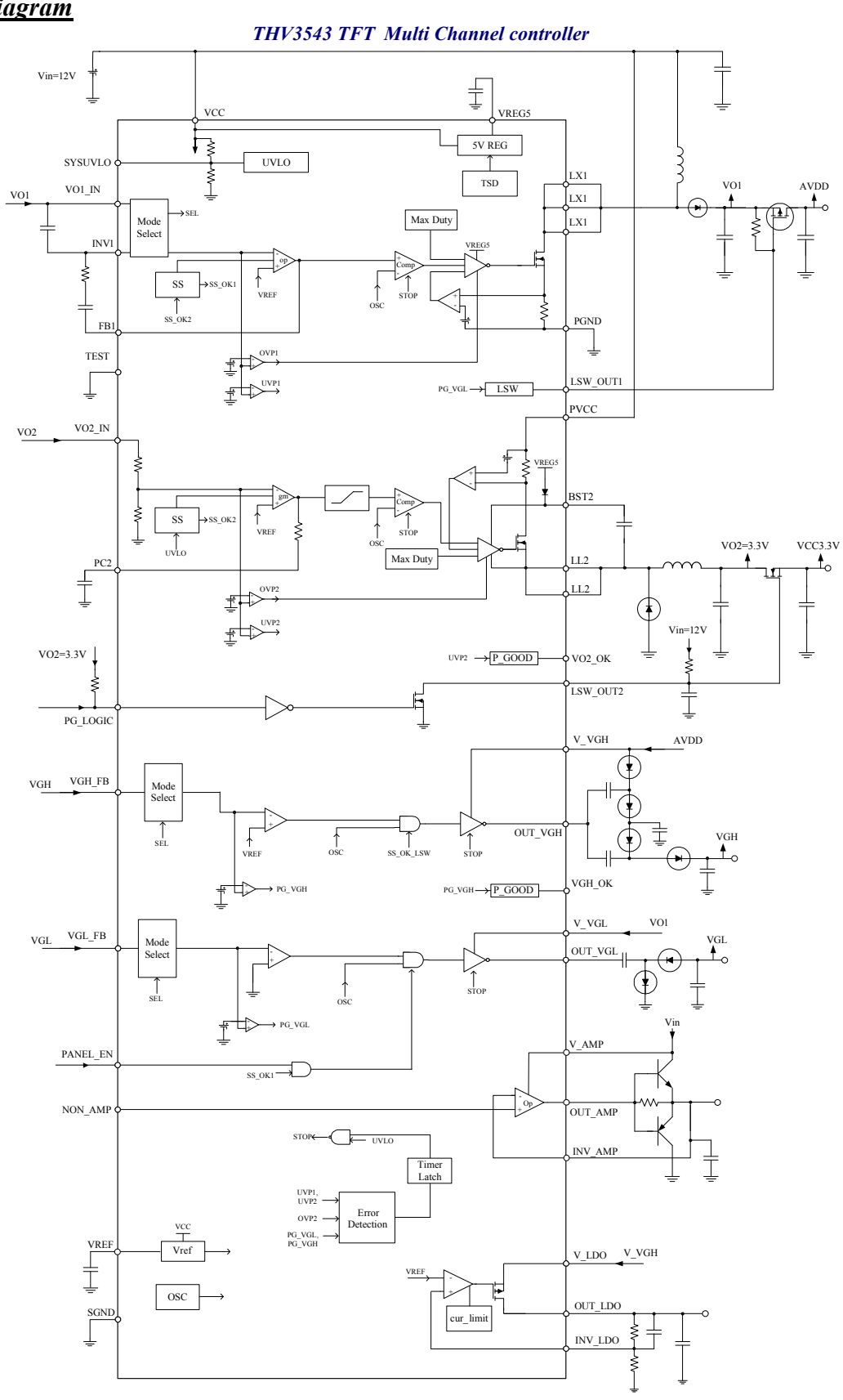


Connect the Exposed Pad to GND for enhanced thermal performance.

Output Channel Descriptions

Output Channel	Description
CH-1	PWM Boost DC/DC converter
CH-2	PWM Buck DC/DC converter
VGH	Positive voltage charge pump
VGL	Negative voltage charge pump
AMP	Operational amplifier
LDO	LDO
LSW_OUT1	Output for the external load switch 1
LSW_OUT2	Output for the external load switch 2

Block Diagram



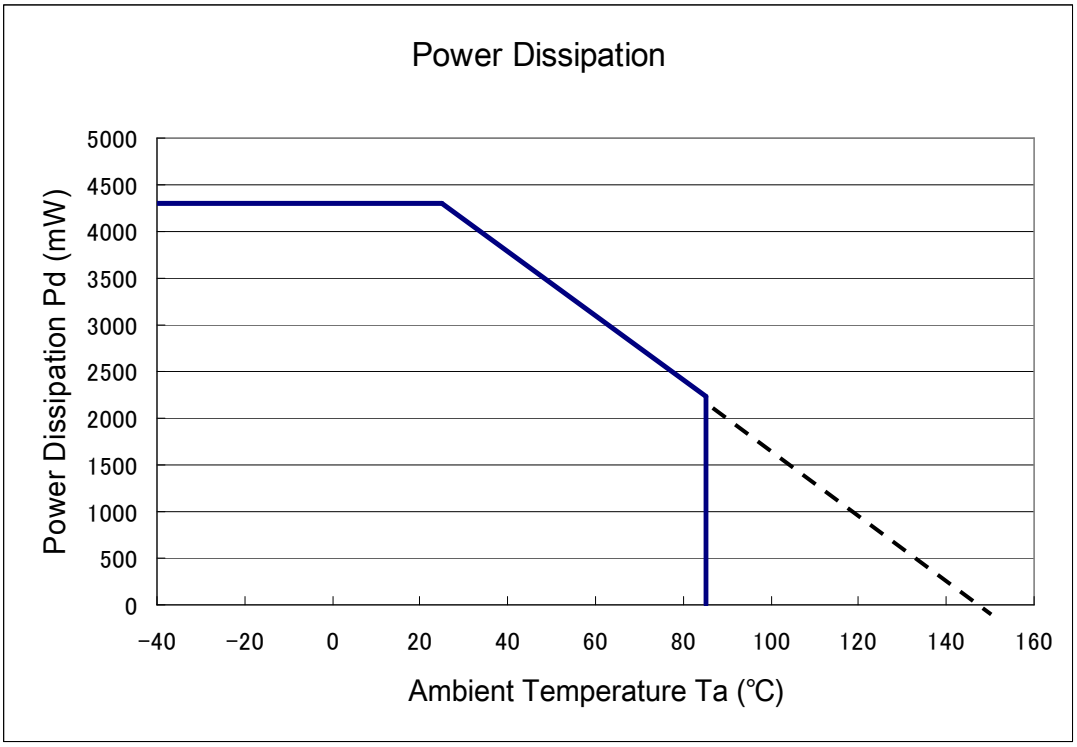
Pin Descriptions

Pin #	Symbol	Function	Description
1	PC2	Output for CH-2 error amplifier	Output pin for CH-2 error amplifier. Connect a capacitor between PC2 and GND for phase compensation.
2	FB1	Output for CH-1 error amplifier	Output pin for CH-1 error amplifier. Connect a resistor and a capacitor between FB1 pin and INV1 pin for phase compensation.
3	VREG5	Output for 5V regulator	Output pin for 5V regulator of the control circuit. Connect an external capacitor (10μF).
4	VO2_IN	Input for CH-2 feedback voltage	Feedback voltage input pin for CH-2. CH-2 is controlled so that VO2_IN pin becomes 3.3V.
5	INV1	Inverting input for CH-1 error amplifier	Inverting input for CH-1 error amplifier. In fixed output voltage mode, connect a resistor and a capacitor for phase compensation. In adjustable output voltage mode, connect resistors between the output and INV1 pin, and between INV1 pin and GND, so that this pin become 1.2V.
6	VGH_OK	VGH power good output	After positive charge pump started properly, this pin switches from Low level to High level. Connect an external pull-up resistor.
7	PG_LOGIC	Input for load switch control	Input pin for controlling LSW_OUT2.
8	VO2_OK	Output for CH-2 power good	After CH-2 started properly, this pin switches from Low level to High level. Connect an external pull-up resistor.
9	VREF	Reference voltage	1.2V reference voltage for feedback of negative voltage charge pump. Connect an external capacitor (0.01μF) for the stability.
10	TEST	Test pin	Used for the production test before shipment. Connect to GND.
11	SYSUVLO	Input for System UVLO	SYSUVLO pin shuts down the operation of IC, when the power supply voltage drops below regulated value. Resistors are internally connected between VCC pin and SYSUVLO pin, and between SYSUVLO pin and GND. It is possible to set the detection voltage at any value by connecting external resister divider to SYSUVLO pin.
12	PANEL_EN	Input for Panel power supply enable	When Low level voltage is applied to PANEL_EN pin, negative voltage charge pump, Load Switch 1 and positive voltage charge pump stop their operations. If not in use, connect to VREG5 pin.
13 14	NC	NC	No connection. Leave open.
15	INV_LDO	LDO amplifier inverting input	LDO inverting input. The voltage on this pin is 1.2V in the normal operation.
16	SGND	Ground for signal	Ground pin for the control circuit block.
17	V_LDO	Power supply for LDO	Power supply pin for LDO amplifier.

Pin #	Symbol	Function	Description
18	NON_AMP	Non-inverting input for operational amplifier	Non-inverting input pin for operational amplifier.
19	INV_AMP	Inverting input for operational amplifier	Inverting input pin for operational amplifier.
20	V_AMP	Power supply for operational amplifier	Power supply pin for operational amplifier.
21	OUT_AMP	Output for operational amplifier	Output pin for operational amplifier.
22	OUT_LDO	Output for LDO	Output pin for LDO.
23	OUT_VGL	Output for VGL driver	Output pin for the negative voltage charge pump driver.
24	V_VGL	Power supply for VGL	Power supply pin for negative voltage charge pump driver circuit.
25	V_VGH	Power supply for VGH	Power supply pin for positive voltage charge pump driver circuit.
26	OUT_VGH	Output for VGH driver	Output pin for the positive voltage charge pump driver.
27	PGND	Power Ground	Power Ground pin.
28	VGL_FB	Input for VGL feedback	Feedback voltage input for negative voltage charge pump. In fixed output voltage mode, connect this pin to the output of negative voltage charge pump. In adjustable output voltage mode, connect resistors between the output and VGL_FB pin, and between VGL_FB pin and VREF pin, so that this pin become 0V.
29	VGH_FB	Input for VGH feedback	Feedback voltage input for positive voltage charge pump. In fixed output voltage mode, connect to the output of positive voltage charge pump. In adjustable output voltage mode, connect resistors between the output and VGH_FB pin, and between VGH_FB pin and GND, so that this pin become 1.2V.
30	LSW_OUT2	Output 2 for load switch control	Gate control pin for Load Switch 2.
31	LSW_OUT1	Output 1 for load switch control	Gate control pin for Load Switch 1, with built-in Soft Start function.
32 33	LL2	Output for CH-2	Switching output pin for CH-2.
34	BST2	Power supply for CH-2 High side driver	Power supply pin for CH-2 High side driver. Connect a capacitor between BST2 pin and LL2 pin.
35	PVCC	Power supply for CH-2	Power supply pin for CH-2.
36	VCC	Power supply for control circuit	Power supply pin for the control circuit block.
37 38 39	LX1	Output for CH-1	Switching output pin for CH-1.
40	VO1_IN	Feedback voltage input for CH-1	Feedback voltage input pin for CH-1 in fixed output voltage mode. Connect to output for CH-1. In adjustable output voltage mode, connect to ground.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
VCC, PVCC	Vcc	18	V
INV1, FB1, VO2_IN, PG_LOGIC, TEST, SYSUVLO, PANEL_EN, INV_LDO, VGL_FB	VL_in	6.5	V
VREG5, PC2, VGH_OK, VO2_OK, VREF, BST2-LL2	VL_out	6.5	V
NON_AMP, INV_AMP, VO1_IN	VH_in1	20	V
VGH_FB	VH_in2	40	V
VGL_FB	VH_in3	-8	V
OUT_AMP, OUT_LDO, OUT_VGL, OUT_VGH, LSW_OUT2, LSW_OUT1	VH_out1	20	V
LL2	VH_out2	18	V
BST2	VH_out3	24.5	V
LX1	VH_out4	25	V
V_LDO, V_AMP, V_VGL, V_VGH	VH_cc	20	V
Power Dissipation	Pd	4295 (Ta<25°C)	mW
Junction Temperature	Tj	150	°C
Operating Temperature Range	Ta	-40 ~ +85	°C
Storage Temperature Range	Tstg	-55 ~ +150	°C



Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VCC, PVCC	4.2	-	15	V
VGH_OK, PG_LOGIC, VO2_OK, SYSUVLO, PANEL_EN	-0.1	-	5.5	V
V_LDO	3.0	-	17	V
V_AMP, V_VGL, V_VGH	4.2	-	17	V
NON_AMP, LSW_OUT2, LSW_OUT1	-0.1	-	17	V
External capacitor for VREF	-	0.01	-	μF
External capacitor for VREG5	-	10	-	μF

Electrical Characteristics（at Vcc=12V, Ta=25℃, unless otherwise noted.）

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Whole of Circuit						
Average Current Consumption	Icc	VCC pin	–	5.0	–	mA
Reference Voltage	Vref	Cvref=0.01μF	1.188	1.200	1.212	V
Load Regulation (Reference Voltage)	Vref(load)	Iref=-100μA ~ -1mA	–	2	5	mV
Line Regulation (Reference Voltage)	Vref(line)	Iref=-100μA VCC=4.2 ~ 15V	–	2	8	mV
Output Voltage (5V Regulator)	Vreg5(range)	Io=-1mA	–	5.0	–	V
Load Regulation (5V Regulator)	Vreg5(load)	Io=-0.1mA ~ -5mA	–	–	100	mV
Line Regulation (5V Regulator)	Vreg5(line)	Io=-1mA VCC=5.5 ~ 15V	–	–	50	mV
Oscillation Frequency	Fosc		430	500	570	kHz
UVLO Release Voltage	Vuvlo	VCC pin	5.0	5.46	6.00	V
UVLO Hysteresis Voltage	Vuvlo(hys)	VCC pin	1.4	1.96	2.5	V
System UVLO Release Voltage	Vsysuvlo	SYSUVLO pin	1.44	1.56	1.68	V
System UVLO Hysteresis Voltage	Vsysuvlo(hys)	SYSUVLO pin	0.41	0.56	0.71	V
CH-1 Boost Converter Block						
Feedback Voltage (in fixed mode)	Vo1(fix)		15.2	15.6	16.0	V
Feedback Voltage (in adjustable mode)	Vo1(adj)		Vref – 10m	Vref	Vref + 10m	V
VO1_IN Voltage Level (in fixed mode)	Vo1_in(fix)_th		4.6	–	–	V
VO1_IN Voltage Level (in adjustable mode)	Vo1_in(adj)_th		–	–	2.7	V
Output On-Resistance	Ron(ch-1)		–	100	170	mΩ
Output Off Leakage Current	Ileak(ch-1)		–	–	10	μA
Maximum Duty Cycle	Dmax(ch-1)	LX1 pin pulse	–	5	–	%
Short Circuit Detection Threshold Voltage	Vuvp(ch-1)	VO1 output voltage	–	85	–	%
Delay Time for Short Circuit Detection Latch	tuvp(ch-1)		–	12.2	–	ms
Over Voltage Detection Threshold Voltage	Vovp(ch-1)	VO1 output voltage	–	125	–	%
Over Current Detection Threshold Voltage	Ics1	VCC=12V, VO1=15.6V, VO1 output current	4.0	–	–	A
CH-2 Buck Converter Block						
Feedback Voltage	Vo2		3.23	3.30	3.37	V
Output On-Resistance	Ron(ch-2)		–	170	290	mΩ

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Off Leakage Current	Ileak(ch-2)		–	–	10	μA
Maximum Duty Cycle	Dmax(ch-2)	LL2 pin pulse	–	88	–	%
Short Circuit Detection Threshold Voltage	Vuvp(ch-2)	VO2 output voltage	–	85	–	%
Delay Time for Short Circuit Detection Latch	tuvp(ch-2)		–	12.2	–	ms
Over Voltage Detection Threshold Voltage	Vovp(ch-2)	VO2 output voltage	–	125	–	%
Delay Time for Over Voltage Detection Latch	Tovp(ch-2)		–	2.44	–	ms
Over Current Detection Threshold Voltage	Ics(ch-2)	VCC=12V, VO2 output current	3.5	–	–	A
Power Good Threshold Voltage	Vpg(ch-2)		–	85	–	%
Output On-Resistance of Power Good	Ipg(ch-2)	VO2_OK pin	–	0.8	1.6	kΩ
Output Leakage Current of Power Good	Ipgleak(ch-2)	VO2_OK=5V	–	–	2	μA
VGH Positive Charge Pump Block						
Feedback Voltage (in fixed mode)	VGH(fix)		34.5	35.6	36.7	V
Feedback Voltage (in variable mode)	VGH(adj)		Vref – 20m	Vref	Vref + 20m	V
High Side Output On-Resistance	Ronh(VGH)	V_VGH=15V Ioh=-50mA	–	3.5	–	Ω
Low Side Output On-Resistance	Ronl(VGH)	V_VGH=15V Ioh=50mA	–	3.5	–	Ω
Duty Cycle	Duty(VGH)		–	50	–	%
Short Circuit Detection Threshold Voltage	Vuvp(VGH)	VGH output voltage	–	85	–	%
Power Good Threshold Voltage	Vpg(VGH)	VGH output voltage	–	85	–	%
Output On-Resistance of Power Good	Ipg(VGH)	VGH_OK pin	–	0.8	1.6	kΩ
Output Leakage Current of Power Good	Ipgleak(VGH)	VGH_OK=5V	–	–	2	μA
VGL Negative Charge Pump Block						
Feedback Voltage (in fixed mode)	VGL(fix)		-6.19	-6.00	-5.81	V
Feedback Voltage (in variable mode)	VGL(adj)		-20	0	20	mV
High Side Output On-Resistance	Ronh(VGL)	V_VGL=15V Ioh=-50mA	–	11	–	Ω
Low Side Output On-Resistance	Ronl(VGL)	V_VGL=15V Ioh=50mA	–	5	–	Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Duty Cycle	Duty(VGL)		–	80	–	%
Short Circuit Detection Threshold Voltage	Vuvp(VGL)	VGL output voltage	–	82	–	%
VGL Start-Up Control Input Threshold Voltage	PANEL_EN (th)	PANEL_EN Voltege	0.88	1.0	1.12	V
LDO Block						
Feedback Voltage	Vldo		Vref – 20m	Vref	Vref + 20m	V
Load Regulation	Vldo(load)	V_LDO=15.6V, OUT_LDO=15.2V Ildo=-0.1m ~ -20mA	–	–	45	mV
Max Output Current	Ildo(max)	V_LDO=15.6V, OUT_LDO=15.2V	250	–	–	mA
Dropout voltage	Vdrop(ldo)	V_LDO=15.6V, OUT_LDO=15.2V Ildo=-10mA	–	–	0.15	V
Operational Amplifier Block						
Input Offset Voltage	Vamp(off)		-13	10	34	mV
Load Regulation	Vamp(load)	Iamp=0 ~ +/-5mA	-50	–	50	mV
Line Regulation	Vamp(line)	V_AMP=9V ~ 17V OUT_AMP=6V	–	–	50	mV
Common Mode Input Voltage Range	Vamp(range)		3	–	V_AMP – 0.1	V
Output Source Maximum Current	Ivcomh(max)	V_AMP=12V, OUT_AMP=6V Output drop : 0.5V	100	180	–	mA
Output Sink Maximum Current	Ivcoml(max)	V_AMP=12V, OUT_AMP=6V Output rise : 0.5V	–	-180	-100	mA
Input Bias Current	Iib(vcom)		–	–	200	nA
Switching Control Block 1						
Soft Start Time	tss(lsw_out1)		–	10	–	ms
Output Resistance	Ro(1sw_out1)	Io=1mA	–	1.2	–	kΩ
Output Off Leakage Current	Ileak		–	–	1	μA
Switching Control Block 2						
Input Threshold Voltage	V(pg_logic)		0.6	–	1.1	V
Output Resistance	Ro(1sw_out2)	Io=1mA	–	1.2	–	kΩ
Output Off Leakage Current	Ileak		–	–	1	μA

Functional Description

- **System UVLO**

THV3543 has built-in UVLO (Under Voltage Lockout) circuit to prevent low-voltage input malfunction. The internal specified threshold voltage is 3.5V, the release voltage is 5.46V. When input power supply voltage (Vin) reaches the UVLO release voltage (5.46V), the device starts the soft start operation and output voltage (Vo) gradually rises up to the regular voltage. When the input power supply voltage (Vin) drops below 3.5V, UVLO stops switching operation immediately and starts discharging soft start. Accordingly, the output voltage (Vo) drops (See Figure 1).

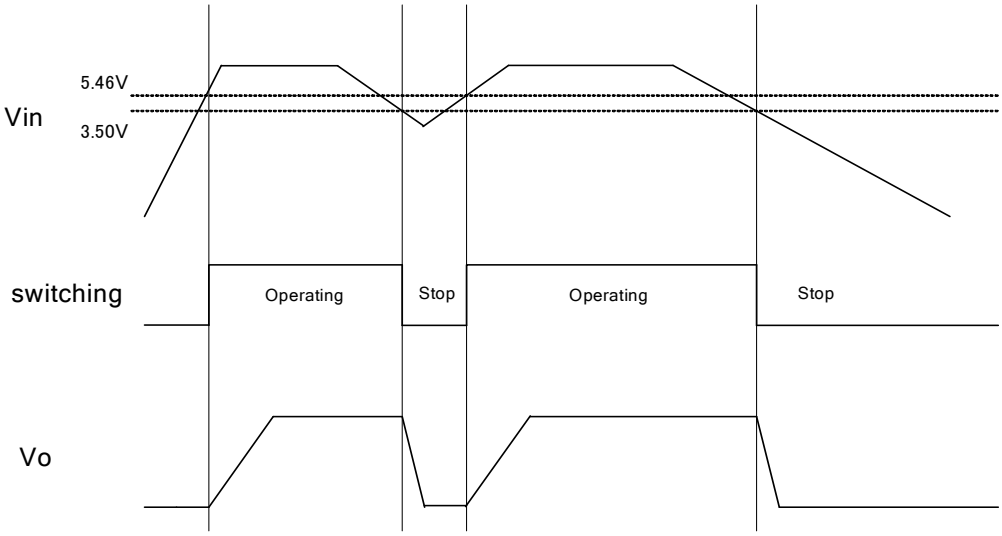


Figure 1. UVLO Operation Example

The UVLO threshold voltage also can be set optionally by applying divided Vin by an external resistance to SYSUVLO pin (See Figure 2). Please use external resistance of enough lower value than the internal resistance. The System UVLO threshold voltage is given by the following formulas.

$$\text{System UVLO Release Voltage} = 1.56 \times \frac{R1 + R2}{R2}$$

$$\text{System UVLO Detection Voltage(Lower Limit Voltage of Operation)} = 1.0 \times \frac{R1 + R2}{R2}$$

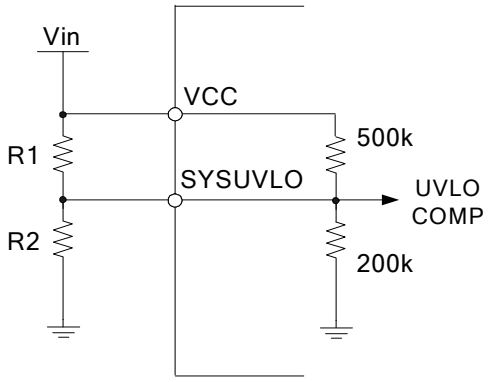


Figure 2. System UVLO Setting Circuit

- **Voltage Reference Circuit**

Voltage reference circuit generates temperature-compensated voltage (1.2V) which is used as the internal reference voltage. Also an external load current (up to 1mA, maximum) can be obtained from VREF pin. Please connect a capacitor (0.01μF) between VREF pin and SGND for stability.

- **VREG5**

VREG5 is Built-in 5V local regulator. Please connect an external capacitor (10μF) between VREG5 pin and SGND.

- **Oscillator Circuit**

Oscillation frequency is internally fixed at 500kHz.

- **Thermal Shut Down (TSD)**

Thermal Shut Down circuit is built in to prevent damages caused by excessive heat. When the junction temperature reaches 175 °C, TSD circuit stops switching operation and the regulator VREG5 operation. The release temperature is 160°C.

- **DC/DC Converter CH-1, CH-2**

CH-1 and CH-2 are PWM controllers. CH-1 is for Boost, CH-2 is fixed at 3.3V for Buck. Power MOSFET and Over Current Detection Circuit are built in. Maximum Duty Cycle ratio of CH-1 LX1 pin is 8.3%, CH-2 LL2 pin is 88%.

- **Charge Pump Circuit VGH, VGL**

VGH is positive charge pump, and VGL is negative. VGH and VGL also can operate in PFM mode. The duty cycle ratio of VGH is fixed at 50%, VGL is fixed at 80%.

- **VO2_OK, VGH_OK**

VO2_OK and VGH_OK are open drain output of the pull-down transistor. When the power supply is turned on, the transistor is turned on pulling VO2_OK pin and VGH_OK pin to ground level. When each voltage on CH-2 and VGH reaches 85% of normal output voltage, VO2_OK and VGH_OK are turned off respectively.

- **Load Switch Control**

LSW_OUT1 pin controls the external P-CH MOSFET load switch after normal start-up of VGL. Soft start function is built in.

LSW_OUT2 pin is open drain output. When PG_LOGIC pin is turned High level, pull-down transistor is turned off. LSW_OUT2 pin can be used as the external N-CH MOSFET load switch controller or level shifter.

- **Operational Amplifier**

Operational amplifier is used for Vcom or Half AVDD. Use an external bipolar transistor when large output current is required.

- **LDO**

LDO have built-in recovery type current limiting protection. The load current capacity is within 250mA. The output voltage is set by external resistance (See “Output Voltage Setting (LDO)”).

- **Soft Start Circuit**

Soft start function raises the output voltage gradually to prevent overshoot and inrush current at start-up. CH-1, CH-2 and Load Switch 1 circuit have internal soft start function. The output voltage of these internal soft start circuits rise according to each internal start-up sequences. Accordingly, the output of DC/DC converter and the output after load switch rise. Soft start operation is completed when these outputs have reached each regular voltage. Soft start time of CH-1, CH-2 and Load Switch 1 are set to 10msec (See Figure 3).

- **Start-up Sequence**

Figure 3 shows the waveform of start-up sequence. The device starts switching after normal start-up of CH-1 and CH-2. VGL starts after normal start-up of CH-1 output (VO1) and also when PANEL_EN pin is turned High level. VGH starts with 5msec delay after start-up of Load Switch 1. Open drain pins, VO2_OK and VGH_OK, start after normal start-up of CH-2 and VGH respectively.

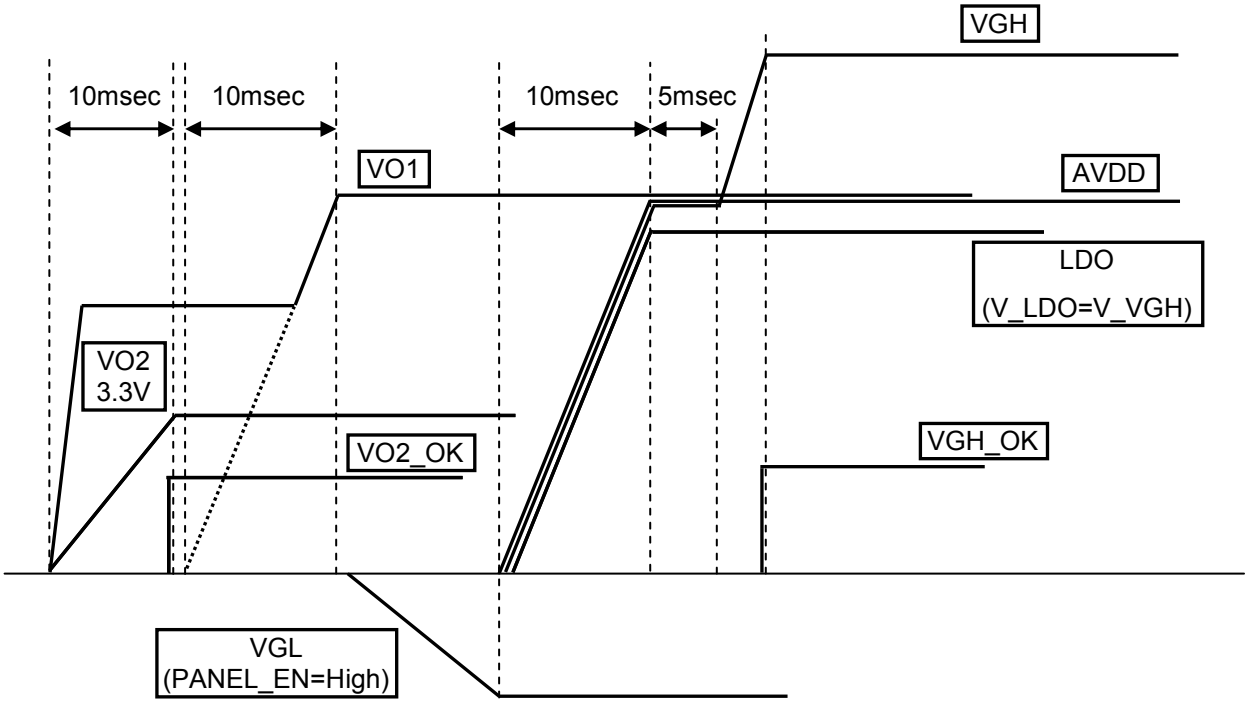


Figure 3. Start-up Sequence Waveforms

- **PANEL_EN**

During the start-up operation of IC, VGL starts after normal start-up of CH-1 output (VO1) and also when PANEL_EN pin is turned High level. If Low level voltage is applied to PANEL_EN pin, VGL/Load Switch 1/VGH stop operating. High level voltage is applied to VGL_ON pin again, operations after VGL are restarted.

If not in use, please connect to VREG5 pin.

- **Under Voltage Protection (UVP)**

UVP is protective function which shuts down the power supply, when under voltage condition of DC/DC, VGH and VGL caused by short circuit continues for more than a definite period of time. The internal comparator monitors the output voltage. If the output voltage drops below a definite value, timer latch circuit starts operating (See Figure 4). When abnormal output continues for more than 12.2msec, the device stops switching operation and goes into latch state. If UVLO operates before the device goes into the latch state, the timer will be reset.

As to VGH and VGL, UVP detection does not operate for 3msec immediately after start-up sequence. Please set the start-up time of charge pumps within 15msec to prevent start-up failure.

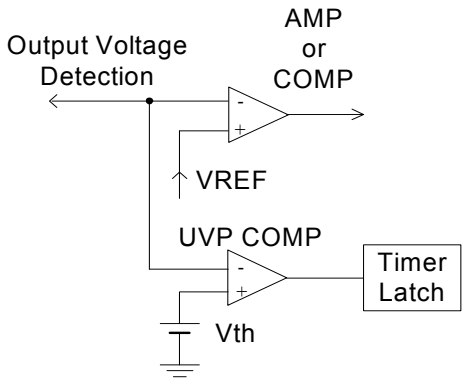


Figure 4. Under Voltage Detection Circuit

- **Over Voltage Protection (OVP)**

OVP is protective function which shuts down the power supply when output voltage on CH-1 and CH-2 exceed a defined voltage. CH-1 stops switching operation, when the voltage on INV1 pin exceeds 1.5V. CH-2 stops switching operation, when the voltage on VO2_IN pin exceeds 4.13V (See Figure 5) .

As to CH-2, if abnormal output is detected, timer latch circuit operates. When abnormal output continues for 2.44msec, the device stops switching operation and goes into latch state.

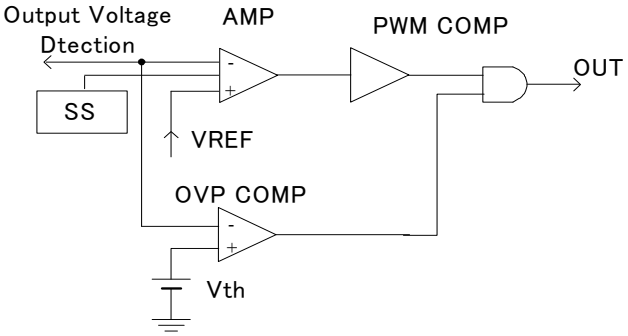


Figure 5. Over Voltage Detection Circuit

- **Over Current Protection (OCP)**

CH-1 and CH-2 have built-in over current protection circuit. When load current exceeds a definite current, OCP stops switching operation of the device. OCP operates at more than 4.0A on CH-1, 3.5A on CH-2.

If over current is detected continuously, low duty switching pulse is generated and that causes output voltage drop. When output voltage drops below a definite voltage for more than 12.2msec, UVP operates and the device goes into latch state.

- **Switching Channel Output Voltage Mode**

Output voltage mode of switching channel can be chosen the adjustable mode or the fixed mode, according to the setting of VO1_IN pin.

When CH-1 output is connected directly to VO1_IN pin, the output voltage is turned into the fixed mode. CH-1 is fixed at 15.6V, VGH at 35.6V and VGL at -6V. When VO1_IN pin is connected to ground, the output voltage is turned into the adjustable mode. Output voltage of CH-1, VGH and VGL can be set by an external resistance. CH-2 is fixed at 3.3V in both modes.

- **Output Voltage Setting (Adjustable Mode)**

In CH-1, the voltage on INV1 pin will be equal to the voltage on VREF by the action of feedback (See Figure 6). The voltage on INV1 pin is divided Vout1 by R1 and R2.

Therefore,

$$\text{Vout1} \times \frac{\text{R2}}{\text{R1}+\text{R2}} = \text{VREF}$$

Thus,

$$\text{Vout1} = \text{VREF} \times \left(1+\frac{\text{R1}}{\text{R2}}\right) = 1.2 \times \left(1+\frac{\text{R1}}{\text{R2}}\right)$$

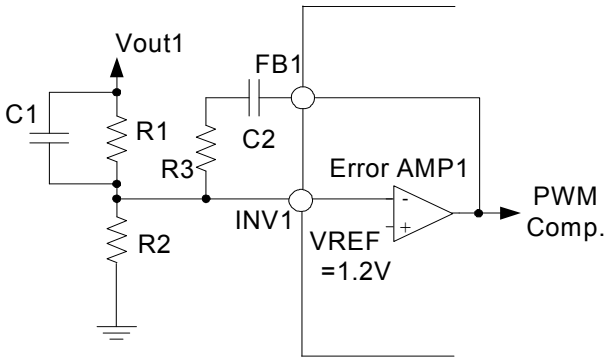


Figure 6. CH-1 Output Voltage Setting

In VGH, the voltage on VGH_FB pin is controlled to be equal to the voltage on VREF (See Figure 7). The voltage on INV_VGH pin is divided voltage on VGH by R4 and R5.

Therefore,

$$\text{VGH} = \text{VREF} \times \left(1+\frac{\text{R4}}{\text{R5}}\right) = 1.2 \times \left(1+\frac{\text{R4}}{\text{R5}}\right)$$

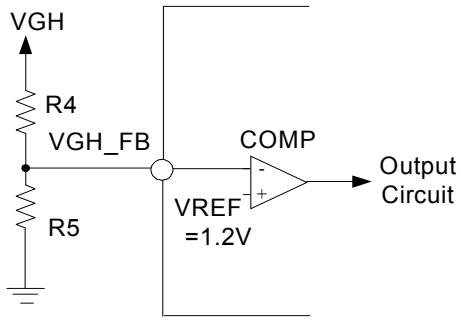


Figure 7. VGH Output Voltage Setting

In VGL, the voltage on VGL_FB pin is controlled to be equal to zero (See Figure 8). The current through VGL_FB pin can be ignored.

Thus,

$$VGL = -(VREF) \times \frac{R6}{R7} = -1.2 \times \frac{R6}{R7}$$

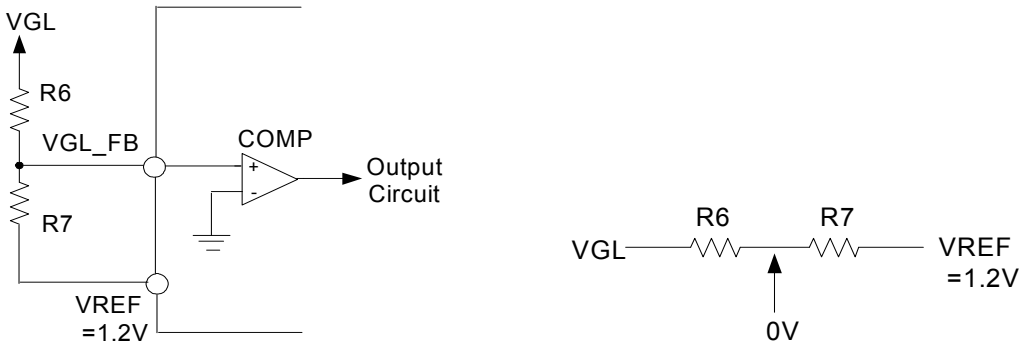


Figure 8. VGL Output Voltage Setting

- **Output Voltage Setting (Fixed Mode)**

When the output of CH-1 is connected directly to VO1-IN pin, the output voltage is in the fixed mode. Connect the output of VGH and VGL directly to VGH_FB pin and VGL_FB pin respectively. CH-1, VGH and VHL are fixed at 15.6V, 35.6V and -6V respectively.

In CH-1, connect a capacitor for phase compensation between VO1_IN pin and INV1 pin, and also a resistance and a capacitor between INV1 pin and FB1 pin (See Figure 9).

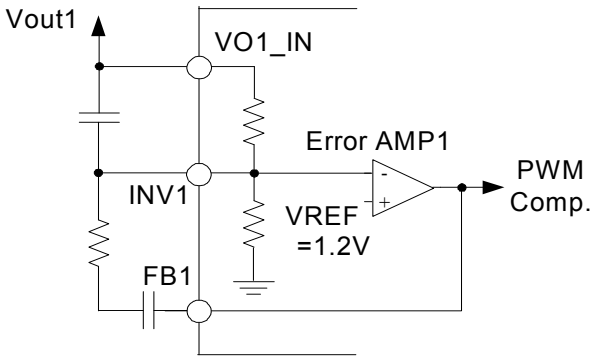


Figure 9. CH-1 Circuit in Fixed Output Voltage Mode

- **Output Voltage Setting (LDO)**

In LDO, the voltage on INV_LDO pin will be equal to the voltage on VREF by the action of feedback (See Figure 10). The voltage on INV_LDO pin is divided OUT_LDO by R8 and R9.

Thus,

$$OUT\_LDO = 1.2 \times \left(1 + \frac{R8}{R9}\right)$$

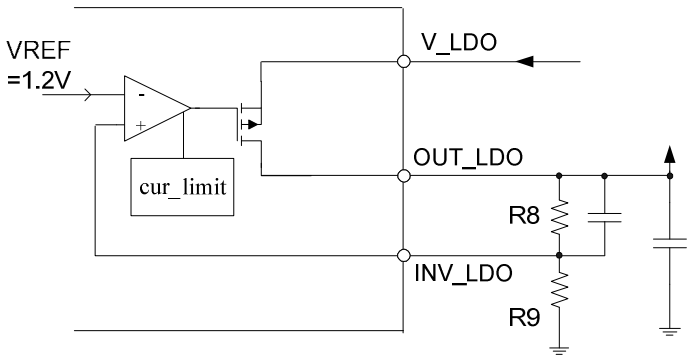
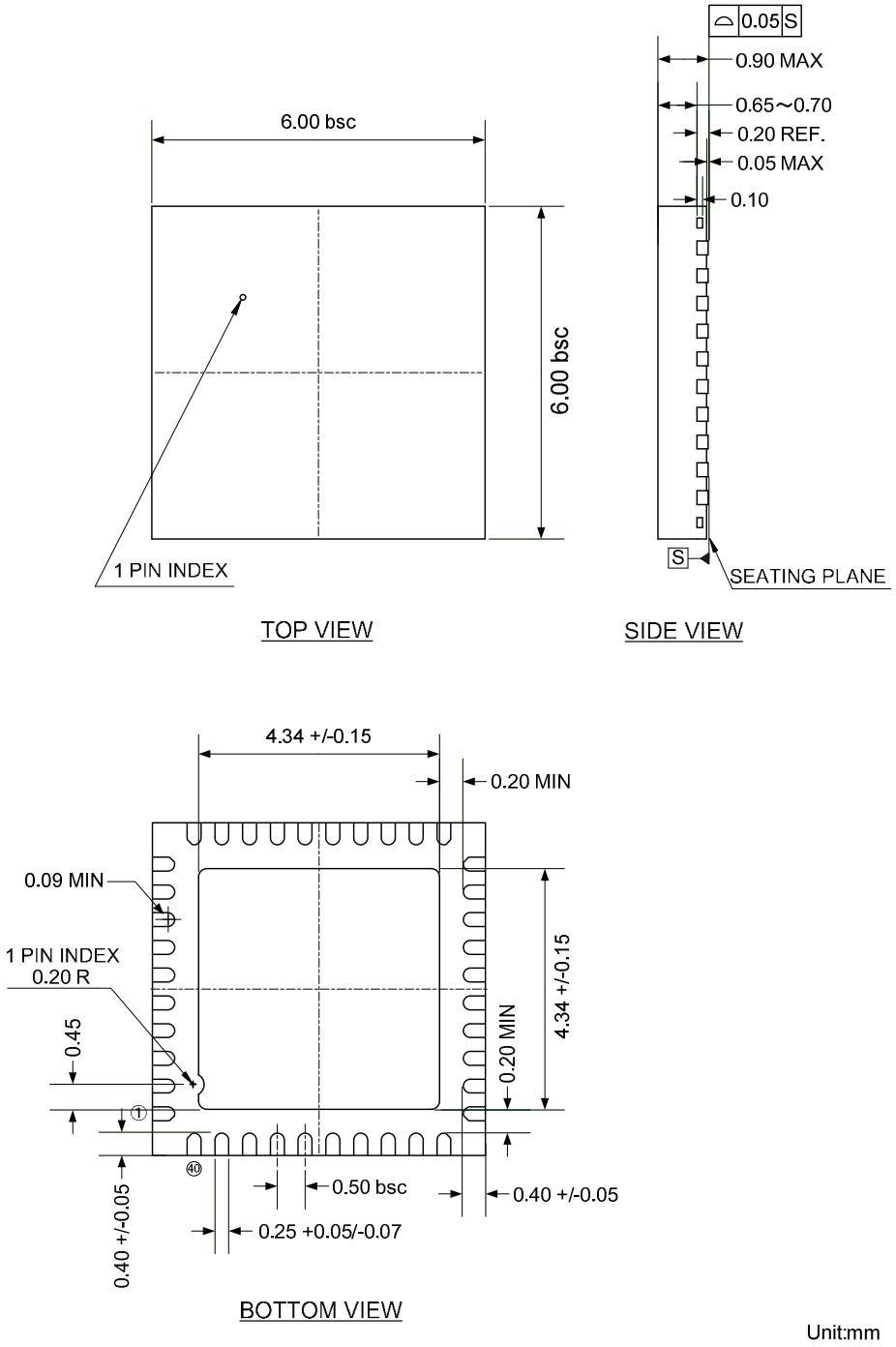


Figure 10. LDO Circuit

Package Dimensions

QFN40 pin



Connect the Exposed Pad to GND for enhanced thermal performance.

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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THine Electronics, Inc.

E-mail: sales@thine.co.jp