

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x3-8PP saves board space
- Fast switching speed
- High performance trench technology

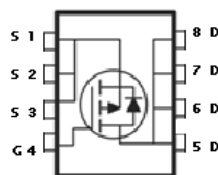
APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

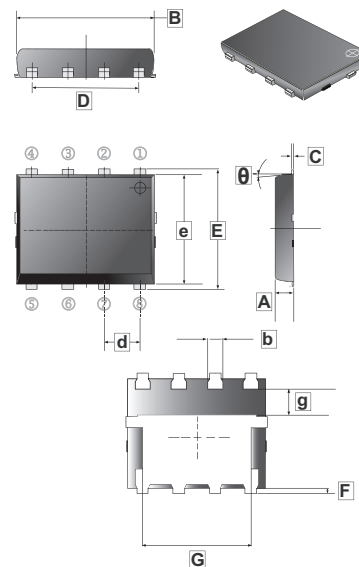
PACKAGE INFORMATION

Package	MPQ	Leader Size
DFN3x3-8PP	3K	13 inch

Top View



DFN3x3-8PP



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	0.70	0.90	θ	0°	12°
B	3.00BSC		b	0.20	0.40
C	0.10	0.25	d	0.65BSC	
D	1.80	2.3	e	3.00BSC	
E	3.2BSC		g	0.70(TYP.)	
F	0.01	0.02			
G	2.35BSC				

MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ¹	I_D	$T_A=25^\circ\text{C}$	-13
		$T_A=70^\circ\text{C}$	-11
Pulsed Drain Current ²	I_{DM}	-50	A
Continuous Source Current (Diode Conduction) ¹	I_S	-2.1	A
Total Power Dissipation ¹	P_D	$T_A=25^\circ\text{C}$	3.5
		$T_A=70^\circ\text{C}$	2.0
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient (Max.) ¹	$R_{\theta JA}$	$t \leq 5 \text{ sec}$	35
		Steady State	81

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$
Gate-Body Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{DS}=0$, $V_{GS} = \pm 8\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -16\text{V}$, $V_{GS}=0$
		-	-	-5		$V_{DS} = -16\text{V}$, $V_{GS}=0$, $T_J=55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	-50	-	-	A	$V_{DS} = -5\text{V}$, $V_{GS} = -10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	14	m Ω	$V_{GS} = -4.5\text{V}$, $I_D = -11.5\text{A}$
		-	-	19		$V_{GS} = -2.5\text{V}$, $I_D = -9.3\text{A}$
Forward Transconductance ¹	g_{fs}	-	29	-	S	$V_{DS} = -15\text{V}$, $I_D = -11.5\text{A}$
Diode Forward Voltage	V_{SD}	-	-0.8	-	V	$I_S=2.5\text{A}$, $V_{GS}=0$
Dynamic ²						
Total Gate Charge	Q_g	-	25	-	nC	$V_{DS} = -15\text{V}$, $V_{GS} = -4.5\text{V}$, $I_D = -11.5\text{A}$
Gate-Source Charge	Q_{gs}	-	11	-		
Gate-Drain Charge	Q_{gd}	-	17	-		
Input Capacitance	C_{iss}	-	2300	-	pF	$V_{DS} = -15\text{V}$, $V_{GS}=0$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	600	-		
Reverse Transfer Capacitance	C_{rss}	-	300	-		
Turn-On Delay Time	$T_{d(on)}$	-	15	-	nS	$V_{DD} = -15\text{V}$ $I_D = -1\text{A}$ $V_{GEN} = -10\text{V}$ $R_L=6\Omega$
Rise Time	T_r	-	13	-		
Turn-Off Delay Time	$T_{d(off)}$	-	100	-		
Fall Time	T_f	-	54	-		

Notes:

- Pulse test : $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

CHARACTERISTIC CURVE

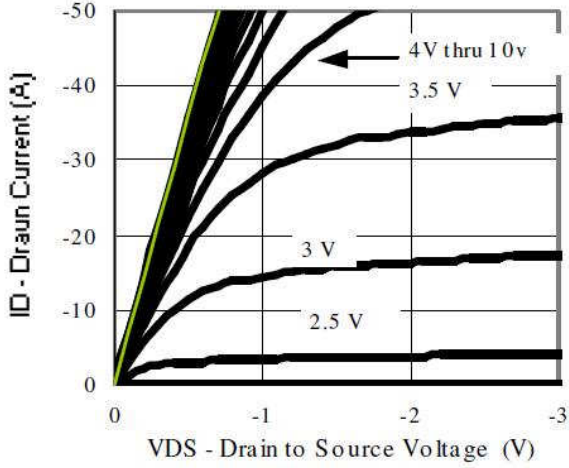


Figure 1. On-Region Characteristics

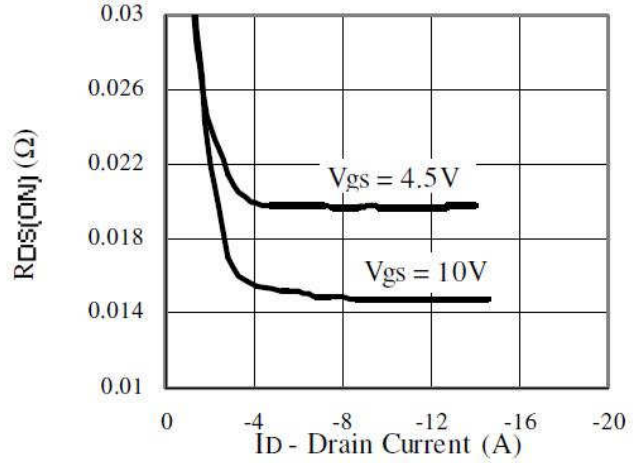


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

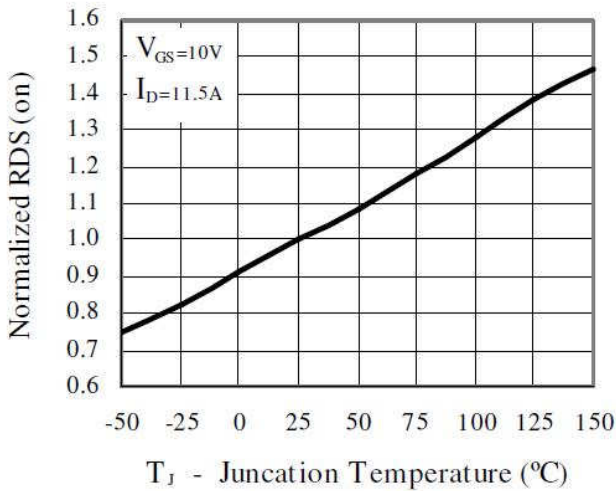


Figure 3. On-Resistance Variation with Temperature

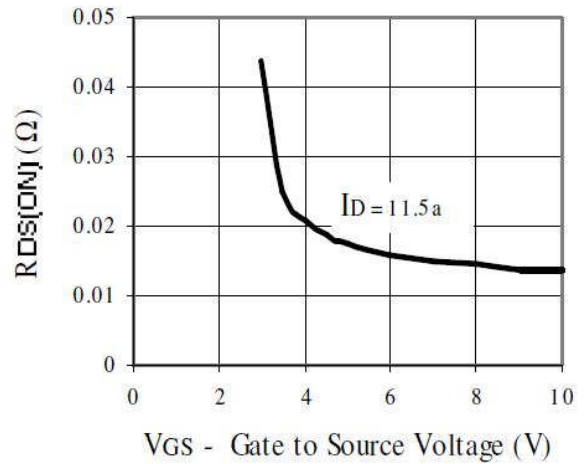


Figure 4. On-Resistance with Gate to Source Voltage

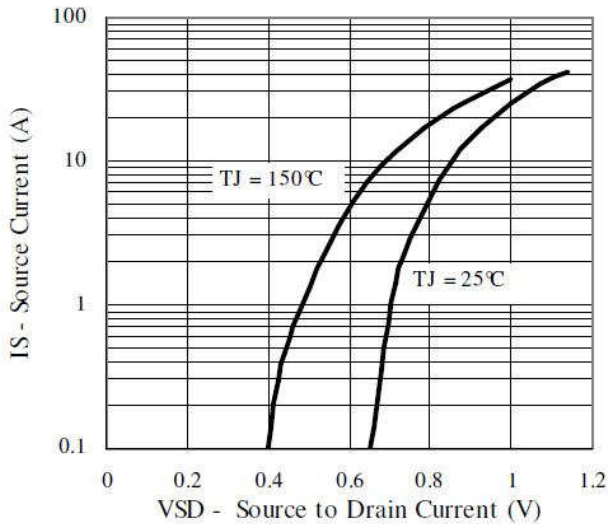


Figure 5. Transfer Characteristics

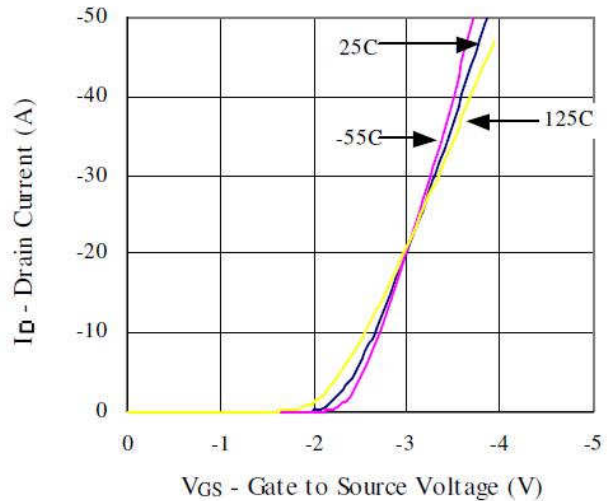


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

CHARACTERISTIC CURVE

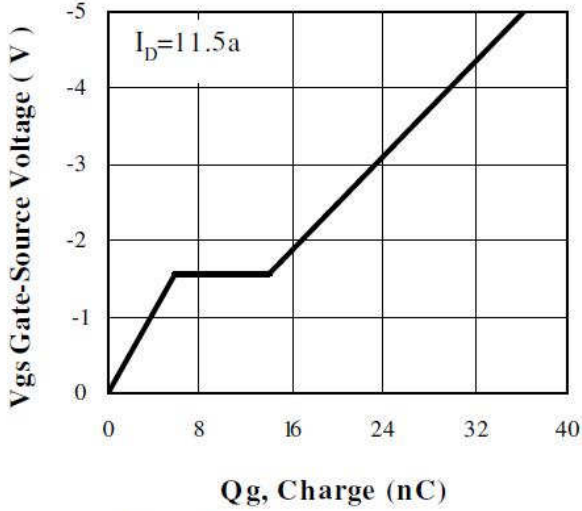


Figure 7. Gate Charge Characteristics

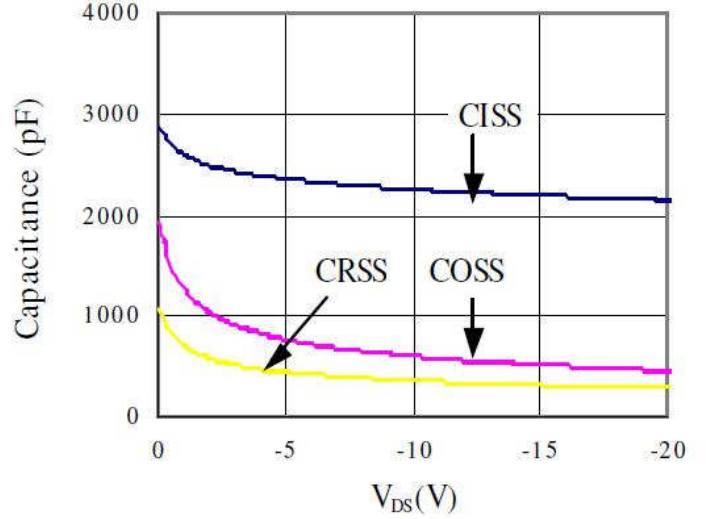


Figure 8. Capacitance Characteristics

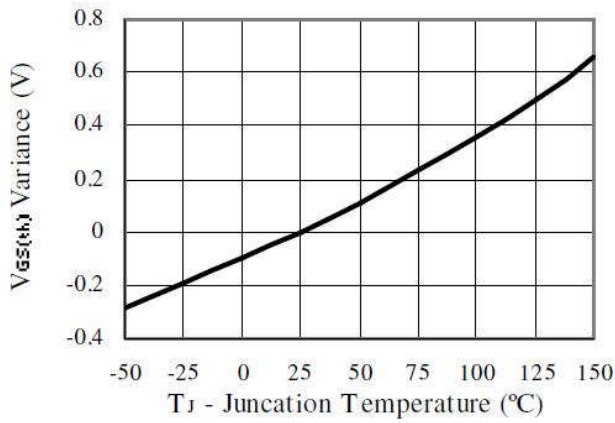


Figure 9. Maximum Safe Operating Area

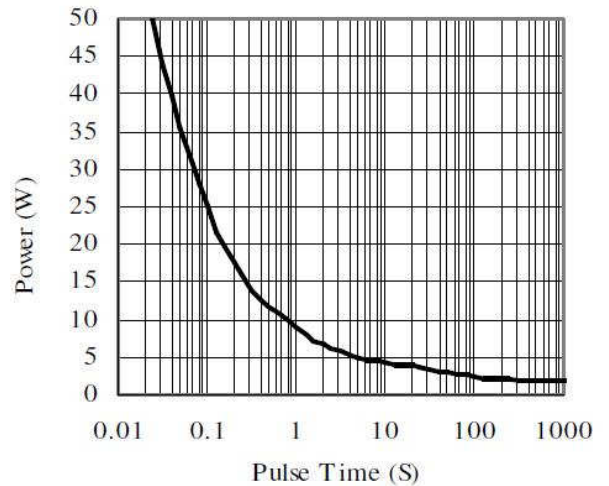


Figure 10. Single Pulse Maximum Power Dissipation

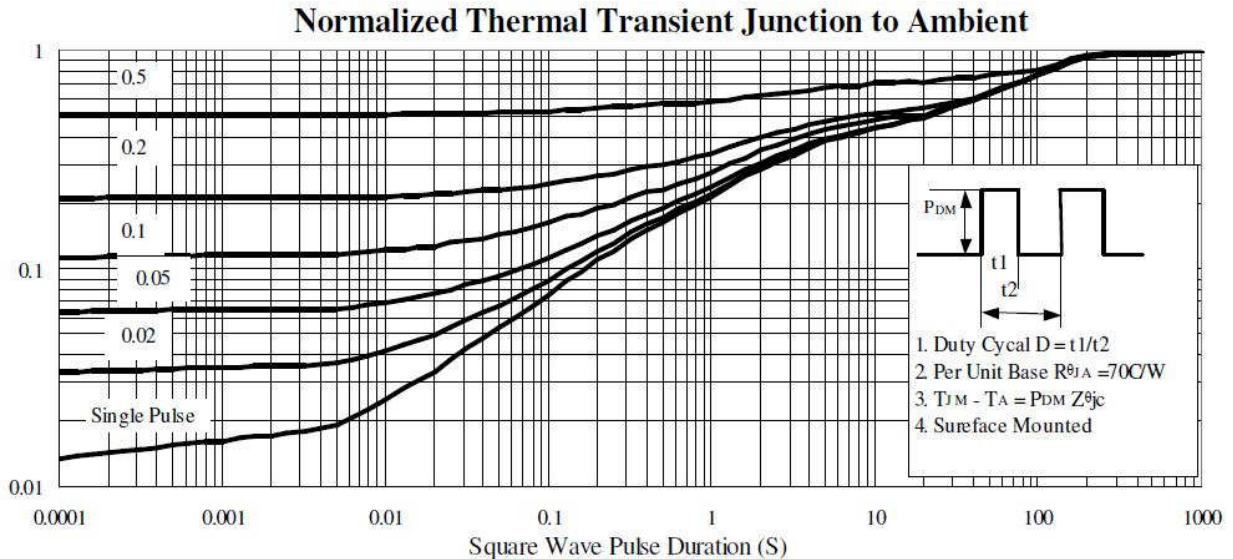


Figure 11. Transient Thermal Response Curve