SAA8200HL

Ensation Base integrated wireless audio baseband

Rev. 02 — 17 October 2005 Preliminary data sheet

1. General description

The Ensation Base, SAA8200HL, is part of the integrated wireless audio system chip set offered by Philips. This chip set enables the development of low cost wireless digital audio systems. The chip set contains:

- An integrated wireless audio baseband chip (SAA8200HL)
- An integrated wireless audio radio chip (TEA7000).

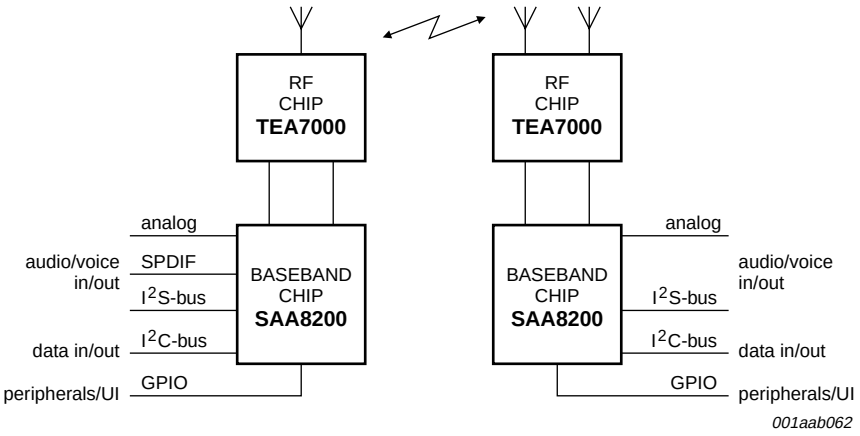


Fig 1. Ensation Link system example using two integrated wireless audio baseband and radio ICs

Integrating a wireless audio link in a home theatre system to remove part of the wiring is a logical application of wireless audio transmission. A very important property of this wireless audio system is the low end-to-end (audio-in at transmit side to audio-out at receive side) system latency, which is below 20 ms.

A second important property is the robustness and reliability of the wireless audio link, the SAA8200HL which is handling the signal processing and the system control enables this.

Furthermore, the SAA8200HL provides the flexibility to allow designers to make trade-offs between air bit-rate, number of transported audio channels, audio formats, audio coding bit-rates, range, number of receiving-slaves and more.

Due to its low power consuming design, the SAA8200HL enables battery powered applications. The SAA8200HL does this all with a minimum of external components due to its high level of integration.

Together with the TEA7000, the SAA8200HL can be used to implement an indoor wireless link for audio applications (system specific). Together with an AV-compliant Bluetooth radio module, the SAA8200HL can be used to implement a Bluetooth wireless audio functionality.

The SAA8200HL enables a low power, low cost two-chip solution with a maximum amount of functions integrated on the SAA8200HL, taking into account strict time-to-market constraints.

2. Features

2.1 General

- Programmable baseband processor and system controller for cable replacement wireless audio
- Supports various audio compression formats
- Wireless audio protocol can make trade-off between quality, number of channels, bandwidth and range
- Supports various transmission frequencies
- High integration allows for two-chip applications
- Embedded ROM with wireless audio software library.

2.2 Hardware

- Audio PLL and system PLL
- Read-Solomon encoder and decoder
- SPDIF interface
- Low cost low power EPICS7B DSP core with hardware debugger and JTAG interface
- Integrated memories:
  - 24/6 kWords program ROM/RAM (bit width: 32 bits)
  - 12 kWords X data RAM (bit width: 24 bits)
  - 12/2 kWords Y data ROM/RAM (bit width: 12 bits).
- Interrupt controller
- DMA controller
- Oscillator and time base unit with programmable clocks
- Embedded LDO regulators and DC-to-DC converters for on-chip and off-chip supply voltage needs
- Power control unit
- Power on and power off switching with battery supply
- Reed-Solomon codec unit
- Serial radio interface unit
- High speed UART
- General purpose digital I/O block with 14 inputs, all of which generate interrupts
- I^2C-bus master/slave
- I^2C-bus for radio chip control
- Control 10-bit ADC with four inputs

- Two serial (I^2S-bus/Japanese) digital audio inputs with independent clocks and word-select
- Two serial (I^2S-bus/Japanese) digital audio outputs with shared clock and word-select
- Integrated 16-bit stereo DAC (line output)
- Integrated stereo headphone amplifier
- Programmable Gain Amplifier (PGA) (line input)
- Low noise microphone amplifier (microphone input)
- Integrated 16-bit stereo ADC
- Watchdog timer.

2.3 Software

- Stereo Sub Band Coding (SBC) encoder/decoder
- Stereo MPEG layer 3 (MP3) decoder
- Reed-Solomon encoder/decoder driver
- Sample rate converter
- I^2C-bus master/slave driver
- Serial radio interface driver
- RF radio chip driver
- UART driver
- Control 10-bit ADC driver
- Power consumption management
- ADC, DAC and headphone driver
- Wireless audio protocol library.

3. Applications

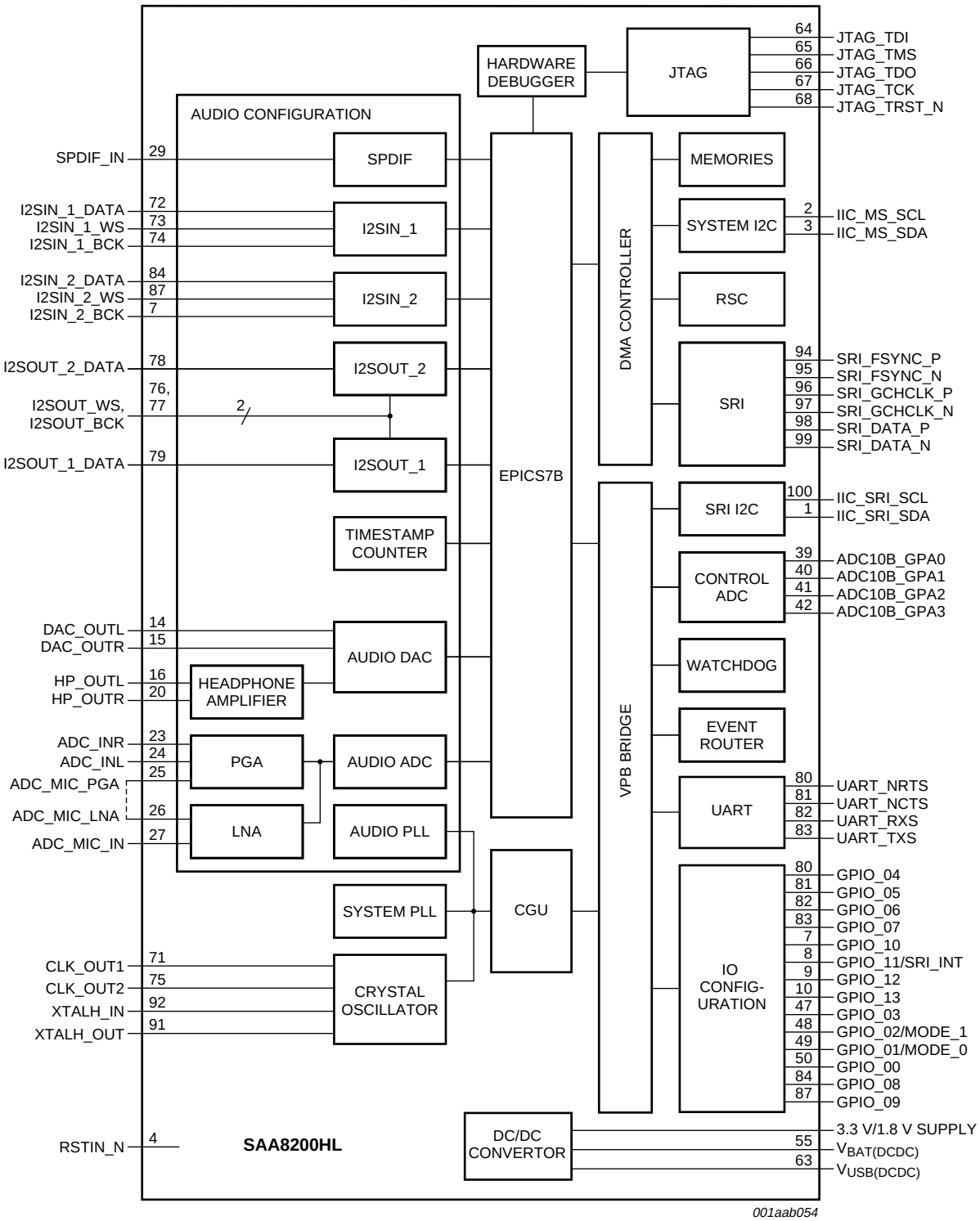
- Wireless front speakers or wireless surround speakers for home theatre
- Wireless indoor headphones
- Wireless second room audio sets
- Wireless headsets.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
SAA8200HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5. Block diagram



Pins 7, 80 to 84 and 87 are multiplexed functions pins.

Fig 2. Block diagram

6. Pinning information

6.1 Pinning

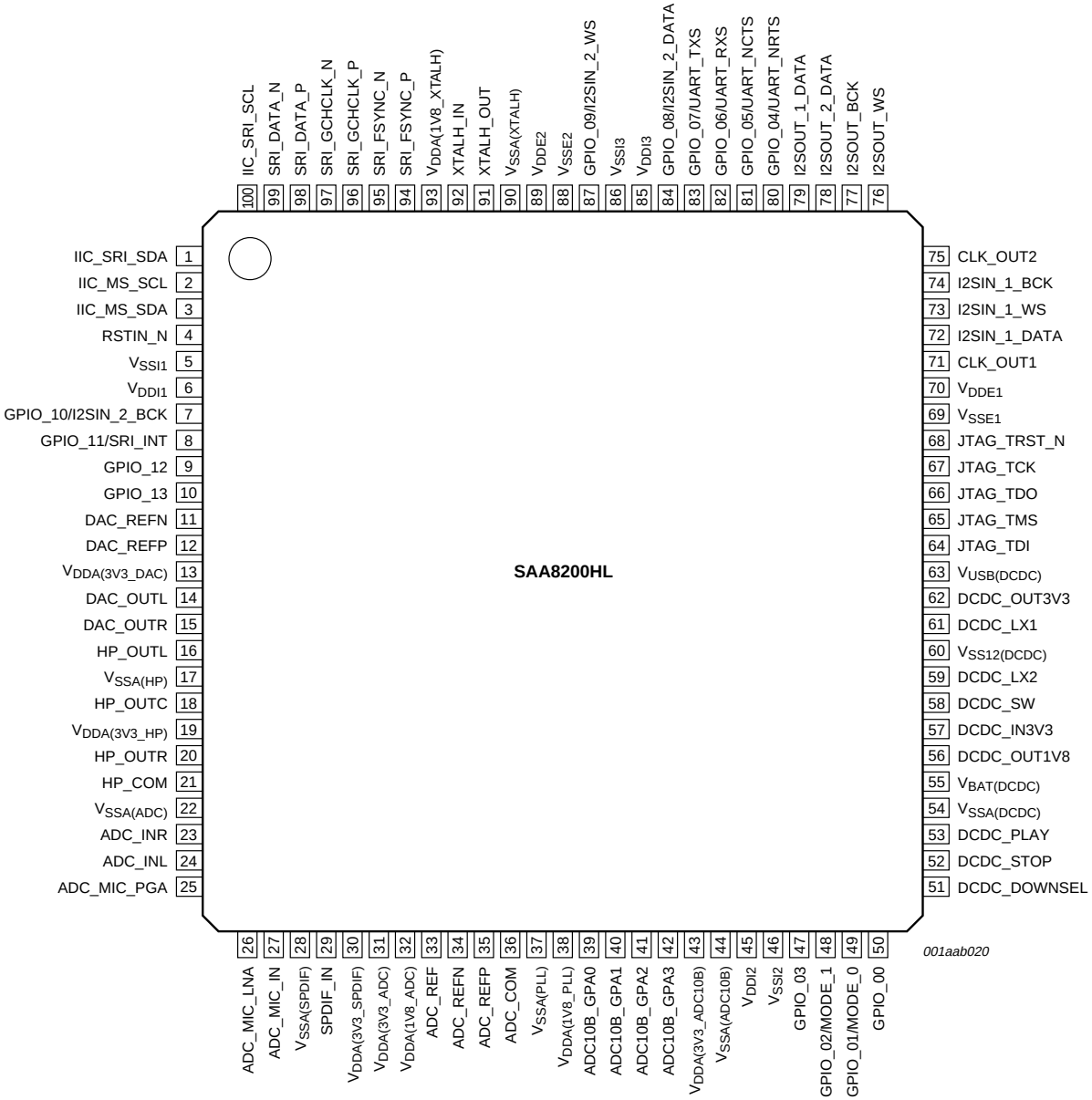


Fig 3. Pin configuration

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Special [1]	Type	Description
Digital supply voltage pins				
V_{SSI1}	5		VSSI	core ground
V_{DDI1}	6		VDDI	core supply voltage
V_{SSE1}	69		VSSE3V3	core ground
V_{DDE1}	70		VDDE3V3	core supply voltage
V_{SSE2}	88		VSSE3V3	core ground
V_{DDE2}	89		VDDE3V3	core supply voltage
V_{DDI2}	45		VDDCO	core supply voltage
V_{SSI2}	46		VSSCO	core ground
V_{DDI3}	85		VDDCO	core supply voltage
V_{SSI3}	86		VSSCO	core ground
DC-to-DC converter				
$V_{USB(DCDC)}$	63	A	VDDCO	USB supply voltage (linear regulator)
DCDC_OUT3V3	62	A	VDDCO	3.3 V output voltage
DCDC_LX1	61	A	VDDCO	coil connection for 3.3 V converter
$V_{SSI2(DCDC)}$	60	A	VSSCO	ground for switches 1.8 V and 3.3 V converter
DCDC_LX2	59	A	VDDCO	coil connection for 1.8 V converter
DCDC_SW	58	A	VDDCO	switch node
DCDC_IN3V3	57	A	VDDCO	3.3 V input voltage
DCDC_OUT1V8	56	A	VDDCO	1.8 V output voltage
$V_{BAT(DCDC)}$	55	A	VDDCO	battery supply voltage
$V_{SSA(DCDC)}$	54	A	VSSCO	ground double bonded clean and substrate
DCDC_PLAY	53	A	APIO	play button signal
DCDC_STOP	52	A	APIO	stop button signal
DCDC_DOWNSEL	51	A	APIO	one ore two battery selection
Crystal oscillator				
$V_{SSA(XTALH)}$	90		VSSCO	analog ground
XTALH_OUT	91		APIO	11.025 MHz clock output
XTALH_IN	92		APIO	11.025 MHz clock input
$V_{DDA(1V8\_XTALH)}$	93		VDDCO	analog supply voltage
PLL				
$V_{DDA(1V8\_PLL)}$	38		VDDCO	analog supply voltage
$V_{SSA(PLL)}$	37		VSSCO	analog ground
Serial radio interface				
SRI_FSYNC_P	94	A	APIO	frame sync positive
SRI_FSYNC_N	95	A	APIO	frame sync negative
SRI_GCHCLK_P	96	A	APIO	gated channel clock positive

Table 2: Pin description *...continued*

Symbol	Pin	Special [1]	Type	Description
SRI_GCHCLK_N	97	A	APIO	gated channel clock negative
SRI_DATA_P	98	A	APIO	data positive
SRI_DATA_N	99	A	APIO	data negative
Serial radio interface I^2C-bus				
IIC_SRI_SCL	100		IIC400KT5V	clock input
IIC_SRI_SDA	1		IIC400KT5V	data input or output
Audio ADC				
ADC_COM	36	A	APIO	common mode reference voltage
ADC_REFP	35	A	APIO	positive reference voltage
ADC_REFN	34	A	APIO	negative reference voltage
ADC_REF	33	A	APIO	reference voltage
$V_{DDA(3V3\_ADC)}$	31	A	VDDCO	analog supply voltage (3.3 V)
$V_{DDA(1V8\_ADC)}$	32	A	VDDCO	analog supply voltage (1.8 V)
$V_{SSA(ADC)}$	22	A	VSSCO	analog ground
ADC_INR	23	A	APIO	right input voltage
ADC_INL	24	A	APIO	left input voltage
ADC_MIC_PGA	25	A	APIO	PGA input for AC coupling
ADC_MIC_LNA	26	A	APIO	LNA output for AC coupling
ADC_MIC_IN	27	A	APIO	microphone input
Audio DAC				
DAC_REFN	11	A	APIO	negative reference voltage
DAC_REFP	12	A	APIO	positive reference voltage
$V_{DDA(3V3\_DAC)}$	13	A	VDDCO	analog supply voltage
DAC_OUTL	14	A	APIO	left line output voltage
DAC_OUTR	15	A	APIO	right line output voltage
Headphone				
HP_COM	21	A	APIO	common mode reference voltage
HP_OUTR	20	A	APIO	right output voltage
$V_{DDA(3V3\_HP)}$	19	A	VDDCO	analog supply voltage
HP_OUTC	18	A	APIO	common output voltage
$V_{SSA(HP)}$	17	A	VSSCO	analog ground
HP_OUTL	16	A	APIO	left output voltage
SPDIF				
$V_{DDA(3V3\_SPDIF)}$	30	A	VDDCO	analog supply voltage
SPDIF_IN	29	A	APIO	input voltage
$V_{SSA(SPDIF)}$	28	A	VSSCO	analog ground
I^2S-bus input				
I2SIN_1_DATA	72	I	IPTHT5V	serial data channel 1
I2SIN_1_WS	73	I/O	BPTS10THT5V	word select channel 1
I2SIN_1_BCK	74	I/O	BPTS10THT5V	bit clock channel 1

Table 2: Pin description *...continued*

Symbol	Pin	Special [1]	Type	Description
GPIO_10/I2SIN_2_BCK	7	I/O	BPTS10THT5V	general purpose IO/I²S-bus input bit clock channel 2
GPIO_09/I2SIN_2_WS	87	I/O	BPTS10THT5V	general purpose IO/I²S-bus input word select channel 1
GPIO_08/I2SIN_2_DATA	84	I/O	BPTS10THT5V	general purpose IO/I²S-bus input serial data channel 2
I²S-bus output				
I2SOUT_WS	76	I/O	BPTS10THT5V	word select
I2SOUT_BCK	77	I/O	BPTS10THT5V	bit clock
I2SOUT_2_DATA	78	O	OTS10CT5V	serial data channel 2
I2SOUT_1_DATA	79	O	OTS10CT5V	serial data channel 1
Control ADC				
$V_{SSA(ADC10B)}$	44	A	VSSCO	analog ground
$V_{DDA(3V3\_ADC10B)}$	43	A	VDDCO	analog supply voltage
ADC10B_GPA3	42	A	APIO	analog general purpose input 3
ADC10B_GPA2	41	A	APIO	analog general purpose input 2
ADC10B_GPA1	40	A	APIO	analog general purpose input 1
ADC10B_GPA0	39	A	APIO	analog general purpose input 0
GPIO				
GPIO_13	10	I/O	BPTS10THT5V	general purpose IO
GPIO_12	9	I/O	BPTS10THT5V	general purpose IO
GPIO_11/SRI_INT	8	I/O	**<tbd>**	general purpose IO
GPIO_10/I2SIN_2_BCK	7	I/O	BPTS10THT5V	general purpose IO/I²S-bus input bit clock channel 2
GPIO_09/I2SIN_2_WS	87	I/O	BPTS10THT5V	general purpose IO/I²S-bus input word select channel 1
GPIO_08/I2SIN_2_DATA	84	I/O	BPTS10THT5V	general purpose IO/I²S-bus input serial data channel 2
GPIO_07/UART_TXS	83	I/O	BPTS10THT5V	general purpose IO
GPIO_06/UART_RXS	82	I/O	BPTS10THT5V	general purpose IO
GPIO_05/UART_NCTS	81	I/O	BPTS10THT5V	general purpose IO
GPIO_04/UART_NRTS	80	I/O	BPTS10THT5V	general purpose IO
GPIO_03	47	I/O	BPTS10THT5V	general purpose IO
GPIO_02/MODE_1	48	I/O	BPTS10THT5V	general purpose IO/boot-up mode selection pin 1
GPIO_01/MODE_0	49	I/O	BPTS10THT5V	general purpose IO/boot-up mode selection pin 0
GPIO_00	50	I/O	BPTS10THT5V	general purpose IO
System I²C-bus				
IIC_MS_SCL	2		IIC400KT5V	clock input or output
IIC_MS_SDA	3		IIC400KT5V	data input or output
Other				
CLK_OUT2	75	O	OTS10CT5V	clock output 2

Table 2: Pin description *…continued*

Symbol	Pin	Special [1]	Type	Description
CLK_OUT1	71	O	OTS10CT5V	clock output 1
RSTIN_N	4	I	IPTHU5V	system reset input
JTAG				
JTAG_TRST_N	68	I	IPTHDT5V	reset input
JTAG_TCK	67	I	IPTHDT5V	clock input
JTAG_TDI	64	I	IPTHDT5V	data input
JTAG_TMS	65	I	IPTHDT5V	mode select input
JTAG_TDO	66	O	OTS10CT5V	data output

[1] A = analog.
I = input.
O = output.

Table 3: Cell types description

Cell name	Definition
IPTHT5V	input pad; push pull; TTL with hysteresis; 5 V tolerant
IPTHU5V	input pad; push pull; TTL with hysteresis; pull-up; 5 V tolerant
IPTHDT5V	input pad; push pull; TTL with hysteresis; pull-down; 5 V tolerant
OTS10CT5V	output pad; 3-state; 10 ns slew rate control; 5 V tolerant
BPTS10THT5V	bi-directional pad; plain input; 3-state output; 10 ns slew rate control; TTL with hysteresis; 5 V tolerant
IIC400KT5V	I^2C-bus pad; 400 kHz I^2C-bus specification; 5 V tolerant
APIO	analog pad; analog input/output
VDDI	V_{DD} pad connected to core V_{DD} and internal V_{DD} supply voltage rail in I/O ring
VDDCO	V_{DD} pad connected to core V_{DD}
VDDE3V3	V_{DD} pad connected to external 3.3 V V_{DD} supply voltage rail
VSSCO	V_{SS} pad connected to core V_{SS}
VSSE3V3	V_{SS} pad connected to external 3.3 V V_{SS} supply voltage rail
VSSI	V_{SS} pad connected to core V_{SS}; internal V_{SS} supply voltage rail in I/O ring and substrate rail in I/O ring

7. Functional description

7.1 EPICS7B

The EPICS7B core has only access to four of the five memory spaces, PMEM, XMEM, YMEM and DIO. Memory space IO is only accessible via the DMA. To distinguish between the memory spaces, 18-bit addressing is used, of which the two Most Significant (MS) bits determine which space the address is in, see Table 4. The EPICS7B only knows about the 16 least significant bits and uses special instructions to access DIO space.

EPICS7B access:

XMEM is accessed by EPICS7B when using X in its instructions

YMEM is accessed by EPICS7B when using Y in its instructions

PMEM is accessed by EPICS7B when it is fetching instructions

DIO is accessed by EPICS7B when using D in its instructions.

All 18 bits are used when accessing memory via DMA.

Table 4: Memory spaces

Two MS bits	Memory space
00	XMEM
01	YMEM
10	PMEM
11	DIO or IO

The memory map of the system is described in Table 5 and Figure 4.

Table 5: Memory map

Address	Type	Words	Bits
IO			
0x[3]FFFF	DSP control register	64	32
0x[3]FFFE	EPICS7B instruction register		32
0x[3]FFC0 to 0x[3]FFFD	user defined	64	32
DIO			
0x[3]FF00 to 0x[3]FF3F	DIO registers		24
PMEM			
0x[2]8000 to 0x[2]97FF	PRAM	6144	
0x[2]0000 to 0x[2]5FFF	PROM [1]	24576	
0x[2]0000 to 0x[2]00FF	BIOSROM [1]		
YMEM			
0x[1]8000 to 0x[1]87FF	YRAM	2048	
0x[1]0000 to 0x[1]2FFF	YROM	12288	
XMEM			
0x[0]FFC0 to 0x[0]FFFF	memory mapped registers		
0x[0]0000 to 0x[0]2FFF	XRAM	12288	

[1] DSP control register bit 0 is selecting PROM or BIOSROM.

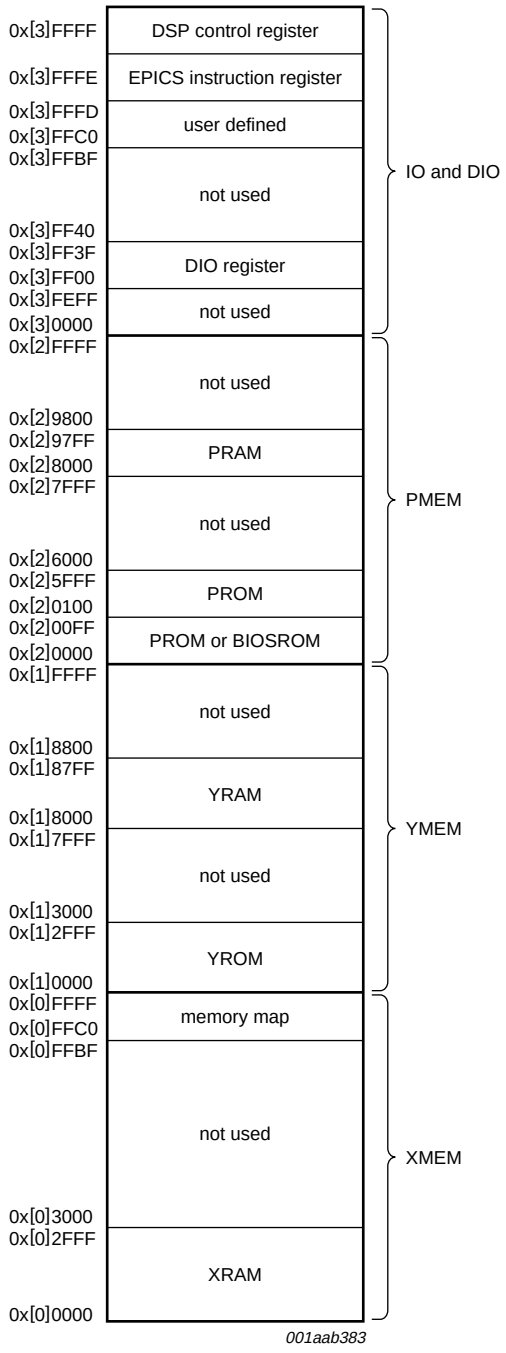


Fig 4. Memory map

The control registers are split in two different spaces. One space is accessible only via DMA while the other space is accessible both via DMA and the DSP core. This space is therefore X-memory mapped.

The location and definition of the control registers is described in Table 6.

Table 6: Control registers description

Register name	Address	R/W	Description	Reset
DSP				
PC	0x0 FFFF	W	program counter register	undefined
SR1	0x0 FFFE	W	status register 1	undefined
SR2	0x0 FFFD	W	status register 2	undefined
RTI_STACK	0x0 FFFC	W	interrupt stack register	undefined
IO_DIR	0x0 FFFB	W	configuration register 1	0x00 0000
IO_MODE	0x0 FFFA	W	configuration register 2	0x00 0FFD
CR	0x3 FFFF	W	control register I/O mapped	0x00 0000
EIR	0x3 FFFE	W	EPICS7B instruction register	0x00 0000
Interrupt controller				
INTC_POL	0x0 FFF9	W	polarity select	0x03 FFFF
INTC_MODE	0x0 FFF8	W	mode select	0x03 FFFF
INTC_MASK	0x0 FFF7	W	mask	0x03 FFFF
INTC_STATUS	0x0 FFF6	R	status	undefined
INTC_TEST	0x0 FFF5	W	test	0x00 0001
INTC_SWCLR	0x0 FFF4	W	software clear	0x00 0000
INTC_SLCT	0x0 FFF3	W	user flag	0x00 0000
DMA controller				
DMAC_IC	0x0 FFF2	R	IRQ counter value	0x00 0000

The interrupts and connection order are described in Table 7.

Table 7: Interrupt flags

Interrupt flag	Symbol	Description
0	FI_DMAC	DMAC interrupt
1	FI_SRI_DMA_RX_RDY	SRI RX DMA block transfer interrupt
2	FI_FLSTART	FSL start interrupt
3	FI_EVENTROUTER	event router interrupt
4	FI_SRI_DMA_TX_RDY	SRI TX DMA block transfer interrupt
5	FI_I2SIN_1	I^2S-bus input 1 interrupt
6	FI_I2SIN_2	I^2S-bus input 2 interrupt
7	FI_SPDIF	SPDIF input interrupt
8	FI_ADC	ADC input interrupt
9	FI_DACALL	I^2S-bus and DAC outputs interrupt
10	FI_RSC_ENCRDY	RSC encoder ready interrupt
11	FI_RSC_DECRDY	RSC decoder ready interrupt
12	FI_RSC_DMARDY	RSC DMA block transfer ready interrupt
13	FI_VPB0	VPB0 interrupt
14	FI_VBP1	VPB1 interrupt
15	FI_UART	UART interrupt
16	FI_I2C_DMARDY	I^2C-bus M/S DMA block transfer interrupt
17	FI_FSLFAST	FSL fast interrupt

The outputs of the ADC, I²S-bus inputs, SPDIF inputs and VPB buses are mapped to the inputs of the EPICS7B.

Table 8: DIO input registers

DIO input register	Register name	Description
0	I2SIN_1L	I²S-bus input 1 left channel
1	I2SIN_1R	I²S-bus input 1 right channel
2	I2SIN_2L	I²S-bus input 2 left channel
3	I2SIN_2R	I²S-bus input 2 right channel
4	SPDIF L	SPDIF input left channel
5	SPDIF R	SPDIF input right channel
6	ADC_L	ADC input left channel
7	ADC_R	ADC input right channel
8	VPB0_DI1	VPB0 data input 1 (bit 0 to bit 15)
9	VPB0_DI2	VPB0 data input 2 (bit 16 to bit 31)
10	VPB1_DI	VPB1 data input (UART)
11	TS_COUNTER	
12	I2SIN_1TS	time stamp counter i2sin1
13	I2SIN_2TS	time stamp counter i2sin2
14	SPDIF_TS	time stamp counter spdif
15	ADC_TS	time stamp counter adc
16	I2SOUT_TS	time stamp counter i2sout
17	TS_COUNTER	

The control of the DAC, I²S-bus outputs and VPB buses are mapped to the outputs of the EPICS7B.

Table 9: DIO output registers

DIO output register	Register name	Description
0	I2SOUT_1L	I²S-bus output 1 left channel
1	I2SOUT_1R	I²S-bus output 1 right channel
2	I2SOUT_2L	I²S-bus output 2 left channel
3	I2SOUT_2R	I²S-bus output 2 right channel
4	DAC_L	DAC output left channel
5	DAC_R	DAC output right channel
6	not connected	
7	not connected	
8	VPB0_DO1	VPB0 data output 1 (bit 0 to bit 15)
9	VPB0_DO2	VPB0 data output 2 (bit 16 to bit 31)
10	VPB0_ADDR	VPB0 address
11	VPB1_DO	VPB1 data output (UART)
12	VPB1_ADDR	VPB1 address
13	not connected	
14	not connected	

Table 9: DIO output registers *…continued*

DIO output register	Register name	Description
15	not connected	
16	not connected	
17	not connected	

7.1.1 User registers

The user registers are memory mapped control signals used to control integrated wireless audio baseband functionality.

Table 10: User register description

Register name	Address	R/W	Description	Reset
SRI_TX_ADDR	0x0 FFDE	W	serial radio interface DMA from MEM start address	0x000 0000
SRI_TX_BLKSIZE	0x0 FFDD	W	serial radio interface DMA from MEM block size	0x000 0000
SRI_MODE	0x0 FFDC	W	serial radio interface mode control	0x000 0000
SRIM_TSTART	0x0FFDB	W	serial radio interface master mode start time	0x000 0000
SRIM_TLINK	0x0 FFDA	W	serial radio interface master mode sync-link time	0x000 0000
SRIM_TIDLE	0x0 FFD9	W	serial radio interface master mode idle time	0x000 0000
SRIM_DLLEN	0x0 FFD8	W	serial radio interface master mode number downlink words	0x000 0000
SRIM_ULLEN	0x0 FFD7	W	serial radio interface master mode number uplink words	0x000 0000
FSL_MODE	0x0 FFD6	W	frame sync lock mode control	0x000 0000
APLL_CONTROL	0x0 FFD5	W	audio PLL direct control	0x000 0000
APLL_SELECT	0x0 FFD4	W	audio PLL direct control select	0x000 0000
SPDIF_STATUS	0x0 FFD3	R	SPDIF status	0x000 0000
FSY_INPERIOD	0x0 FFD2	R	frame sync measured period	0x000 0000
FSY_REFPERIOD	0x0 FFD1	R	frame sync reference measured period	0x000 0000
FSY_PHASEDIF	0x0 FFD0	R	frame sync phase difference	0x000 0000
IWAB_BOOTCFG	0x0 FFCF	W	SAA8200HL boot mode configuration	0x000 0000
SRI_STATUS	0x0 FFCE	R	serial radio interface status	0x000 0000
APLL_ACK	0x0 FFCD	R	audio PLL direct control acknowledge	0x000 0000
RSC_STATUS	0x0 FFCC	R	Reed-Solomon status	0x000 0000
RSC_CONTROL	0x0 FFCB	W	Reed-Solomon control	0x000 0000
RSC_ADDR	0x0 FFCA	W	Reed-Solomon DMA start address	0x000 0000
RSC_BLKSIZE	0x0 FFC9	W	Reed-Solomon DMA block size	0x000 0000

Table 10: User register description *...continued*

Register name	Address	R/W	Description	Reset
SRI_RX_ADDR	0x0FFC8	W	serial radio interface DMA to MEM start address	0x000 0000
SRI_RX_BLKSIZE	0x0FFC7	W	serial radio interface DMA to MEM block size	0x000 0000
APLL_M	0x0FFC6	W	direct control of audio PLL M value	0x000 0000
APLL_N	0x0FFC5	W	direct control of audio PLL N value	0x000 0000
I2C_ADDR	0x0FFC4	W	master/slave I^2C-bus DMA memory address	0x002 8000
I2C_BLKSIZE	0x0FFC3	W	master/slave I^2C-bus DMA block size	0x000 0000
I2C_CONTROL	0x0FFC2	W	master/slave I^2C-bus control	0x000 0002
MPI_DEVADDR	0x0FFC1	W	MPI device address	0x000 0048

7.2 VPB0 bridge

Section 7.2 specifies the interfaces and function of the VPB0 bridge. The VPB0 bridge acts as a bridge between a range of RTG IP blocks using the VPB bus and the EPICS7B DIO interface. Two bridges are used one to connect to several slow blocks and an additional one specifically for the UART.

The VPB0 bridge forms the bridge between the EPICS7B and the clock generation unit, SRI I^2C-bus, watchdog timer, event router, I/O configuration and the audio configuration respectively.

7.2.1 VPB0 bridge address definitions

Table 11: VPB0 bridge interface description

Base address	Offset	Key	Description
0x0000			**clock generation unit**
	0x0000	SCR_LP0	switch control register for system PLL clock
	0x0004	SCR_HP0	switch control register for audio PLL clock
	0x0008	SCR_DCDC	switch control register for DC-to-DC converter clock
	0x000C	SCR_SPDIF	switch control register for SPDIF clock
	0x0010	SCR_I2SIN_1	switch control register for I2SIN_1 bit clock
	0x0014	SCR_I2SIN_2	switch control register for I2SIN_2 bit clock
	0x0018	SCR_I2SOUT	switch control register for I2SOUT bit clock
	0x001C	SCR_SRI_GCHCLK	switch control register for SRI gated channel clock
	0x0020	SCR_CR_CLK_OUT1	switch control register for CR output 1 clock
	0x0024	SCR_CR_CLK_OUT2	switch control register for CR output 2 clock
	0x0028	SCR_SRI_CHCLK	switch control register for SRI reference channel clock
	0x002C	FS1_ LP0	frequency select side 1 for system PLL clock
	0x0030	FS1_ HP0	frequency select side 1 for audio PLL clock
	0x0034	FS1_ DCDC	frequency select side 1 for DC-to-DC converter clock
	0x0038	FS1_ SPDIF	frequency select side 1 for SPDIF clock

Table 11: VPB0 bridge interface description *…continued*

Base address	Offset	Key	Description
	0x003C	FS1_ I2SIN_1	frequency select side 1 for I2SIN_1 bit clock
	0x0040	FS1_ I2SIN_2	frequency select side 1 for I2SIN_2 bit clock
	0x0044	FS1_ I2SOUT	frequency select side 1 for I2SOUT bit clock
	0x0048	FS1_ SRI_GCHCLK	frequency select side 1 for SRI gated channel clock
	0x004C	FS1_ CR_CLK_OUT1	frequency select side 1 for CR output 1 clock
	0x0050	FS1_ CR_CLK_OUT2	frequency select side 1 for CR output 2 clock
	0x0054	FS1_ SRI_CHCLK	frequency select side 1 for SRI reference channel clock
	0x0058	FS2_ LP0	frequency select side 2 for system PLL clock
	0x005C	FS2_ HP0	frequency select side 2 for audio PLL clock
	0x0060	FS2_ DCDC	frequency select side 2 for DC-to-DC converter clock
	0x0064	FS2_ SPDIF	frequency select side 2 for SPDIF clock
	0x0068	FS2_ I2SIN_1	frequency select side 2 for I2SIN_1 bit clock
	0x006C	FS2_ I2SIN_2	frequency select side 2 for I2SIN_2 bit clock
	0x0070	FS2_ I2SOUT	frequency select side 2 for I2SOUT bit clock
	0x0074	FS2_ SRI_GCHCLK	frequency select side 2 for SRI gated channel clock
	0x0078	FS2_ CR_CLK_OUT1	frequency select side 2 for CR output 1 clock
	0x007C	FS2_ CR_CLK_OUT2	frequency select side 2 for CR output 2 clock
	0x0080	FS2_ SRI_CHCLK	frequency select side 2 for SRI reference channel clock
	0x0084	SSR_ LP0	frequency select status for system PLL clock
	0x0088	SSR_ HP0	frequency select status for audio PLL clock
	0x008C	SSR_ DCDC	frequency select status for DC-to-DC converter clock
	0x0090	SSR_ SPDIF	frequency select status for SPDIF clock
	0x0094	SSR_ I2SIN_1	frequency select status for I2SIN_1 bit clock
	0x0098	SSR_ I2SIN_2	frequency select status for I2SIN_2 bit clock
	0x009C	SSR_ I2SOUT	frequency select status for I2SOUT bit clock
	0x00A0	SSR_ SRI_GCHCLK	frequency select status for SRI gated channel clock
	0x00A4	SSR_ CR_CLK_OUT1	frequency select status for CR output 1 clock
	0x00A8	SSR_ CR_CLK_OUT2	frequency select status for CR output 2 clock
	0x00AC	SSR_ SRI_CHCLK	frequency select status for SRI reference channel clock
	0x00B0	PCR_SPD_SYSCLK	power control register for system clock
	0x00B4	PCR_SYSCLK_DIV4	power control register for $0.25 \times f_s$ system clock
	0x00B8	PCR_UART_UCLK	power control register for UART clock
	0x00BC	PCR_VPB1_PCLK	power control register for VPB1 bus clock
	0x00C0	PCR_UART_PCLK	power control register for UART bus clock
	0x00C4	PCR_DEBOUNCE_PCLK	power control register for DEBOUNCE bus clock
	0x00C8	PCR_CGU_PCLK	power control register for CGU bus clock
	0x00CC	PCR_WDOG_PCLK	power control register for WDOG bus clock
	0x00D0	PCR_ADC_PCLK	power control register for control ADC bus clock
	0x00D4	PCR_IOCONF_PCLK	power control register for IO configuration bus clock
	0x00D8	PCR_EVENT_ROUTER_PCLK	power control register for event router bus clock
	0x00DC	PCR_SRI_I2C_PCLK	power control register for SRI I^2C-bus clock

Table 11: VPB0 bridge interface description *...continued*

Base address	Offset	Key	Description
	0x00E0	PCR_ADC_CLK	power control register for control ADC system clock
	0x00E4	PCR_I2C_MS_PCLK	power control register for M/S I^2C-bus clock
	0x00E8	PCR_RSC_PCLK	power control register for RSC bus clock
	0x00EC	PCR_EXTDMACNTR_PCLK	power control register for external DMA controller clock
	0x00F0	PCR_DIO2VPB0 _PCLK	power control register for DIO2VPB0 bus clock
	0x00F4	PCR_DIO2VPB1_PCLK	power control register for DIO2VPB1 bus clock
	0x00F8	PCR_I2SIN_1 _PCLK	power control register for I2SIN_1 bus clock
	0x00FC	PCR_I2SIN_2 _PCLK	power control register for I2SIN_2 bus clock
	0x0100	PCR_I2SOUT_1 _PCLK	power control register for I2SOUT_1 bus clock
	0x0104	PCR_I2SOUT_2_PCLK	power control register for I2SOUT_2 bus clock
	0x0108	PCR_ADSS _PCLK	power control register for ADSS bus clock
	0x010C	PCR_AUDIO_CONFIG _PCLK	power control register for audio configuration bus clock
	0x0110	PCR_SPDIF _PCLK	power control register for SPDIF bus clock
	0x0114	PCR_SRI _PCLK	power control register for SRI bus clock
	0x0118	PCR_FRAMESYNCREF	power control register for SRI frame sync reference
	0x011C	PCR_CR_I2SIN_2_BCK	power control register for I2SIN_2 bit clock
	0x0120	PCR_CR_I2SIN_1_BCK	power control register for I2SIN_1 bit clock
	0x0124	PCR_CR_I2SOUT_BCK	power control register for I2SOUT bit clock
	0x0128	PCR_CR_I2SIN_2_WS	power control register for I2SIN_2 word select
	0x012C	PCR_CR_I2SIN_1_WS	power control register for I2SIN_1 word select
	0x030	PCR_CR_I2SOUT_WS	power control register for I2SOUT word select
	0x0134	PCR_SDAC_NS_CLK	power control register for SDAC new sample
	0x0138	PCR_SDAC_DSPCLK	power control register for SDAC DSP clock
	0x013C	PCR_SADC_DECCLK	power control register for SADC decimation filter clock
	0x0140	PCR_SADC_SYSCLK	power control register for SADC system clock
	0x0144	PCR_DCDC_CONVERTER_CLK	power control register for DC-to-DC converter clock
	0x0148	PCR_SPDIF_BCK	power control register for SPDIF bit clock from pad
	0x014C	PCR_I2SIN_1_BCK	power control register for I2SIN_1 bit clock from pad
	0x0150	PCR_I2SIN_2_BCK	power control register for I2SIN_2 bit clock from pad
	0x0154	PCR_I2SOUT_BCK	power control register for I2SOUT bit clock from pad
	0x0158	PCR_SRI_GCC_SHO	power control register for SRI gated channel clock from pad
	0x015C	PCR_CR_CLK_OUT1	power control register for crystal output 1 from pad
	0x0160	PCR_CR_CLK_OUT2	power control register for crystal output 2 from pad
	0x0164	PCR_SRI_CHCLK	power control register for SRI channel clock
	0x0168	PSR_SPD_SYSCLK	power status register for system clock
	0x016C	PSR_SYSCLK_DIV4	power status register for $0.25 \times f_s$ system clock
	0x0170	PSR_UART_UCLK	power status register for UART clock
	0x0174	PSR_VPB1_PCLK	power status register for VPB1 bus clock
	0x0178	PSR_UART_PCLK	power status register for UART bus clock
	0x017C	PSR_DEBOUNCE_PCLK	power status register for DEBOUNCE bus clock
	0x0180	PSR_CGU_PCLK	power status register for CGU bus clock

Table 11: VPB0 bridge interface description *…continued*

Base address	Offset	Key	Description
	0x0184	PSR_WDOG_PCLK	power status register for WDOG bus clock
	0x0188	PSR_ADC_PCLK	power status register for control ADC bus clock
	0x018C	PSR_IOCONF_PCLK	power status register for IO configuration bus clock
	0x0190	PSR_EVENT_ROUTER_PCLK	power status register for event router bus clock
	0x0194	PSR_SRI_I2C_PCLK	power status register for SRI I^2C-bus clock
	0x0198	PSR_ADC_CLK	power status register for control ADC system clock
	0x019C	PSR_I2C_MS_PCLK	power status register for M/S I^2C-bus clock
	0x01A0	PSR_RSC_PCLK	power status register for RSC bus clock
	0x01A4	PSR_EXTDMACNTR_PCLK	power status register for external DMA controller clock
	0x01A8	PSR_DIO2VPB0 _PCLK	power status register for DIO2VPB0 bus clock
	0x01AC	PSR_DIO2VPB1_PCLK	power status register for DIO2VPB1 bus clock
	0x01B0	PSR_I2SIN_1 _PCLK	power status register for I2SIN_1 bus clock
	0x01B4	PSR_I2SIN_2 _PCLK	power status register for I2SIN_2 bus clock
	0x01B8	PSR_I2SOUT_1 _PCLK	power status register for I2SOUT_1 bus clock
	0x01BC	PSR_I2SOUT_2_PCLK	power status register for I2SOUT_2 bus clock
	0x01C0	PSR_ADSS _PCLK	power status register for ADSS bus clock
	0x01C4	PSR_AUDIO_CONFIG _PCLK	power status register for audio configuration bus clock
	0x01C8	PSR_SPDIF _PCLK	power status register for SPDIF bus clock
	0x01CC	PSR_SRI _PCLK	power status register for SRI bus clock
	0x01D0	PSR_FRAMESYNCREF	power status register for SRI frame sync reference
	0x01D4	PSR_CR_I2SIN_2_BCK	power status register for I2SIN_2 bit clock
	0x01D8	PSR_CR_I2SIN_1_BCK	power status register for I2SIN_1 bit clock
	0x01DC	PSR_CR_I2SOUT_BCK	power status register for I2SOUT bit clock
	0x01E0	PSR_CR_I2SIN_2_WS	power status register for I2SIN_2 word select
	0x01E4	PSR_CR_I2SIN_1_WS	power status register for I2SIN_1 word select
	0x01E8	PSR_CR_I2SOUT_WS	power status register for I2SOUT word select
	0x01EC	PSR_SDAC_NS_CLK	power status register for SDAC new sample
	0x01F0	PSR_SDAC_DSPCLK	power status register for SDAC DSP clock
	0x01F4	PSR_SADC_DECCLK	power status register for SADC decimation filter clock
	0x01F8	PSR_SADC_SYSCLK	power status register for SADC system clock
	0x01FC	PSR_DCDC_CONVERTER_CLK	power status register for DC-to-DC converter clock
	0x0200	PSR_SPDIF_BCK	power status register for SPDIF bit clock from pad
	0x0204	PSR_I2SIN_1_BCK	power status register for I2SIN_1 bit clock from pad
	0x0208	PSR_I2SIN_2_BCK	power status register for I2SIN_2 bit clock from pad
	0x020C	PSR_I2SOUT_BCK	power status register for I2SOUT bit clock from pad
	0x0210	PSR_SRI_GCC_SHO	power status register for SRI gated channel clock from pad
	0x0214	PSR_CR_CLK_OUT1	power status register for crystal output 1 from pad
	0x0218	PSR_CR_CLK_OUT2	power status register for crystal output 2 from pad
	0x021C	PSR_SRI_CHCLK	power status register for SRI channel clock
	0x0220	ESR_SPD_SYSCLK	enable fraction divider for system clock
	0x0224	ESR_SYSCLK_DIV4	enable fraction divider for $0.25 \times f_s$ system clock

Table 11: VPB0 bridge interface description *…continued*

Base address	Offset	Key	Description
	0x0228	ESR_UART_UCLK	enable fraction divider for UART clock
	0x022C	ESR_VPB1_PCLK	enable fraction divider for VPB1 bus clock
	0x0230	ESR_UART_PCLK	enable fraction divider for UART bus clock
	0x0234	ESR_DEBOUNCE_PCLK	enable fraction divider for DEBOUNCE bus clock
	0x0238	ESR_CGU_PCLK	enable fraction divider for CGU bus clock
	0x023C	ESR_WDOG_PCLK	enable fraction divider for WDOG bus clock
	0x0240	ESR_ADC_PCLK	enable fraction divider for control ADC bus clock
	0x0244	ESR_IOCONF_PCLK	enable fraction divider for IO configuration bus clock
	0x0248	ESR_EVENT_ROUTER_PCLK	enable fraction divider for event router bus clock
	0x024C	ESR_SRI_I2C_PCLK	enable fraction divider for SRI I^2C-bus clock
	0x0250	ESR_ADC_CLK	enable fraction divider for control ADC system clock
	0x0254	ESR_I2C_MS_PCLK	enable fraction divider for M/S I^2C-bus clock
	0x0258	ESR_RSC_PCLK	enable fraction divider for RSC bus clock
	0x025C	ESR_EXTDMACNTR_PCLK	enable fraction divider for external DMA controller clock
	0x0260	ESR_DIO2VPB0 _PCLK	enable fraction divider for DIO2VPB0 bus clock
	0x0264	ESR_DIO2VPB1_PCLK	enable fraction divider for DIO2VPB1 bus clock
	0x0268	ESR_I2SIN_1 _PCLK	enable fraction divider for I2SIN_1 bus clock
	0x026C	ESR_I2SIN_2 _PCLK	enable fraction divider for I2SIN_2 bus clock
	0x0270	ESR_I2SOUT_1 _PCLK	enable fraction divider for I2SOUT_1 bus clock
	0x0274	ESR_I2SOUT_2_PCLK	enable fraction divider for I2SOUT_2 bus clock
	0x0278	ESR_ADSS _PCLK	enable fraction divider for ADSS bus clock
	0x027C	ESR_AUDIO_CONFIG _PCLK	enable fraction divider for audio configuration bus clock
	0x0280	ESR_SPDIF _PCLK	enable fraction divider for SPDIF bus clock
	0x0284	ESR_SRI _PCLK	enable fraction divider for SRI bus clock
	0x0288	ESR_FRAMESYNCREF	enable fraction divider for SRI frame sync reference
	0x028C	ESR_CR_I2SIN_2_BCK	enable fraction divider for I2SIN_2 bit clock
	0x0290	ESR_CR_I2SIN_1_BCK	enable fraction divider for I2SIN_1 bit clock
	0x0294	ESR_CR_I2SOUT_BCK	enable fraction divider for I2SOUT bit clock
	0x0298	ESR_CR_I2SIN_2_WS	enable fraction divider for I2SIN_2 word select
	0x029C	ESR_CR_I2SIN_1_WS	enable fraction divider for I2SIN_1 word select
	0x02A0	ESR_CR_I2SOUT_WS	enable fraction divider for I2SOUT word select
	0x02A4	ESR_SDAC_NS_CLK	enable fraction divider for SDAC new sample
	0x02A8	ESR_SDAC_DSPCLK	enable fraction divider for SDAC DSP clock
	0x02AC	ESR_SADC_DECCLK	enable fraction divider for SADC decimation filter clock
	0x02B0	ESR_SADC_SYSCLK	enable fraction divider for SADC system clock
	0x02B4	ESR_DCDC_CONVERTER_CLK	enable fraction divider for DC-to-DC converter clock
		ESR_SPDIF_BCK	no fractional divider supported for this clock
		ESR_I2SIN_1_BCK	no fractional divider supported for this clock
		ESR_I2SIN_2_BCK	no fractional divider supported for this clock
		ESR_I2SOUT_BCK	no fractional divider supported for this clock
		ESR_SRI_GCC_SHO	no fractional divider supported for this clock

Table 11: VPB0 bridge interface description *...continued*

Base address	Offset	Key	Description
	0x02B8	ESR_CR_CLK_OUT1	enable fraction divider for crystal output 1 from pad
	0x02BC	ESR_CR_CLK_OUT2	enable fraction divider for crystal output 2 from pad
	0x02C0	ESR_SRI_CHCLK	enable fraction divider for SRI channel clock
	0x02C4	BCR_LP0	base control register for system PLL clock
	0x02C8	BCR_HP0	base control register for audio PLL clock
	0x2CC	FDC_SPD_SYSCLK	fractional divider control for system clock
	0x2D0	FDC_SYSCLK_DIV4	fractional divider control for $0.25 \times f_s$ system clock
	0x02D4	FDC_UART_UCLK	fractional divider control for UART clock
	0x02D8	FDC_DEBOUNCE_PCLK	fractional divider control for DEBOUNCE bus clock
	0x02DC	FDC_ADC_CLK	fractional divider control for control ADC system clock
	0x02E0	FDC_DIO_PCLK	fractional divider control for DIO interface clock
	0x02E4	FDC_AUDIO_PCLK	fractional divider control for audio bus clock
	0x02E8	FDC_FRAMESYNCREF	fractional divider control for SRI frame sync reference
	0x02EC	FDC_CR_I2SIN_2_BCK	fractional divider control for I2SIN_2 bit clock
	0x02F0	FDC_CR_I2SIN_1_BCK	fractional divider control for I2SIN_1 bit clock
	0x2F4	FDC_CR_I2SOUT_BCK	fractional divider control for I2SOUT bit clock
	0x02F8	FDC_I2S_WS	fractional divider control for I2S word select
	0x02FC	FDC_SDAC_NS_CLK	fractional divider control for SDAC new sample
	0x300	FDC_AUDIO_SYSCLK	fractional divider control for audio system clock
	0x0304	FDC_DCDC_CONVERTER_CLK	fractional divider control for DC-to-DC converter clock
	0x0308	FDC_CR_CLK_OUT1	fractional divider control for crystal output 1 from pad
	0x030C	FDC_CR_CLK_OUT2	fractional divider control for crystal output 2 from pad
	0x0310	FDC_SRI_CHCLK	fractional divider control for SRI channel clock
	0x0C00	CNF_POWERMODE	power-down CGU
	0x0C04	CNF_WD_BARK	watchdog bark register
	0x0C08	reserved	
	0xC0C	reserved	
	0x0C10	OSC_ON	activate crystal oscillator
	0x0C14	OSC_BYPASS	bypass crystal oscillator
	0x0C18	CNF_UART_RST_N	reset for UART
	0x0C1C	CNF_I2SIN_1_RST_N	reset for I2S input 1
	0x0C20	CNF_I2SIN_2_RST_N	reset for I2S input 2
	0x0C24	CNF_I2SOUT_1_RST_N	reset for I2S output 1
	0x0C28	CNF_I2SOUT_2_RST_N	reset for I2S output 2
	0x0C2C	CNF_DEC_RST_N	reset for decimation filter
	0x0C30	CNF_INT_RST_N	reset for interpolation filter
	0x0C34	CNF_SPDIF_RST_N	reset for SPDIF
	0xC38	CNF_EPICS7B_RST_N	reset for EPICS7B
	0x0C3C	CNF_DIO2VPB0_RST_N	reset for VPB0 bridge
	0x0C40	CNF_DIO2VPB1_RST_N	reset for UART VPB bridge
	0x0C44	CNF_MS_I2C_RST_N	reset for M/S I^2C-bus

Table 11: VPB0 bridge interface description *…continued*

Base address	Offset	Key	Description
	0x0C48	CNF_SRI _RST_N	reset for serial radio interface
	0x0C4C	CNF_RSC_RST_N	reset for Reed-Solomon codec
	0x0C50	CNF_SRI_I2C_RST_N	reset for SRI I^2C-bus
	0x0C54	CNF_AD10BIT_RST_N	reset for control ADC
	0x0C58	CNF_FSL_RST_N	reset for frame sync lock
	0x0C5C	CNF_GCC_RST_N	reset for gated channel clock
	0x0C60	CNF_AD10BIT_PRST_N	preset for control ADC
	0x0C64	HP0_FIN_SELECT	audio clock PLL input select
	0x0C68	HP0_MDEC	audio clock PLL M divider
	0x0C6C	HP0_NDEC	audio clock PLL N divider
	0x0C70	HP0_PDEC	audio clock PLL P divider
	0x0C74	HP0_MODE	audio clock PLL mode
	0x0C78	HP0_STATUS	audio clock PLL status
	0x0C7C	HP0_ACK	audio clock PLL acknowledge
	0x0C80	HP0_REQ	audio clock PLL change request
	0x0C84	HP0_INSELR	audio clock PLL input bandwidth selection
	0x0C88	HP0_INSELI	audio clock PLL input bandwidth selection
	0x0C8C	HP0_INSELP	audio clock PLL input bandwidth selection
	0x0C90	HP0_SELR	audio clock PLL input bandwidth selection
	0x0C94	HP0_SELI	audio clock PLL input bandwidth selection
	0x0C98	HP0_SELP	audio clock PLL input bandwidth selection
	0x0C9C	LP0_FIN_SELECT	system clock PLL input select
	0x0CA0	LP0_PWD	system clock PLL power-down
	0x0CA4	LP0_BYPASS	system clock PLL bypass
	0x0CA8	LP0_LOCK	system clock PLL in-lock
	0x0CAC	LP0_DIRECT	system clock PLL direct CCO control
	0x0CB0	LP0_MSEL	system clock PLL M divider
	0x0CB4	LP0_PSEL	system clock PLL P divider
0x1000			**SRI I^2C-bus**
	0x0000	RX	receive FIFO
	0x0000	TX	transmit FIFO
	0x0004	STS	status register
	0x0008	CTL	control register
	0x000C	CLKHI	clock divisor high
	0x0010	CLKLO	clock divisor low
	0x0014	ADDR	I^2C-bus address
	0x0028	TXS	slave transmit FIFO
0x2000			**control ADC**
	0x0000	ADC_R0	ADC data channel 0
	0x0004	ADC_R1	ADC data channel 1
	0x0008	ADC_R2	ADC data channel 2

Table 11: VPB0 bridge interface description *…continued*

Base address	Offset	Key	Description
	0x000C	ADC_R3	ADC data channel 3
	0x0010	ADC_R4	ADC data channel 4
	0x0014	ADC_R5	ADC data channel 5
	0x0018	ADC_R6	ADC data channel 6
	0x001C	ADC_R7	ADC data channel 7
	0x0020	ADC_CON	control register
	0x0024	ADC_CSEL_RES	channel and resolution selection register
	0x0028	ADC_INT_ENABLE	interrupt enable register
	0x002C	ADC_INT_STATUS	interrupt status register
	0x0030	ADC_INT_CLEAR	interrupt clear register
0x3000			**watchdog timer**
	0x0000	IR	interrupt register
	0x0004	TCR_REG	timer control register
	0x0008	TC	timer counter
	0x000C	PR_REG	pre-scale register
	0x0010	PC	pre-scale counter
	0x0014	MCR	match control register
	0x0018	MR0	match register 0
	0x001C	MR1	match register 1
	0x003C	EMR	external match register
0x4000			**event router**
	0x0804	DTR_GP_13_IRQ	de-bounce time register for GP_13_IRQ
	0x0808	DTR_GP_12_IRQ	de-bounce time register for GP_12_IRQ
	0x080C	DTR_GP_11_IRQ	de-bounce time register for GP_11_IRQ
	0x0810	DTR_GP_10_IRQ	de-bounce time register for GP_10_IRQ
	0x0814	DTR_GP_9_IRQ	de-bounce time register for GP_9_IRQ
	0x0818	DTR_GP_8_IRQ	de-bounce time register for GP_8_IRQ
	0x081C	DTR_GP_7_IRQ	de-bounce time register for GP_7_IRQ
	0x0820	DTR_GP_6_IRQ	de-bounce time register for GP_6_IRQ
	0x0824	DTR_GP_5_IRQ	de-bounce time register for GP_5_IRQ
	0x0828	DTR_GP_4_IRQ	de-bounce time register for GP_4_IRQ
	0x082C	DTR_GP_3_IRQ	de-bounce time register for GP_3_IRQ
	0x0830	DTR_GP_2_IRQ	de-bounce time register for GP_2_IRQ
	0x0834	DTR_GP_1_IRQ	de-bounce time register for GP_1_IRQ
	0x0838	DTR_GP_0_IRQ	de-bounce time register for GP_0_IRQ
	0x0C00	PEND	input event pending status
	0x0C20	INT_CLR	interrupt clear
	0x0C40	INT_SET	interrupt set
0x6000			**input/output configuration**
	0x0000	IOC_PINS	read pin values
	0x0010	IOC_MODE0	load mode 0

Table 11: VPB0 bridge interface description *…continued*

Base address	Offset	Key	Description
	0x0014	IOC_MODE0_SET	set mode 0
	0x0018	IOC_MODE0_RESET	reset mode 0
	0x0020	IOC_MODE1	load mode 1
	0x0024	IOC_MODE1_SET	set mode 1
	0x0028	IOC_MODE1_RESET	reset mode 1
0x7000			**audio configuration**
	0x0000	I2S_FORMAT_SETTINGS	I^2S-bus format settings
	0x0004	I2S_MUX_SETTINGS	I^2S-bus multiplexer settings
	0x0008	SPDIF_STATUS	SPDIF status
	0x000C	SPDIF_IRQ_EN	SPDIF interrupt enable
	0x0010	SPDIF_IRQ_STATUS	SPDIF interrupt status
	0x0014	SPDIF_IRQ_CLEAR	SPDIF interrupt clear
	0x0018	SDAC_CTRL_INTI	audio DAC input interpolation filter control
	0x001C	SDAC_CTRL_INTO	audio DAC output interpolation filter control
	0x0020	SDAC_SETTINGS	audio DAC control
	0x0024	SADC_CTRL_SDC	audio ADC amplifiers control
	0x0028	SADC_CTRL_ADC	audio ADC control
	0x002C	SADC_CTRL_DECI	audio ADC input decimation filter control
	0x0030	SADC_CTRL_DECO	audio ADC output decimation filter control
	0x0034	E7B_IRQ	EPICS7B interrupt request
	0x0038	PD_ADC10B	power-down control ADC
	0x003C	SET_DCDC1V8_ADJUST	DC-to-DC converter adjust output voltage (1.8 V)
	0x0040	SET_DCDC3V3_ADJUST	DC-to-DC converter adjust output voltage (3.3 V)
	0x0044	DCDC_CLOCKSTABLE	DC-to-DC converter clock stable signal

7.3 Clock generation unit

The Clock Generation Unit (CGU) generates all clock signals required for the SAA8200HL, it contains:

- A crystal oscillator
- For low power mode the internal DC-to-DC converter clock can be used as system clock
- An audio PLL to generate audio sample frequencies
- A system PLL to generate the clocks for the VPB bus and the DSP subsystem
- A clock switch block
- A configuration register block
- A reset and power block.

An 11.2896 MHz oscillator or an external 11.025 MHz clock (provided by the TEA7000) can be used in combination with the two PLLs and the external clocks to generate the system frequencies.

All PLLs are programmed with the registers in the register configuration block.

7.3.1 Crystal oscillator

The crystal oscillator is a 50 MHz Pierce crystal oscillator with amplitude control. It can be used in many applications e.g. as a digital reference for digital circuits, A/D and D/A clocking, etc. It is a robust design and can be used across a large frequency range.

Features:

- On-chip biasing resistance
- Amplitude controlled
- Large frequency range: 1 MHz to 20 MHz
- Slave mode
- Power-down mode
- Bypass test mode.

7.3.2 Audio PLL

The audio PLL is a multi purpose PLL.

Features:

- Integrated PLL with on-chip Current Controlled Oscillator (CCO), no external components for clock generation
- Input frequency range: 100 kHz to 150 MHz
- CCO output frequency: 275 MHz to 550 MHz
- Output frequency range: 4.3 MHz to 550 MHz
- Programmable pre-divider, feedback-divider and post-divider
- On the fly adjustment of the clock possible
- Positive edge locking
- Frequency limiter to avoid hang-up of the PLL
- Lock detector
- Power-down mode
- Possibility to bypass whole PLL, the post-divider or the pre-divider
- Possibility to disable the output clock
- Skew mode
- Free running mode
- Scan mode
- Maximum peak cycle-to-cycle output jitter = 200 ps.

7.3.3 System PLL

The DSP-PLL works in normal operating mode with feedback-divider and with post-divider, this means that the base for the clock signal is the current controlled oscillator ($f_{out} = f_{cco/P}$), running on 264.6 MHz. The output clock (f_{out}) is divided-by-2 to generate a 132.3 MHz clock.

Features:

- Integrated PLL with on-chip Current Controlled Oscillator (CCO), no external components for clock generation
- Functional down to 1.2 V (with reduced frequency range)
- 10 MHz to 25 MHz input frequency range
- 9.75 MHz to 160 MHz selectable output frequency with 50 % output duty cycle
- 156 MHz to 320 MHz CCO frequency range
- Power-down mode
- Input clock bypass mode
- Lock detector available
- Current consumption maximum 1 mA
- Maximum peak cycle-to-cycle output jitter = 300 ps.

7.4 Serial radio interface

Features:

- Interface between wireless audio baseband processor and wireless audio radio IC
- Bi-directional 3-wire serial interface
- Can be locked to audio sample frequencies
- Enables end-to-end audio clock synchronization
- Supports master and slave modes
- Supports continuous and high speed repetitive burst mode
- Control of the radio IC is handled via a separate I^2C-bus interface
- Designed for minimal interference with the radio chip.

7.5 SRI I^2C-bus

The I^2C-bus master/slave module provides a serial interface that meets the I^2C-bus specification and supports all transfer modes from and to the I^2C-bus. It supports the following functionality:

- It supports both the normal mode (100 kHz SCL) and the fast mode (400 kHz SCL)
- It has word (32-bit) access from the CPU side
- Interrupt generation on received or sent byte (and some special cases).

The purpose of the SRI I^2C-bus is to allow the download of program code from an external EEPROM at start-up, configuration and monitoring of the radio IC (TEA7000), and storage/retrieval of application specific parameters in an external data EEPROM.

7.6 System I²C-bus interface

A master and slave DMA interface to the EPICS7B sub-system and the means to select one or the other are provided. The I²C-bus master/slave module provides a serial interface that meets the I²C-bus specification and supports all transfer modes from and to the I²C-bus.

Features:

- Supports both the normal mode (100 kHz SCL) and the fast mode (400 kHz SCL)
- 32-bit word access from the CPU side
- Interrupt generation on received or sent byte (and some special cases)
- Four modes of operation:
  - master transmitter
  - master receiver
  - slave transmitter
  - slave receiver.

7.7 Control ADC

This section describes the multi-channel 10-bit control ADC interface module, a module that connects an ADC to a DSP. The ADC interface module can be used for observing battery voltage.

The interface can be divided into two main modules; a 10-bit ADC and an ADC controller.

The 10-bit ADC is a 10-bit successive approximation ADC. The ADC controller module is responsible for the communication between the ADC and DSP.

Features:

- Four analog input channels, selected by an analog multiplexer
- Programmable ADC resolution from 2-bit to 10-bit
- Single ADC scan mode and continuous ADC scan mode
- Converted digital values are stored in a 2×10-bit register
- Power-down mode.

7.8 Watchdog timer

Once the watchdog is enabled, it will monitor the programmed time out period and generates a reset request when the period expires. In normal operation the watchdog is triggered periodically, resetting the watchdog counter and ensuring that no reset is generated. In the event of a software or hardware failure preventing the CPU from triggering the watchdog, the time out will be exceeded and a reset requested from the CGU.

The interrupt pin of this watchdog timer is not connected to the interrupt controller. Instead of this, two pins M0 and M1 are used which will generate events. Pins M0 and M1 will generate events when their match register matches the Timer Counter (TC) register.

The watchdog timer in the SAA8200HL can be used as follows:

- As watchdog, the M1 output is used for generating an event to the CGU, which requests a reset.
- As timer, the M0 output is used for generating an event to the event router, which generates an interrupt to the interrupt controller.
- As watchdog and as timer, the value of the MCR0 has to be lower than the value of MCR1 (otherwise unwanted resets could be generated by the CGU).

7.9 Reed-Solomon codec

The Reed-Solomon codec is an essential part of the baseband IC. It allows redundancy to be added to the transmitted bits so that transmission errors can be corrected at the receiving end. The Reed-Solomon codec will provide some flexibility to the customer to choose packet length. For SBC based applications the Reed-Solomon block length will be such that it contains one or two SBC-encoded audio frames.

The Reed-Solomon codec is a hardware block that makes use of a locally attached memory for I/O, work space and temporary storage. The communication between this local RAM and the EPICS7B X-memory space will happen via the external DMA controller.

Features:

- 8-bit; 1-byte symbols
- 256-byte blocks
- 16 parity bytes
- No interleaving (for latency reduction)
- Automatic zero insertion (virtual zero padding).

7.10 Event router

This module can be used in low power systems to request power-up or start a clock on an external or internal event. It can also be used to generate interrupts as a result:

- Provides bus-controlled routing of input events to multiple outputs for use as interrupts or wake-up signals
- Input events can be used either directly or latched (edge detected) as an interrupt source:
  - Direct interrupts will disappear when the event becomes inactive
  - Latched interrupts will remain active until they are explicitly cleared.
- Interrupt events can be inverted (programmable)
- Each interrupt can be masked on event level
- Interrupt event detect status can be read per interrupt type
- Interrupt detection is fully asynchronous (no active clock required).

The event router provides bus control over the interrupt system. The event sources can be defined, their polarity and activation type selected, also each input can be routed to any output(s) at reset.

Table 12: Event router connections overview

Event	Name	Description
Input		
0	SPDIF_IN	
1	GP_13_IRQ	interrupt from general purpose pin
2	GP_12_IRQ	interrupt from general purpose pin
3	GP_11_IRQ	interrupt from general purpose pin
4	GP_10_IRQ	interrupt from general purpose pin
5	GP_9_IRQ	interrupt from general purpose pin
6	GP_8_IRQ	interrupt from general purpose pin
7	GP_7_IRQ	interrupt from general purpose pin
8	GP_6_IRQ	interrupt from general purpose pin
9	GP_5_IRQ	interrupt from general purpose pin
10	GP_4_IRQ	interrupt from general purpose pin
11	GP_3_IRQ	interrupt from general purpose pin
12	GP_2_IRQ	interrupt from general purpose pin
13	GP_1_IRQ	interrupt from general purpose pin
14	GP_0_IRQ	interrupt from general purpose pin
15	I2C_SRI_NINTR	I^2C-bus SRI event interrupt
16	ADC10B_IRQ	Control ADC event interrupt
17	FSL_START_IRQ	FrameSyncLock (FSL) start of frame
18	FSL_FAST_IRQ	FrameSyncLock (FSL) fast interrupt for APLL control
19	XDMA_I2C_DMARDY	block transfer I^2C-bus MS ready
20	XDMA_MPIARDY	block transfer I^2C-bus MPI ready
21	SRI_TXFIFO_EMPTYLEVEL	SRI TXFIFO reached empty level
22	SRI_RXFIFO_FULLLEVEL	SRI RXFIFO reached full level
23	SRI_TXFIFO_UNDERRUN	exception: TXFIFO underrun occurred
24	SRI_RXFIFO_OVERRUN	exception: RXFIFO overrun occurred
25	WDT_NINT	watchdog timer event interrupt
26	WDT_M0	watchdog time match 0
27	WDT_M1	watchdog time match 1
28	SRI_ULD_REQ	SRI
Output		
0	CASCADED_INTERRUPT_0	EPICS7B interrupt
1	WATCHDOG_CAP0_INT	
2	CGU_WAKEUP	CGU wake-up interrupt

7.11 SPDIF inputs

One input is provided, this SPDIF input is fed through a bit slicer which is used to re-generate the bitstream signal, allowing for a higher robustness of the link.

The SPDIF input hardware consists of a series connection of a bit slicer, which is an analog module, the SPDIF decoder and a SPDIF input block. This SPDIF input block is almost the same as the SPDIF input blocks which are connected to the SPDIF input pads. The only difference between the SPDIF input blocks is that the input format of the SPDIF input block is fixed in hardware to accept only SPD3 format.

The SPDIF decoder is running on a dedicated clock, which should lie between 36 MHz and 69 MHz. In this clock domain signal SPD3_BCK is generated, which is treated by the I^2S-bus input block as a bit clock. This bit clock is again routed via the CGU to be able to insert the test clock during test mode. The SPDIF input decoder latches it's output data on the negative edge of SPD3_BCK. The I^2S-bus input will latch the data on the positive edge of the bit clock. This guarantees reliable data transfer even though the clock is delayed by the path through the CGU.

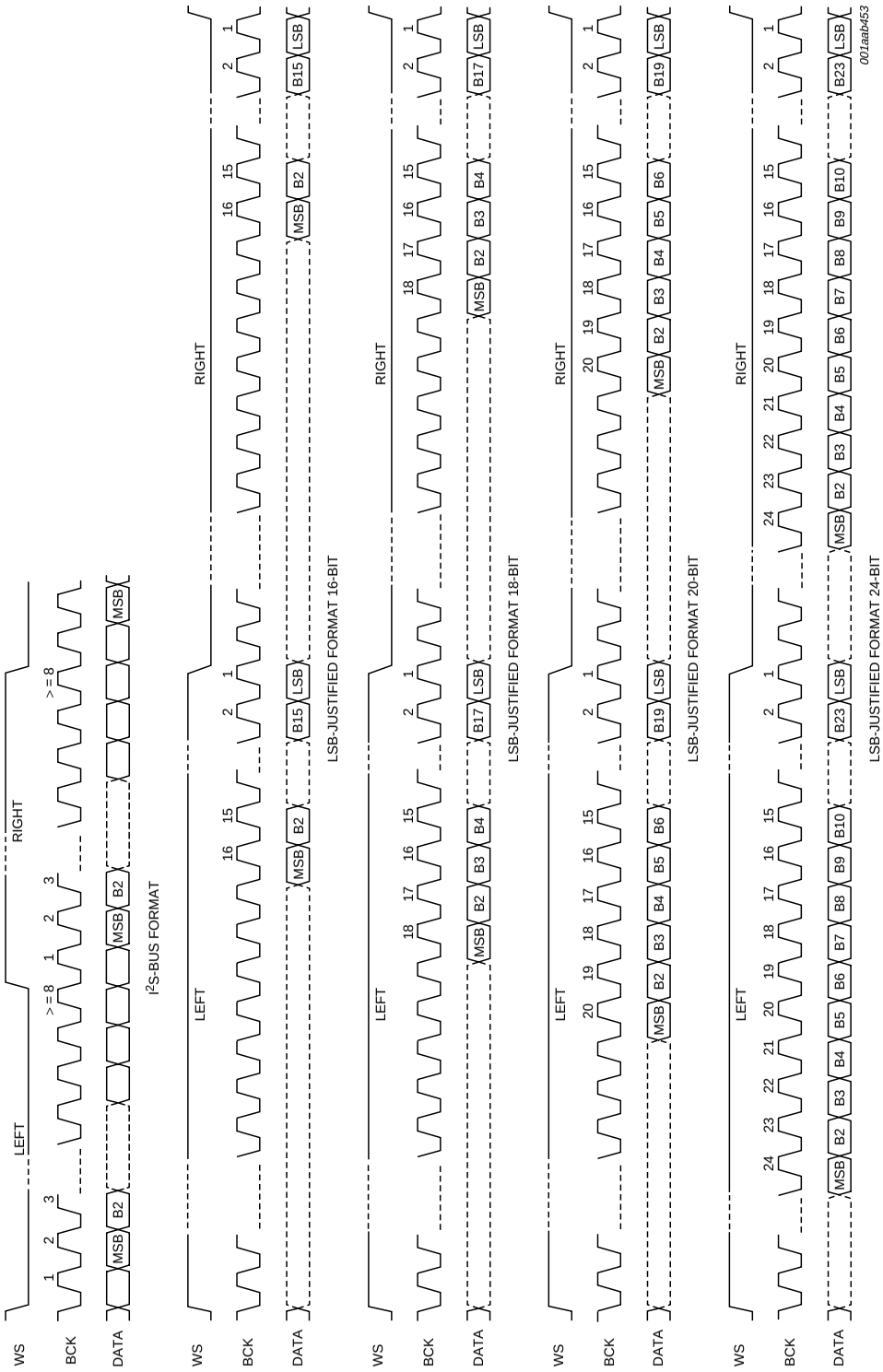
The word select from the SPDIF input decoder is routed to the CGU. This makes it possible to lock the audio PLL to the incoming SPDIF stream.

7.12 I^2S-bus

The supported audio formats for the control modes are:

- I^2S-bus
- LSB-justified, 16-bit
- LSB-justified, 18-bit
- LSB-justified, 20-bit
- LSB-justified, 24-bit (only for the output interface).

The bit clock BCK can be up to $128f_s$, or in other words the BCK frequency is 128 times the WS frequency or less: $f_{BCK} \leq 128f_{WS}$.



The WS edge must coincide with the negative edge of the BCK at all times for proper operation of the digital I/O data interface.

Fig 5. Serial interface input and output formats

7.12.1 I²S-bus inputs

Two I²S-bus inputs are provided, one of the two has dedicated pins, the second is multiplexed using pin GPIO8 to GPIO10.

The I²S-bus inputs can be used in slave and master mode. In slave mode an external I²S-bus source generates the bit clock and in master mode the SAA8200HL generates the bit clock. In slave mode the bit clock arrives on pad I2SIN_x_BCK and is led to the CGU input xt_I2SIN_x_BCK. This input should be switched directly to the CGU output I2SIN_x_BCK which delivers the bit clock for the I²S-bus blocks.

In slave mode the audio PLL needs to lock on the incoming source. This can best be done on the bit clock or on the word select. The bit clock is the preferred source because of its higher frequency. The audio PLL has problems with locking on frequencies below 100 kHz. If the ratio between the bit clock and the sample frequency is not known, the source word select can be used. The digital audio source will put out the data and the word select on the negative edge of the bit clock and these will be sampled by the I²S-bus block on the positive edge of the bit clock.

7.12.2 I²S-bus outputs

Two I²S-bus outputs are provided, both have dedicated data pins but the word select and bit clock for both outputs are shared.

Depending on the application the source of the audio PLL could have an other input, then the fractional dividers should be programmed to account for the difference in clock frequency.

The I2S_OUT can only be used in master mode. For this reason the output enable of the I2S_OUT_WS and I2S_OUT_BCK pads is always active in functional mode. The bit clock generated by the CGU is inverted with respect to the word select, such that word select changes on a negative edge of the bit clock.

7.13 Time stamp counters

A time stamp counter has been included to allow the software to get an indication of the audio clocks.

The time stamp counter output is hardwired to seven EPICS7B input registers. Each input register will be latched by another strobe signal. These strobe signals are generated by the audio interfaces I2SIN, SPDIF, ADC, I2SOUT and DAC. This way each sample of each audio source and sink can be labeled with a time stamp. The time stamp increases by one every DSP clock tick, and will wrap-round at value ($2^{24} - 1$).

7.14 DMA controller

The purpose of the external DMA controller block is to share the external DMA channel of the EPICS7B DSP sub system between a number of external peripherals: the serial radio interface, the Reed-Solomon codec, the I^2C-bus M/S and MPI. The controller needs to arbitrate between those blocks.

Features:

- Interface between external DMA hardware blocks and the EPICS7B DSP subsystem
- Allows hardware blocks to read/write directly to X-, Y-, P-memory and to internal DSP registers.
- Supports single word memory access and memory block transfers of programmable length.
- Signals block transfer ready per requesting hardware device
- Arbiter priority schedule between four requesting sources (SRI, I^2C-bus M/S, RSC and MPI).
- Each requesting hardware block has its own start address and block transfer size register
- Dispatches acknowledges and keeps track of progress of each block transfer
- Signals block transfer ready per requesting hardware device.

7.15 I/O configuration

The input/output configuration (IOCONF) is designed to provide developers a set of registers. This can be used for configuration of various on chip components especially a pad multiplexer.

The IOCONF block is used to provide individual control and visibility for a set of pads. In conjunction with a set of pad multiplexers, individual pads can be switched either in normal operation mode, or in GPIO mode. In GPIO mode, a pad is fully controllable. Through the IOCONF, individual pad levels can be observed in both normal and GPIO modes.

Functional pads can be grouped into function blocks.

All output values in a function block can be set simultaneously by accessing a single register. Changing modes for all pads within a function block requires at most two register access. All input values in a function block can be read simultaneously by accessing a single register. Input values are not registered and always read directly from the pad's input driver regardless of the mode of the pad.

For each function block there are two registers holding the control mode. MODE bit 1 leaves the IOCONF inverted as it is intended to be used as inverted (output-) enable. Each register can be written and read, has configurable pad names per bit (maximum 32) and provides set and clear access methods (SET/CLEAR bit when '1'), and configurable reset value. Configurable pad names are provided in order to enhance readability and consistency of both HDL and generated C header file.

Table 13: Mode settings

MODE[1:0]	Pin multiplexer mode
00	GPIO; high-impedance
01	normal operation; controlled by subsystem
10	GPIO drive LOW
11	GPIO drive HIGH

7.16 VPB1 bridge

This section describes the interfaces and function of the VPB1 bridge. The VPB1 bridge acts as a bridge between the UART and the EPICS7B DIO interface. Two bridges are used; one to connect to several slow blocks and an additional one specifically for the universal synchronous receiver transmitter, which is commonly used to implement a serial interface. In any case where a device needs a low overhead, standard, low performance interface, a UART can be used. The UART includes advanced features like a fractional clock divider.

Table 14: VPB1 bridge interface description

Base address	Offset	Key	Description
0x0000			UART
	0x0000	UART_RBR	receive FIFO
	0x0000	UART_THR	transmit FIFO
	0x0004	UART_IER	interrupt enable register
	0x0008	UART_IIR	interrupt ID register
	0x0008	UART_FCR	FIFO control register
	0x000C	UART_LCR	line control register
	0x0010	UART_MCR	modem control register
	0x0014	UART_LSR	line status register
	0x0018	UART_MSR	modem status register
	0x001C	UART_SCR	scratch pad register
	0x0000	UART_DLL	divisor latch LSB
	0x0004	UART_DLM	divisor latch MSB
	0x0028	UART_FDR	fractional divider register

7.17 UART configuration

The UART interface is used to be implemented as a serial interface to, for example a modem and is compatible with the industry standards 16650 UARTs.

No full modem interface is included, only the CTS and RTS modem signals are available.

The UART interface can also be configured as an IrDA (InfraRed Digital Association) SIR (Serial InfraRed) interface, which has a pulse and polarity compliancy with the IrDA Version 1.0 Physical Layer Specification.

7.18 Audio configuration

The audio configuration block gives access to the following system settings:

- I²S-bus input/output format settings
- Status of SPDIF module
- SPDIF interrupt request
- SDAC control and status registers
- SADC control and status registers
- Interrupt request to EPICS7B; with automatically clearing register
- Power-down of the multi-channel 10-bit control ADC
- DC-to-DC converter output voltage settings
- DC-to-DC clock-stable indicator.

7.19 Audio input

7.19.1 ADC analog front-end

The analog front-end of the ADC consists of one stereo ADC with a selector in front of it. Using this selector one can either select the microphone input with the microphone amplifier (LNA) with a fixed 30 dB gain or the line input. The microphone input as well as the line inputs have a Programmable Gain Amplifier (PGA) that allows gain control from 0 dB to 24 dB in steps of 3 dB.

The input impedance of the PGA (line in) is 12 kΩ, for the LNA this is 5 kΩ.

7.19.1.1 Applications and Power-down modes

The following Power-down and functional modes are supported:

- Power-down mode in which the current consumption is very low (only leakage currents). In this mode there is no reference voltage at the line input.
- Line-in mode, in which the PGA can be used.
- Microphone mode in which the rest of the non-used PGAs and ADCs are powered down. In this mode the mono microphone signal can be sent to both left and right input of the decimation filter. This is done with a separate multiplexer in front of the decimation input. This multiplexer is controlled by bit SEL_MIC in the I²C-bus control interface.
- Mixed PGA and LNA mode with one line-in and one microphone input.

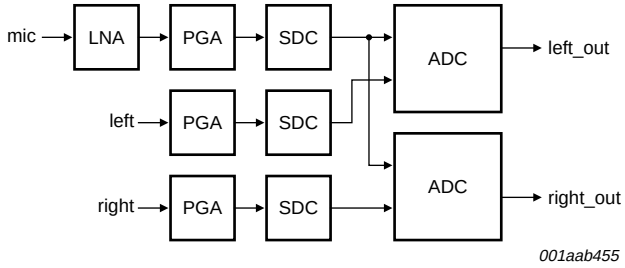


Fig 6. Analog front-end

7.19.1.2 LNA

LNA, a Low Noise microphone Amplifier with nominal gain of 30 dB.

7.19.1.3 PGA

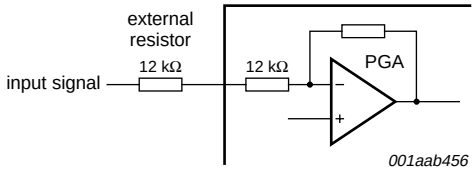
The input signal is amplified with a gain set by control bits CTRL[3:0]. The resulting signal will be available at V_{out}. If control bit CTRL3 = 1 the gain is set to 24 dB independent of the other bits. If CTRL3 = 0 the gain is set for other (lower) settings. The PGA is based on an inverting amplifier architecture. The feedback resistance exists of a resistor string. By switching between different resistors with the use of a 4-bit digital decoder the gain of the amplifier can be modified. The gain can be set in steps of 3 dB from 0 dB up to 24 dB (see Table 15). The PGA is designed to handle a nominal 1 V (RMS) input level. A systematic gain of −1.94 dB is added to accommodate the 800 mV (RMS) input level of a single-to-differential converter that is normally connected to the PGA output. The power-down signal is controlled by the digital core of the SAA8200HL.

Table 15: PGA gain settings

CTRL3	CTRL2	CTRL1	CTRL0	Gain
0	0	0	0	0 dB
0	0	0	1	3 dB
0	0	1	0	6 dB
0	0	1	1	9 dB
0	1	0	0	12 dB
0	1	0	1	15 dB
0	1	1	0	18 dB
0	1	1	1	21 dB
1	X	X	X	24 dB

7.19.1.4 Applications with 2 V (RMS) input

For the Line-in mode it is preferable to have 0 dB and 6 dB gain setting in order to be able to apply both 1 V (RMS) and 2 V (RMS) (using series resistance). For this purpose a PGA is used which has 0 dB to 24 dB gain with 3 dB steps.



Input signal is 2 V (RMS); V_{DD} = 3 V.

Fig 7. ADC front-end with PGA (line-in input)

In applications in which a 2 V (RMS) input signal is used, a 12 kΩ resistor must be used in series with the input of the ADC. This forms a voltage divider together with the internal ADC resistor and ensures that only 1 V (RMS) maximum is input to the SAA8200HL. Using this application for a 2 V (RMS) input signal, the switch must be set to 0 dB. When a 1 V (RMS) input signal is input to the ADC in the same application, the gain switch must be set to 6 dB.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 16; the power supply voltage is assumed to be 3 V.

Table 16: Application modes using input gain stage

Resistor 12 kΩ	input gain switch	maximum input voltage
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

7.19.1.5 SDC

The Single-to-Differential Converter (SDC) consists of an inverting amplifier and a filter network. The input is DC coupled, which means that decoupling must be done in front of this module in case the input signal has a different common mode level than the SDC. For optional biasing conditions, the SDC requires a sourcing bias current (into an NMOS transistor) that is preferably proportional to the analog supply voltage.

7.19.2 Decimation filter (ADC)

The decimation from 128fs is performed in two stages (see Figure 8). The first stage realizes sin(x)/x characteristics with decimation factor of 16. The second stage consists of three half-band filters, each decimating by a factor of 2. The filter characteristics are shown in Table 17.

Table 17: Filter characteristics

Description	Conditions	Value	Unit
Decimation filter			
Pass band ripple	up to $0.45f_s$	±0.02	dB
Stop band	from $0.55f_s$	−60	dB
Overall gain	DC	3	dB
Dynamic range	up to $0.45f_s$	140	dB
Droop	at $0.45f_s$	−0.18	dB
DC blocking filter 1			
Pass band ripple		none	dB
Pass band gain		0	dB
Droop	at $0.00045f_s$	0.5	dB
DC attenuation		> 40	dB
Dynamic range	up to $0.45f_s$	> 110	dB
DC blocking filter 2			
Pass band ripple		none	dB
Pass band gain		0	dB
Droop	at $0.00045f_s$	0.031	dB
DC attenuation		> 40	dB
Dynamic range	up to $0.45f_s$	> 110	dB

Table 17: Filter characteristics *...continued*

Description	Conditions	Value	Unit
Interpolation filter			
pass band ripple	up to $0.4535f_s$	±0.02	dB
stop band	from $0.5465f_s$	−72	dB
gain	pass band	−1.1	dB
dynamic range	up to $0.4535f_s$	>143	dB

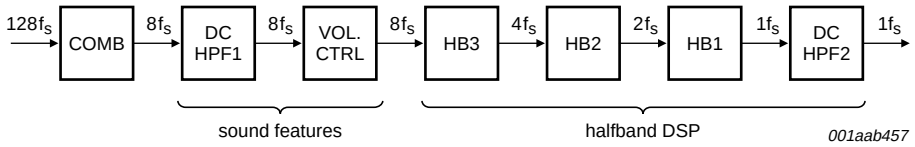


Fig 8. Decimator data path

7.19.2.1 Volume control

The decimator is equipped with a digital volume control. This volume control is separate for left and right and can be set via the SADC_CTRL_DECI register. The range is from +24 dB down to −63 dB and mute in steps of 0.5 dB.

7.19.2.2 DC blocking filter

Two optional 1st order Infinite Impulse Response (IIR) high-pass filters are provided to remove unwanted DC components from the input (DC offset, DC dither) and/or volume control output to avoid clipping when using large gain settings. These filters may be bypassed by setting bits EN_DCFILTI (SADC_CTRL_DECI[20]) and/or EN_DCFILTO (SADC_CTRL_DECI[19]) to a logic 0, which is necessary when fast settling of the decimator is required.

On recovery from power-down or after a reset, the parallel output data on bits dout_l[23:0] and DOUT_R[23:0] is held at logic 0 until valid data is available from the decimation filter. This time depends on which of the DC-blocking filters is selected and if the ENABLE bit of the delay timer is ON (EN_DELAY_DBLIN = SADC_CTRL_DECI[21]):

- EN_DELAY_DBLIN OFF:

  t = 0 s
- DC filter 1 is off, DC filter 2 is off and EN_DELAY_DBLIN is on:

  $t = 44/f_s$; t = 1 ms at f_s = 44.1 kHz
- DC filter 1 is ON, DC filter 2 is OFF and EN_DELAY_DBLIN is ON:

  $t = 17066/f_s$; t = 387 ms at f_s = 44.1 kHz
- DC filter 2 is ON and EN_DELAY_DBLIN is ON:

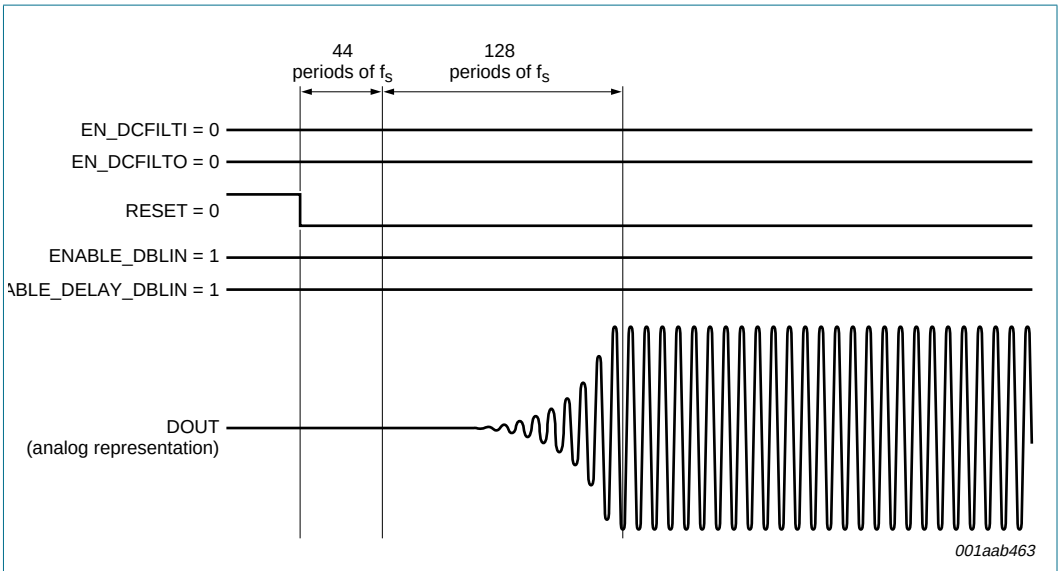
  $t = 67473/f_s$; t = 1.53 s at f_s = 44.1 kHz.

7.19.2.3 Soft start-up after reset

After a reset of the decimation filter and if bit EN_DBLIN (SADC_CTRL_DECI[21]) is a logic 1, the output gain of the decimator is increased from mute to −63.5 dB and at a rate of 0.5 dB per f_s period to 0 dB (dB linear) to avoid harsh audible plops. The time required for a complete soft start-up if bit EN_DBLIN is a logic 1 for 128 f_s periods. This time is without the time required if bit EN_DELAY_DBLIN (SADC_CTRL_DECI[21]) is a logic 1, e.g. if bit EN_DBLIN and bit EN_DELAY_DBLIN are a logic 1, bit EN_DCFILTI and bit EN_DCFILTO are logic 0 the total time required is (44 +128) f_s periods (see Table 18). The decimator soft start-up function is illustrated in Figure 9.

Table 18: Required time after reset

EN_DELAY_DBLIN	EN_DBLIN	EN_DCFILTI	EN_DCFILTO	Required time
0	0	X	X	0 s
0	1	X	X	128 periods of f_s
1	0	0	0	44 periods of f_s
1	0	1	0	17066 periods of f_s
1	0	X	1	67473 periods of f_s
1	1	0	0	(44 + 128) periods of f_s
1	1	1	0	(17066 + 128) periods of f_s
1	1	X	1	(67473 + 128) periods of f_s



For readability, the parallel output data is shown in its analog representation.

Fig 9. Soft start-up function

7.19.2.4 Signal polarity

The polarity of the output signal is controlled by bit EN_POL_INV (SADC_CTRL_DECI[17]). When this bit is enabled, the polarity of the output data is inverted.

7.19.2.5 Mute

When the left and right channel of the decimator are muted (bit EN_MUTE is a logic 1), the gain in the decimator is decreased linearly to –63.5 dB with a final step to mute at a rate of 0.5 dB per f_s period (dB linear). This is done to avoid harsh audible plops. The time required for a complete mute depends on the initial gain setting. Maximum required time is 256 f_s periods. When a complete mute is achieved for both left and right channels, the bit MUTE_STATE (SADC_CTRL_DECO[0]) is made logic 1. When the channels are de-muted (bit EN_MUTE is a logic 0) the gain of the decimator is increased at the same rate until the programmed gain setting is achieved.

7.19.2.6 Overflow detection

The output signal is used to indicate whenever the output data, in either the left or right channel, is larger than –1.16 dB of the maximum possible digital swing. When this condition is detected the overflow bit (SADC_CTRL_DECO[1]) is forced to a logic 1 for at least 512 f_s cycles (11.6 ms at f_s = 44.1 kHz) allowing even a slow microcontroller to poll this event. This time-out is reset for each infringement.

7.19.2.7 AGC function

The decimation filter is equipped with an Automatic Gain Control (AGC) block. This function is intended, when enabled, to keep the output signal at a constant level.

The AGC can be used for microphone applications in which the distance to the microphone is not always the same.

The AGC can be enabled via the control register (SADC_CTRL_DECI[23]). In this case it bypasses the digital volume control. Other features of the AGC, such as the attack, decay and target level can be set via the same register.

The DC filter in front of the decimation filter must be enabled when AGC is in operation, otherwise the output will be disturbed by the DC offset added in the ADC.

Table 19: AGC enable control

AGC_EN	AGC function
0	disabled, manual gain control via the left/right decimator volume control, (default)
1	enabled, with manual microphone gain settings via PGA

Table 20: AGC target level settings

AGC_LEVEL1	AGC_LEVEL0	AGC target level value (dB)
0	0	–5.5
0	1	–8.0
1	0	–11.5
1	1	–14.0

Table 21: AGC time constant settings

AGC_TIME2	AGC_TIME1	AGC_TIME0	AGC setting			
			44.1 kHz sampling		8 kHz sampling	
			Attack time (ms)	Decay time (ms)	Attack time (ms)	Decay time (ms)
0	0	0	11	100	61	551
0	0	1	16	100	88.2	551
0	1	0	11	200	61	1102
0	1	1	16	200	88.2	1102
1	0	0	21	200	116	1102
1	0	1	11	400	61	2205
1	1	0	16	400	88.2	2205
1	1	1	21	400	116	2205

7.20 Audio output

7.20.1 SDAC

The Stereo Digital-to-Analog Converter (SDAC) is a module with interpolation filters and noise shaper for low frequency applications such as audio and TV-audio. In this section the analog and digital part is described. The digital part consists of an interpolation filter that increases the sample rate from $1f_s$ to $128f_s$ and a third order noise shaper that runs on $128f_s$ or $256f_s$.

The inputs to the SDAC are two 24-bit parallel input words, left and right, and a synchronization signal (DIN_VALID) at f_s (f_s, the sample rate, is typically 44.1 kHz). The output is a stereo analog signal (VOUT_LINEL and VOUT_LINER).

7.20.1.1 Features of the SDAC

- 24-bit data path with 16-bit coefficients
- Full FIR filter implementation for all of the upsampling filter
- Digital dB-linear volume control in 0.25 dB steps
- Digital de-emphasis for 32 kHz, 44.1 kHz, 48 kHz and 96 kHz
- Selection for the $2f_s$ to $8f_s$ upsampling filter characteristics (sharp/slow-roll-off)
- Support for $2f_s$ and $8f_s$ input signals:
  - $1f_s$ with full feature support, being de-emphasis, master volume control and soft mute
  - $2f_s$ input with master volume and mute support: required for double speed mode
  - $8f_s$ input no features supported. This is intended for DSD support (grabbing data at $8f_s$ from an external DSD unit)
- Soft mute with a raised cosine function
- Controlled power-down sequence comprising a raised cosine mute function followed by a DC ramp down to zero to avoid audible plops or clicks
- Integrated digital silence detection for left and right with selectable silence detection time
- Polarity control

- Simple switched resistors architecture
- Data-weighted averaging technique reducing distortion
- Large supply voltage range (0.8 V to 3.6 V)
- Low noise (N > 100 dBA).

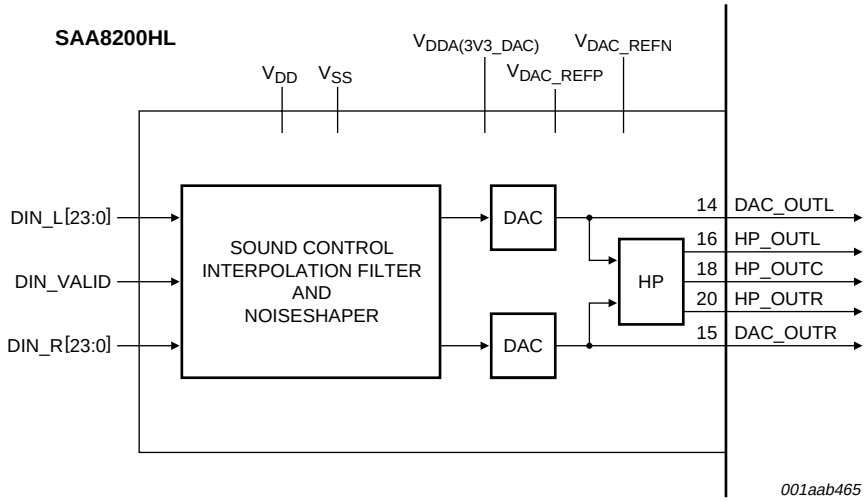


Fig 10. Block diagram of the SDAC

7.20.1.2 Functional description

The SDAC comprises the following functions:

- Sound feature processor
- Digital upsampling filter
- Noise shaper
- DAC.

Digital de-emphasis can be set by a 3-bit control bus (bits CTRL_INTI[18:16]) for the range of sample frequencies available (32 kHz, 44.1 kHz, 48 kHz and 96 kHz). The de-emphasis filters are only in the signal path for normal speed mode (data input at $1f_s$).

In the interpolation filter a three stage linear digital volume control is provided with a range from 0 dB to −89 dB and −∞ dB. Down to the attenuation of −50 dB the step size equals 0.25 dB, from −50 dB to −83 dB it equals 3 dB and the last step to −89 dB is one of 6 dB. The attenuation for the left channel is controlled by bits CTRL_INTI[15:8]; the attenuation for the right channel is controlled by bits CTRL_INTI[7:0].

When the left and right channels of the interpolator are muted (bit CTRL_INTI[19] = 1), the gain in the interpolator is decreased to −∞ dB conforming to a raised cosine function to avoid harsh audible plops (soft mute). This mute function is completed after a period of 128 samples in normal mode i.e. 2.9 ms at f_s = 44.1 kHz. When a complete mute is achieved for both left and right channels, the bit CTRL_INTO[0] is made a logic 1. The interpolator mute function is illustrated in Figure 11.

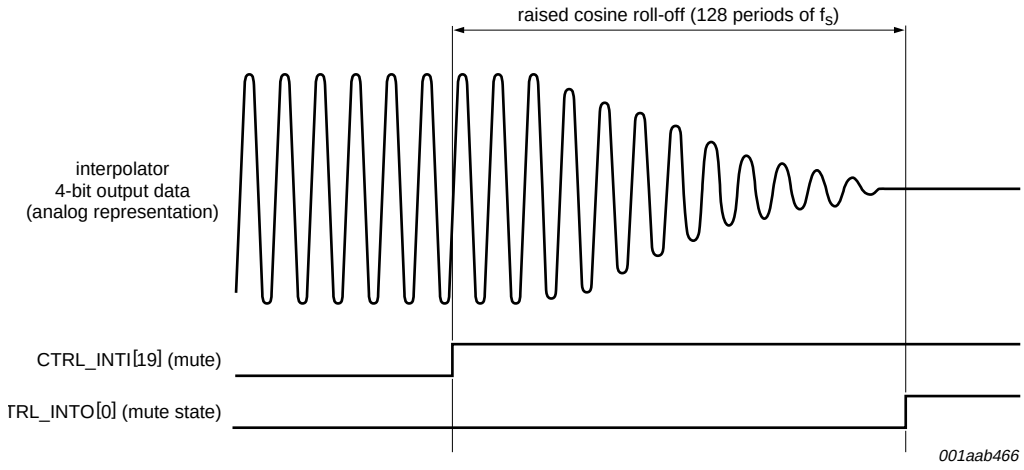


Fig 11. Interpolator mute signals

7.20.1.3 Power-down

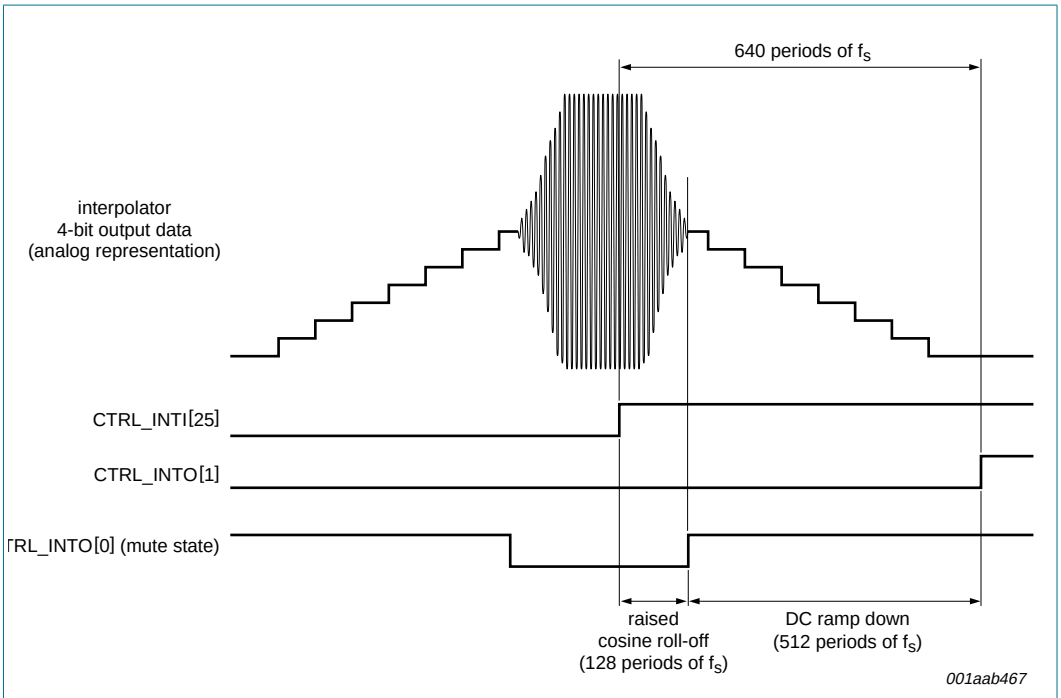


Fig 12. Interpolator power-up and power-down sequence

When the interpolator is powered down (bit CTRL_INTI[25] = 1), the gain in the interpolator is decreased to −∞ dB to conform to a raised cosine function. This is followed by a DC ramp down to zero output data (000000h). The slope of this DC ramp can be set by bit CTRL_INTI[24] to either 512 f_s periods (default) or 1024 f_s periods. The power-up follows the reverse procedure, a DC ramp up to mid scale plus DC dither (2 to [6 + 2] to [10 + 2] to 17) followed by a gain increase to conform to a raised cosine function. Total

time required for a full power-up or power-down equals 128 f_s periods (raised cosine function) plus 512 f_s periods (DC ramp up/down) making 640 f_s periods or 14.5 ms for f_s = 44.1 kHz. The power-up and power-down function is illustrated in Figure 12.

7.20.1.4 Silence detection

The silence detection circuit counts the number of digital input samples equal to zero. It is enabled by the control bit CTRL_INTI[30]. The number of zero samples before signalling silence detected (bit CTRL_INTO[3] for left channel and bit CTRL_INTO[2] for right channel) can be set by bits CTRL_INTI[29:28]. This feature is not used to control the SDAC, it is simply a feature that can be used in the system.

7.20.1.5 Polarity control

The stereo output signal polarity of the C18INT can be changed by setting the CTRL_INTI[26] to logic 1. Note that this single control bit affects both channels.

7.20.1.6 Digital upsampling filter

The interpolation from $1f_s$ to $128f_s$ is realized in four stages:

- The first stage is a 99-tap half band filter (HB) which increases the sample rate from $1f_s$ to $2f_s$ and has a steep transition band to correct for the missing inherent filter function of the SDAC.
- The second stage is a 31-tap FIR filter which increases the data rate from $2f_s$ to $8f_s$, scales the signal and compensates for the roll-off caused by the sample-and-hold function prior to the noise shaper. For this filter three sets of coefficients can be chosen realizing three different transfer characteristics.
- The third stage is a simple hardware linear interpolator (LIN) function that increases the sample rate from $8f_s$ to $16f_s$ and removes the $8f_s$ component in the output spectrum. The main reason for upsampling to $16f_s$ is the fact that the SDAC only has a first order roll-off function.
- The fourth and last stage is a sample-and-hold function increasing the sample rate from $16f_s$ to a selectable $128f_s$ or $256f_s$, depending on the actual input data rate. For input sample rates between 8 kHz and 32 kHz the noise shaper and DAC must run on $256f_s$ instead of the typical $128f_s$ to avoid a significant noise increase in the audible frequency band of 0 kHz to 20 kHz.

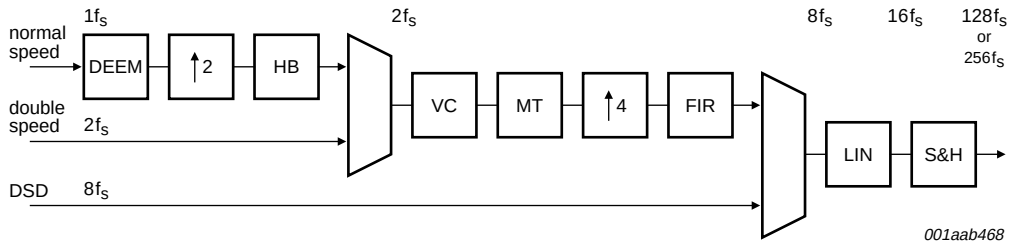


Fig 13. Interpolator data path

The SDAC has three modes of operation which are set by the control input bits CTRL_INTI[21:20]:

- Normal $1f_S$ input mode used for input data rates between 8 kHz and 96 kHz using sharp filter roll-off. De-emphasis (DEEM), volume control (VC) and mute (MT) functions are all available in this mode
- $2f_S$ input mode which may be used as:
  - Double speed input when the data rate is between 96 kHz and 200 kHz
  - A means to get slow roll-off by skipping the first half band filter (HB). In this mode the de-emphasis (DEEM) is not available
- $8f_S$ or DSD input mode, in which case the input is obtained form an external DSD block. De-emphasis (DEEM), volume control (VC) and mute (MT) features are unavailable in this mode.

7.20.1.7 Noise shaper

The 3rd-order noise shaper operates at either $128f_S$ or $256f_S$ depending on the mode of operation defined by bits CTRL_INTI[23:20]. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved at low frequencies. The noise shaper output is converted into an analog signal using a 4-bit switched resistor digital-to-analog converter.

7.20.1.8 SDAC

The 4-bit SDAC is based on a switched resistor architecture which is merely a controlled voltage divider between the positive and negative reference supplies *VREF_DACP* and *VREF_DACN*. The 4-bit input data from the noise shaper is first decoded to a 15 level thermometer code controlling the 15 taps of the converter. Added to the decoding is a selectable Data Weighted Averaging (DWA) technique which guarantees that there is no correlation between the input signal and the resistors used for that input signal.

After decoding and DWA the buffers connect the resistors to either the *VREF_DACP* or *VREF_DACN*. In doing this the reference voltage will be divided depending on the input signal. The result is an analog output voltage with a rail-to-rail maximum output swing. The output impedance of this DAC is approximately 1 kΩ. By applying an external capacitor of 3.3 nF to the line output (VOUTLINEL or VOUT_LINER) a low pass post filter is introduced with a −3 dB roll off at 48 kHz (dimensioned for f_S = 44.1 kHz). This will thus reduce the 3rd order noise shaped output spectrum of the DAC to a noise spectrum increasing with 2nd order. The value of this capacitor depends on the actual sample frequency used.

7.20.1.9 Data weighting averaging

The SDAC features two DWA algorithms which can be selected independently for the left (bit CTRL_DAC[1]) and right (bit CTRL_DAC[0]) channels. By setting these bits to a logic 0 the uni-directional DWA algorithm is chosen which is best suited for good S/N figures. By setting these bits to a logic 1 the bi-directional DWA algorithm is chosen which is best for low distortion.

7.20.2 Headphone

7.20.2.1 Headphone driver

The headphone driver can deliver 22 mW (at 3.0 V power supply) into16 Ω load.

The headphone driver does not need external DC decoupling capacitors because it can be DC-coupled with respect to a special headphone output reference voltage. This saves two external capacitors. Changes in the load on the DAC outputs influence the output of the headphone. This is because the headphone inputs are directly connected to the DAC outputs.

7.20.2.2 Headphone Limiter

To protect the headphone amplifier from serious damage due to short-circuiting of the outputs (e.g. during the connection of a headphone jack plug) a current limiter is incorporated. The activation of this current limiter is signaled by individual logic clip signals (*CLIP_L*, *CLIP_R* and *CLIP_C*). The level at which the current limiter is activated can be set to four different levels for each amplifier.

The current level to which the output stage is limited can be set with the bits SET_LIMITER_L/R/C[1:0] inputs from 80 mA to 140 mA for the left and right channels and from 180 mA to 240 mA for the common channel (see Table 22). The maximum current for the common ground channel is larger (double on average) as this channel must be able to sink and source the left and right channel output currents. When the current through the output stage exceeds the programmed current level, the monitor bit CLIP_L, CLIP_R or CLIP_C is set to a logic 1 and the output stage is shut down.

These values are based on the worst case situation of two in-phase full scale input signals of 1.0 V (RMS) and a minimum headphone impedance of 16 Ω. This results in left and right channel peak output currents of 1.41 V / 16 Ω = 88.4 mA and a common ground peak output current of 2 × 88.4 mA = 176.8 mA. The maximum current that is actually flowing in the common ground amplifier is always the sum of the left and right channel maximum currents.

Table 22: Output current limiter settings

SET_LIMITER_L[1:0], SET_LIMITER_R[1:0], SET_LIMITER_C[1:0]	Maximal output current	
	Left and right channel	Common channel
00	OFF	OFF
01	100 mA (default)	200 mA (default)
10	120 mA	220 mA
11	140 mA	240 mA

7.21 DC-to-DC converter

The SAA8200HL needs two supply voltages, 3.3 V for analog functions and 1.7 V for digital functions. For normal operation one or two batteries of 1.5 V will be used as an energy source, from which the DC-to-DC converter must generate the required voltage levels, see Figure 14. Two inductive DC-to-DC converters will be used when the chip is battery operated. The V_{DDE} pins are externally connected to pin DCDC_OUT3V3, The V_{DDI} pins are connected to pin DCDC_OUT1V8. When the SAA8200HL is supplied from USB, the outputs of the DC-to-DC converters will be overruled by two linear regulators. In that case the supply voltages will be 3.3 V and 1.8 V. This is independent from the USB voltage (4.0 V to 5.5 V) so a reference circuit is needed.

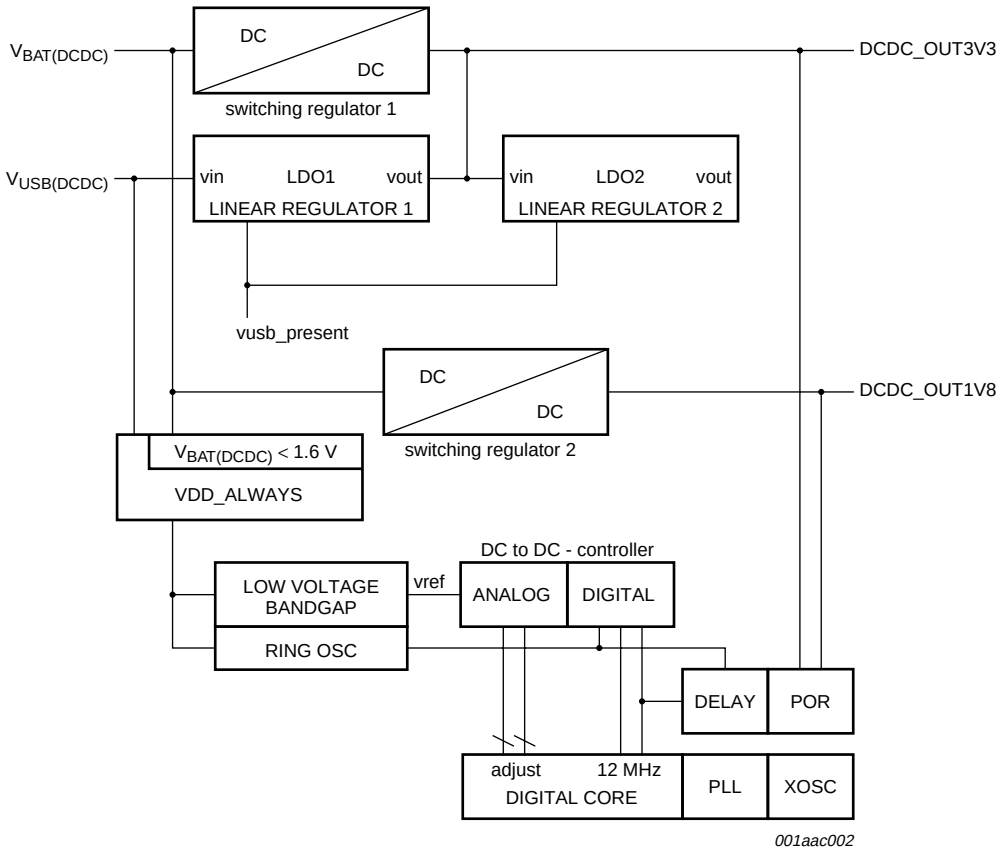


Fig 14. DC-to-DC converter block schematic

During the start-up sequence the DC-to-DC controller uses the RING OSC to control the switching regulators. After start-up the 12 MHz from the digital core is fed to the DC-to-DC controller. In battery operation mode the output voltage DCDC_OUT1V8 and DCDC_OUT3V3 can be controlled by three adjust bits. Care has to be taken with signal levels (level shifters) and the start-up and shut-down from battery to USB and from USB to battery transitions. A delay circuit uses RING OSC clocks to generate a delay of about 1 ms for the RESET_B pulse. In USB mode the delay can be generated otherwise.

The DC-to-DC converter has to operate from a single or from two batteries. This has no consequence for the first DC-to-DC converter, this is always an up converter. In case a single battery is used the second converter is also an up converter but it is a down

converter when two batteries are used. Pin DOWNSEL selects the type of converter and thus how many batteries are connected. If pin DOWNSEL is HIGH the SAA8200HL operates from two batteries and the second DC-to-DC converter is a down converter. If pin DOWNSEL is LOW the SAA8200HL operates from one battery and the second DC-to-DC converter is an up converter, see Figure 15

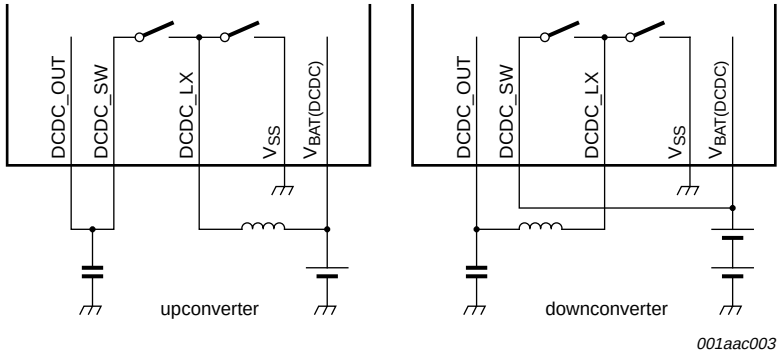


Fig 15. Up and down converter topology

7.21.1 Controller

The controller consists of an analog and a digital part. The analog part compares the output voltage VOUT[1,2] with a programmable voltage window in eight possible adjust settings. The digital part computes the switching time such that the output voltage stays within this window. In the analog part is one restive divider with a programmable output, see Figure 16.

Together with reference voltage V_{ref} the voltage window is defined. The output of the resistive divider is compared to the reference voltage with comparators with added offset. The outputs VTH (voltage too high) and VTL (voltage too low) are based on the comparison.

When VTH is asserted means that VIN is higher than the upper limit of the window, indicating to the digital part of the controller that the output voltage must be lowered. When VTL is asserted it indicates that VIN is lower than the lower limit of the window, indicating to the digital part of the controller that the output voltage must be higher. When neither is asserted, VIN is between the lower and upper limit of the window, indicating to the digital part of the controller that the output voltage is in the limits of the window and it does not have to change the output voltage. This is the normal mode of operating and is called continuous mode because the coil continuously carries current.

In continuous mode the digital part of the controller generates switching cycles at a fixed frequency. During the first part of such a cycle (t1) switch 1 will be closed and switch 2 will be opened, during the last part of the cycle (t2) switch 2 will be closed and switch 1 will be opened. The length of t1 as a fraction of the cycle time is set such that the required output voltage is generated. When the output voltage runs outside the window this length is updated such that the output voltage falls within the window again.

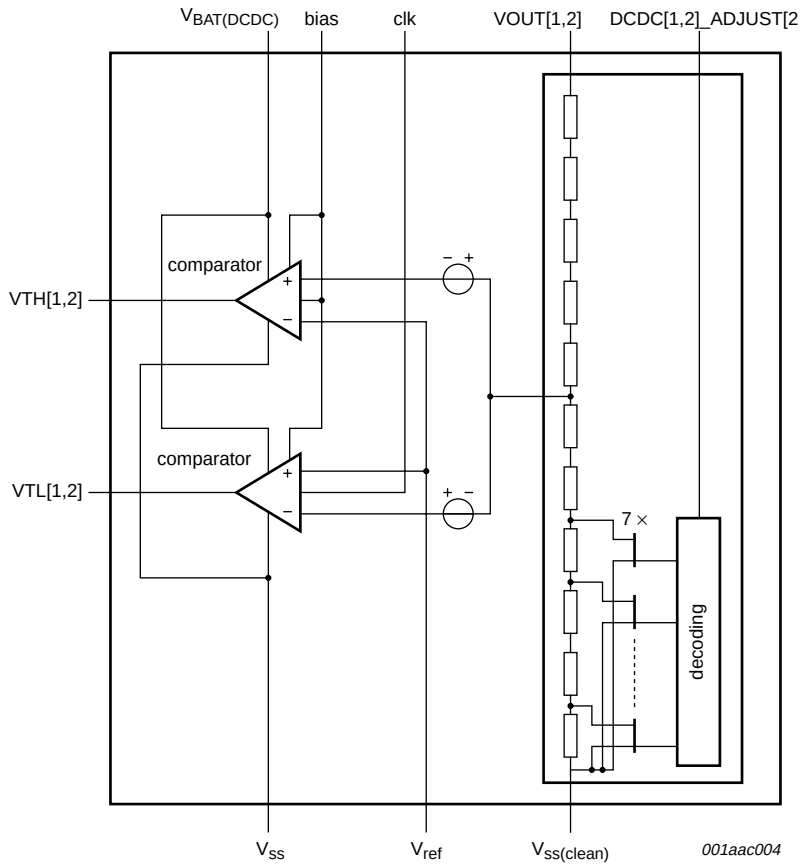


Fig 16. Analog part of the controller

See Figure 17 for a coil current cycle in continuous mode. The average coil current is equal to the average current demanded by the load. The lengths of t1 and t2 are determined by the battery voltage and the output voltage of the DC-to-DC converter. The output voltage is allowed to vary within a certain window. This means that there will be a voltage ripple with a frequency that is largely correlated to the frequency content of the load current. The peak-to-peak amplitude of the ripple will be more or less equal to the window height. There will be ripple at the switching frequency too, this is mainly caused by the fact that the coil current will run through parasitic resistances of the load circuit.

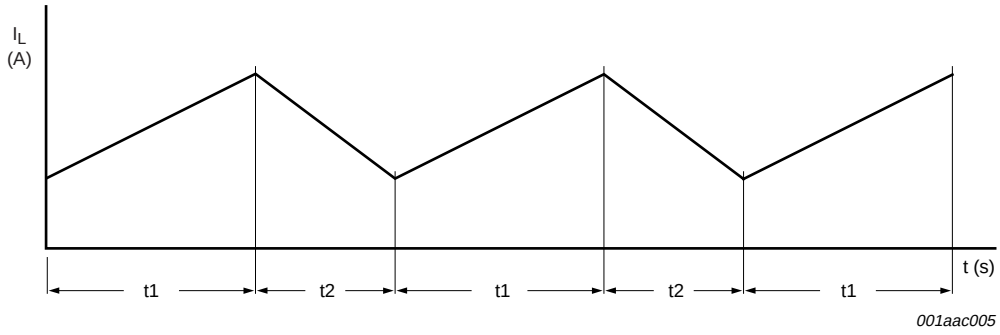


Fig 17. Coil current cycle in continuous mode

See Figure 18 for a coil current cycle in ramp-up mode. The controller enters this mode when there is an increased demand for energy (voltage falls to below the lower limit). By a one-time increase of t1 the coil current is increased to a higher average.

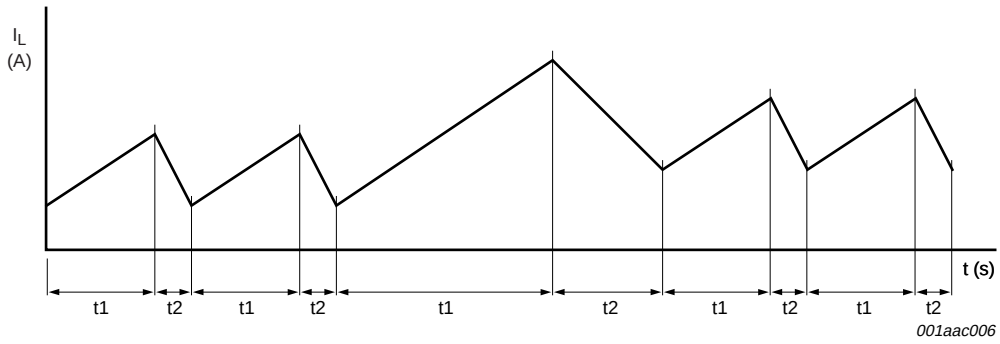


Fig 18. Coil current cycle in ramp-up mode

See Figure 19 for a coil current cycle in discontinuous mode. In this mode the coil current does not flow continuously. Dependent on energy demand a cycle is generated. So instead of changing the duty cycle as in continuous mode the frequency is changed. This mode is intended for low power operation. During the first phase the battery ramps up the current from zero and during the second phase it is ramped down to zero by the load. The coil current is made to decrease to zero by opening both switches shortly before the current reaches zero. The moment when the switches are to be closed is learned from the behavior of the DC-to-DC converter in continuous mode.

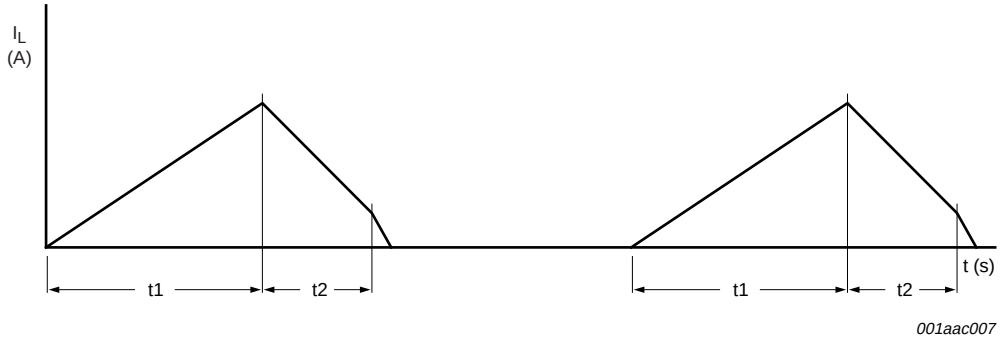
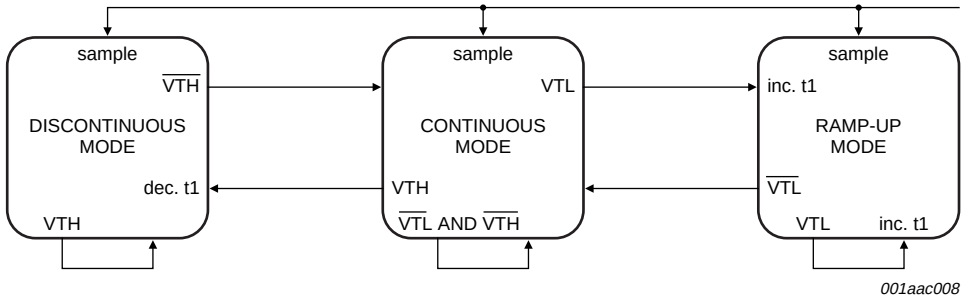


Fig 19. Coil current cycle in discontinuous mode

The digital part of the controller consists of a state machine that enables the controller to switch modes. A decision to jump to a different state is taken on the basis of the outputs of the analog part. As a result of some of the jumps, the duration of the first phase of the cycle is increased or decreased, see Figure 20.



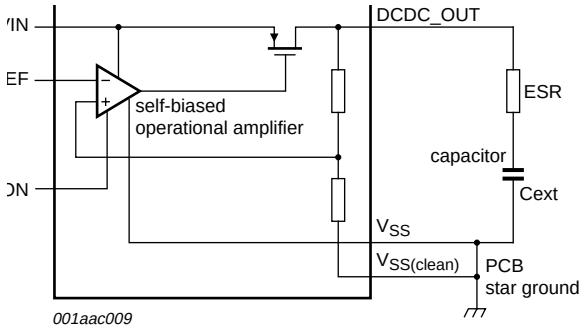
The controller will be in discontinuous mode if adjusted DCDC_OUT1V8 ≤ $V_{BAT(DCDC)}$.

No forward diode from $V_{BAT(DCDC)}$ to DCDC_OUT1V8 allowed.

Fig 20. Digital part of the controller

7.21.2 Linear regulators

The linear regulators will be implemented as Low Drop voltage Output (LDO) regulators for a fixed output voltage, see Figure 21. One LDO has to handle input signals in the order of 5.0 V so a special construction with thick gate oxide is needed. The other LDO handles an input signal of 3.3 V thus a normal construction with thick gate oxide is sufficient. For the loop stability the choice is made that the dominant pole lies externally. The series resistance of Cext (ESR) gives a zero and degrades the stability and thus limited to a maximum value. For an accurate output voltage a reference voltage is needed. This voltage can be made with a band gap circuit. A fraction of the output voltage is fed back to the operation amplifier. In Stop mode the LDOs should be stable to deliver only small currents.



The on terminal is connected to VUSB_PRESENT.

Fig 21. Principle of LDO

7.21.3 Timing specification

7.21.3.1 Play and stop with battery supply

A negative edge at pin DCDC_PLAY starts the DC-to-DC converter, see Figure 22. When minimum supply voltages are detected for DCDC_OUT1V8 and DCDC_OUT3V3 by the POR, the signal SUPPLY_OK is made logic 1. After about 1 ms signal RESET_B becomes logic 1. When the supply voltages are correct the voltages to the application control switches rises from $V_{BAT(DCDC)}$ to DCDC_OUT3V3. New negative edges on pin DCDC_PLAY has no influence. When pin DCDC_STOP becomes HIGH the DC-to-DC converter stops and directly the signal SUPPLY_OK becomes a logic 0.

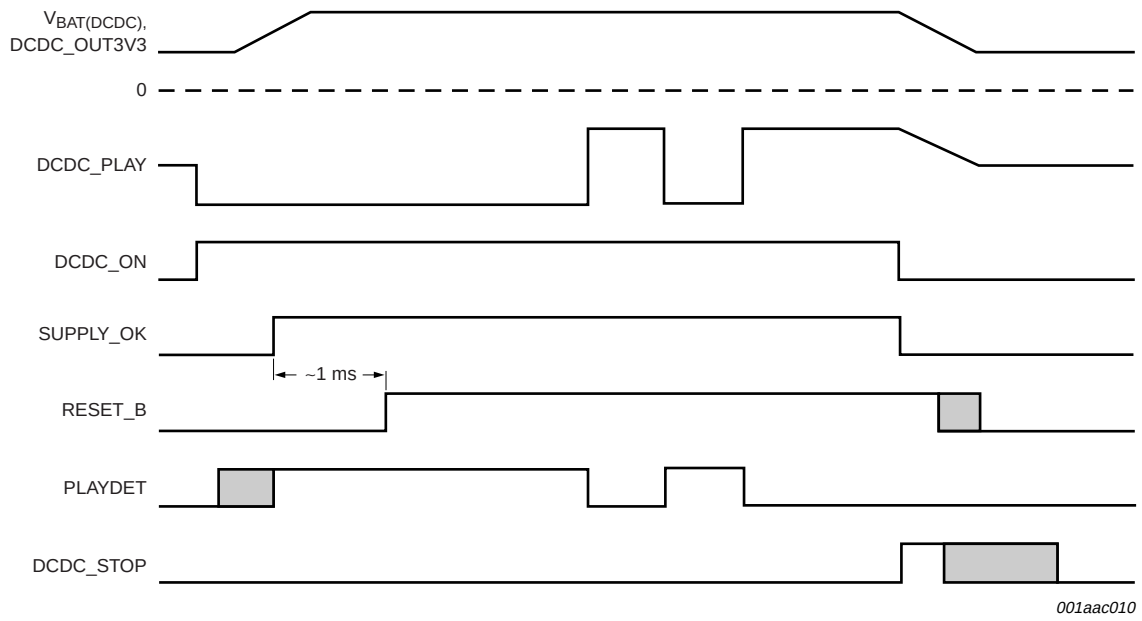


Fig 22. Play and stop with battery supply

The reference circuit, ring oscillator and the POR will be fed by $V_{DD(ALWAYS)}$. Signal RESET_B stays at logic 0 for about 1 ms for proper reset. Not shown in Figure 22 is signal CLK_STABLE, showing the moment for the core clock to become available to the DC-to-DC converters. As soon as a stable core clock is detected the DC-to-DC converters will switch to this clock in order to be in-phase with the DAC clock, which will minimize interference into the audio signal. The SAA8200HL is started up when this has happened.

7.21.3.2 Play and stop with USB supply

A start-up from the USB supply gives also a RESET_B pulse, see Figure 23. The signal VUSB is shaped by the bonding pad supplies V_{DDI} and V_{DDE}. The disconnection of $V_{USB(DCDC)}$ generates a stop pulse.

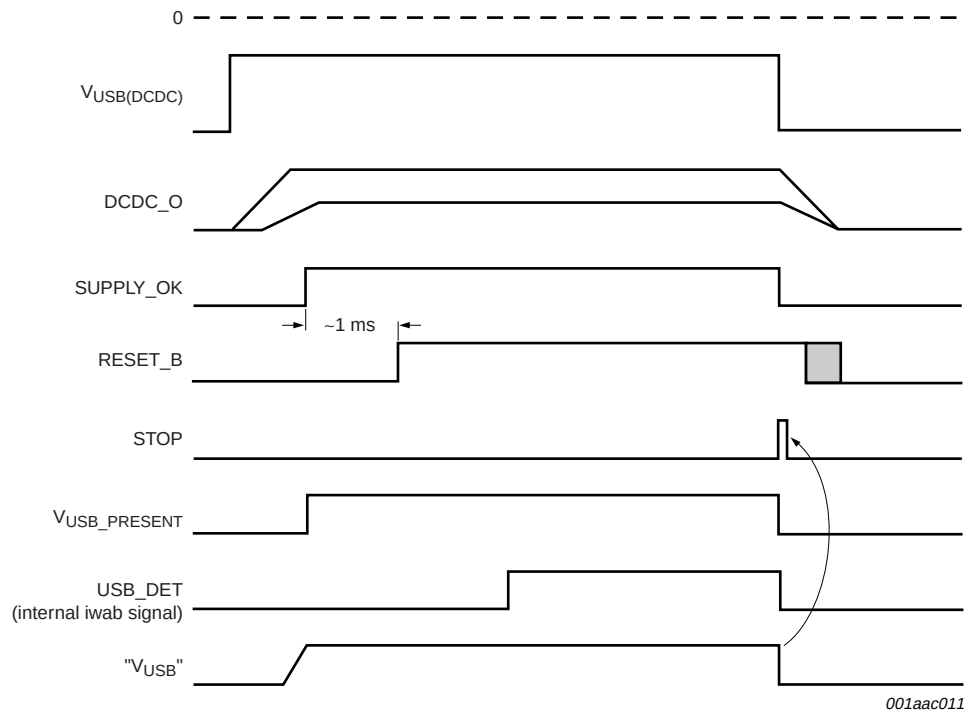


Fig 23. Play and stop with USB supply

7.21.3.3 Change from battery to USB supply

Figure 24 shows the timing diagram with a wireless transceiver changed to USB supply. The USB supply has the priority. When the USB plug is disconnected the device goes to the off state. In Idle mode the supplies DCDC_OUT1V8 and DCDC_OUT3V3 has still to be present, but the LDOs have to deliver only a small current. The total device may not draw more than 500 mA from the USB supply so a quiescent current of the few active circuits has to be less then 100 mA each.

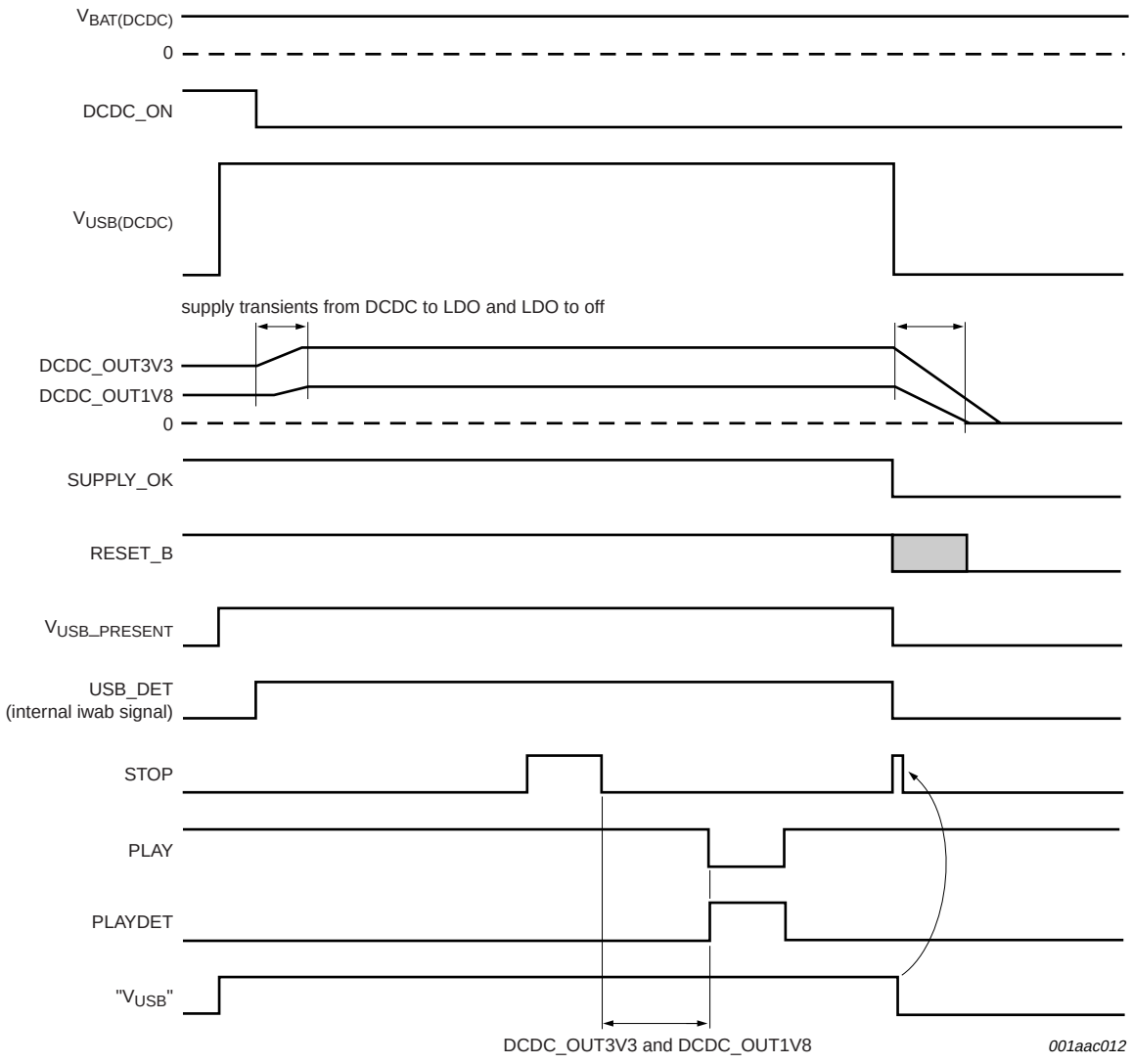


Fig 24. Change from battery to USB supply

8. Limiting values

Table 23: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDI}	core supply voltage (internal)		–0.5	2.5	V
V_{DDE}	core supply voltage (external)		–0.5	4.6	V
$V_{DDA(1V8)}$	1.8 V supply voltage		–0.5	2.5	V
$V_{DDA(3V3)}$	3.3 V supply voltage		–0.5	4.6	V
V_I	input voltage	normal digital input pins	–0.5	V_{DDE} + 0.5	V
		5 V tolerant digital input pins	–0.5	6.0	V
		analog input pins	–0.5	V_{DDA3v3} + 0.5	V
		pin XTALH_IN	–0.5	2.0	V
T_{amb}	ambient temperature		–20	+70	°C
T_j	junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+125	°C
T_{xtal}	crystal temperature		-	150	°C
$V_{BAT(DCDC)}$	battery voltage	single battery	0.9	1.6	V
		double battery	1.8	3.2	V
$V_{USB(DCDC)}$	USB voltage range		4.0	5.5	V
V_{esd}	electrostatic discharge voltage		[1] **<tbd>**	**<tbd>**	V
			[2] **<tbd>**	**<tbd>**	V

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.

9. Thermal characteristics

Table 24: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	**<tbd>**	K/W

10. Characteristics

Table 25: Supply voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDI}	core supply voltage (internal)		1.7	1.8	2.0	V
V_{DDE}	core supply voltage (external)	MPMC pins	1.7	3.3	3.6	V
		other	2.7	3.3	3.6	V
$V_{DDA(1V8\_XTALH)}$	crystal oscillator supply voltage		1.7	1.8	2.0	V
$V_{DDA(3V3\_SPDIF)}$	SPDIF supply voltage		3.0	3.3	3.6	V
$V_{DDA(3V3\_ADC10B)}$	control ADC supply voltage		2.7	3.3	3.6	V
$V_{DDA(1V8\_ADC)}$	audio ADC supply voltage		1.7	1.8	2.0	V
$V_{DDA(3V3\_ADC)}$	audio ADC supply voltage		2.7	3.3	3.6	V
$V_{DDA(3V3\_DAC)}$	audio DAC supply voltage		2.7	3.3	3.6	V
$V_{DDA(3V3\_HP)}$	headphone supply voltage		2.7	3.3	3.6	V
$V_{USB(DCDC)}$	USB supply voltage		4.0	5.0	5.5	V

Table 26: 5 V tolerant cells characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input circuits							
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
Output circuits							
V_{OH}	HIGH-level output voltage	I_{OH} depends on I/O cell type	[1]	V_{DDE} – 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} depends on I/O cell type	[1]	-	-	0.4	V
I_{OH}	HIGH-level output current	10 ns slew rate output; $V_{OH} = V_{DDE} - 0.4$ V	[1]	–5	-	-	mA
I_{OL}	LOW-level output current	10 ns slew rate output; $V_{OL} = 0.4$ V	[1]	4	-	-	mA
$I_{sc(H)}$	HIGH-level short circuit current	10 ns slew rate output; $V_{OH} = 0$ V	[2]	-	-	–45	mA
$I_{sc(L)}$	LOW-level short circuit current	10 ns slew rate output; $V_{OL} = V_{DDE}$	[2]	-	-	50	mA

[1] Accounts for 100 mV voltage drop in all supply lines.

[2] Allowed for a short time period.

Table 27: Control ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFN}	negative reference voltage		V_{SSA}	-	$V_{REFP} - 2$	V
V_{REFP}	positive reference voltage		$V_{REFN} + 2$	-	V_{DDA}	V
f_{smpl}	sampling rate		400	-	1500	kHz
Z_i	input impedance REFN to REFP		20	-	39	kΩ
V_i	input voltage		V_{REFN}	-	V_{REFP}	V
f_{clk}	clock frequency		-	-	4.5	MHz

Table 27: Control ADC characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N	resolution		2	-	10	bit
INL	integral non-linearity		-	-	±1	LSB
DNL	differential non-linearity		-	-	±1	LSB
E_{OS}	offset error		–20	-	+20	mV
E_{FS}	full scale error		–20	-	+20	mV
t_{conv}	conversion time		-	(N + 1) cycles	-	

Table 28: Static audio characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Audio DAC							
V_{REFN}	negative reference voltage			-	$V_{SSA(DAC)}$	-	V
V_{REFP}	positive reference voltage			-	$V_{DDA(3V3\_DAC)}$	-	V
V_O	output voltage	digital silence		-	$0.5V_{DDA(3V3\_DAC)}$	-	V
		during power-down	[1]	-	0	-	V
R_O	output resistance		[2]	0.7	1	1.3	kΩ
R_L	load resistance		[3]	>75	-	-	kΩ
R_{INT}	resistance between V_{REFP} and V_{REFN}			-	4	-	kΩ
Headphone amplifier							
V_{HP_COM}	reference input voltage			-	$0.5V_{DDA(3V3\_VREFP)}$	-	V
$V_{O(cm)}$	common mode output voltage			-	$V_{I(ref)}$	-	V
V_{offset}	input offset voltage			–10	-	+10	mV
R_L	load resistance			16	-	-	Ω
I_{sc}	output current at short circuit	left and right		80	100	140	mA
		center		180	200	240	mA
Audio ADC							
V_{ADC_REFP}	positive reference voltage			-	$V_{DDA(3V3\_ADC)}$	-	V
V_{ADC_REFN}	negative reference voltage			-	0	-	V
V_{ADC_COM}	common mode reference voltage			-	$0.5V_{DDA(3V3\_ADC)}$	-	V
R_I	input resistance			-	12	-	kΩ
C_I	input capacitance			-	24		pF
Low noise amplifier							
R_I	input resistance			3.5	5	-	kΩ
V_{offset}	output offset voltage			-	-	1	mV

[1] Set headphone amplifier in Power-down mode before setting audio DAC in Power-down mode because the line output is connected to the headphone driver the output of the headphone clips towards its analog supply.

[2] Exclusive the input load of the headphone driver which is 10 kΩ.

[3] The output of the DAC is already connected with the headphone driver which has an input load of 10 kΩ.

Table 29: Dynamic audio characteristics

$V_{DDA(3V3)}$ = 3.3 V; f_i = 1 kHz at −1 dB; T_{amb} = 25 °C; R_L = 100 kΩ; f_s = 48 kHz; all voltages measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Audio DAC							
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input;	[1]	-	1	-	V
ΔV_o	unbalance between channels			-	<0.1	-	dB
V_O	output voltage	digital silence		-	$0.5V_{DDA(3V3\_DAC)}$	-	V
		during power-down	[1]	-	0	-	V
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB		-	−80	-	dB
		at −60 dB; A-weighted		-	−40	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted; bidirectional DWA		-	100	-	dB
α_{cs}	channel separation			-	90	-	dB
Headphone amplifier							
$P_{o(rms)}$	output power (RMS value)	at 0 dBFS digital input; R_L = 16 Ω		-	35	-	mW
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at 0 dB; R_L = 16 Ω		-	62	−52	dB
		at 0 dB; R_L = 5 kΩ		-	82	-	dB
		at −60 dB; A-weighted		-	35	-	dB
S/N	signal-to-noise ratio	code = 0; A-weighted		-	97	-	dB
α_{cs}	channel separation	R_L = 16 Ω		-			
		no decoupling capacitors		-	−36	-	dB
		with decoupling capacitors		-	−90	-	dB
Audio ADC							
ΔV_i	unbalance between channels			-	<1	-	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted		-	95	-	dB
α_{cs}	channel separation			-	110	-	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 30 mV					
	$V_{DDA(3V3\_ADC)}$			-	−55	-	dB
	$V_{DDA(3V3\_REFP)}$			-	−65	-	dB
D_o	digital output level	0 dB setting; $V_{i(rms)}$ = 1.0 V		−2.5	−1	−1	dBFS
		3 dB setting; $V_{i(rms)}$ = 708 mV		−2.5	−1	−1	dBFS
		6 dB setting; $V_{i(rms)}$ = 501 mV		−2.5	−1	−1	dBFS
		9 dB setting; $V_{i(rms)}$ = 354 mV		−2.5	−1	−1	dBFS
		12 dB setting; $V_{i(rms)}$ = 252 mV		−2.5	−1	−1	dBFS
		15 dB setting; $V_{i(rms)}$ = 178 mV		−2.5	−1	−1	dBFS
		18 dB setting; $V_{i(rms)}$ = 125 mV		−2.5	−1	−1	dBFS
		21 dB setting; $V_{i(rms)}$ = 89 mV		−2.5	−1	−1	dBFS
		24 dB setting; $V_{i(rms)}$ = 63 mV		−2.5	−1	−1	dBFS

Table 29: Dynamic audio characteristics *…continued*

$V_{DDA(3V3)}$ = 3.3 V; f_i = 1 kHz at −1 dB; T_{amb} = 25 °C; R_L = 100 kΩ; f_s = 48 kHz; all voltages measured with respect to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	at −1 dBFS				
		0 dB setting	-	−85	-	dB
		3 dB setting	-	−87	-	dB
		6 dB setting	-	−88	-	dB
		9 dB setting	-	−88	-	dB
		12 dB setting	-	−87	-	dB
		15 dB setting	-	−85	-	dB
		18 dB setting	-	−83	-	dB
		21 dB setting	-	−80	-	dB
		at −60 dBFS				
		0 dB setting	-	−35	-	dB
		3 dB setting	-	−34	-	dB
		6 dB setting	-	−32	-	dB
		9 dB setting	-	−30	-	dB
		12 dB setting	-	−28	-	dB
		15 dB setting	-	−26	-	dB
		18 dB setting	-	−23	-	dB
		21 dB setting	-	−20	-	dB
		24 dB setting	-	−20	-	dB
LNA plus ADC						
$V_{i(rms)}$	input voltage (RMS value)	at 0 dBFS digital output; R_S = 2.2 kΩ	-	-	35	mV
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	V_o = 600 mV	-	−75	-	dB
		at −60 dB; A-weighted	-	−25	-	dB
S/N	signal-to-noise ratio	V_i = 0 V; A-weighted	-	85	-	dB

[1] The output voltage of the DAC is proportional to the DAC power supply voltage and the headphone is in Power-down mode.

[2] Exclusive the input load of the headphone driver which is 10 kΩ.

[3] The output of the DAC is already connected with the headphone driver which has an input load of 10 kΩ.

Table 30: DC-to-DC converter characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{bat}	battery voltage	single battery	0.9	1.35	1.6	V
		double battery	1.8	2.7	3.2	V
V_{USB}	USB voltage		4.0	5.0	5.5	V
DC-to-DC converter for 3.3 V						
V_O	output voltage		3.0	3.4	3.7	V
$V_{O(tol)}$	output voltage tolerance		-	-	100	mV

Table 30: DC-to-DC converter characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_O	output current	V_{bat} = 2.4 V; R_L = 0.3 Ω	200	-	-	mA
		V_{bat} = 2.0 V; R_L = 0.3 Ω	150	-	200	mA
I_{su}	start-up current		-	-	25	mA
I_{sw}	switch current		-	<tbd>	-	mA
f_{switch}	switching frequency		-	-	1	MHz
f_{clk}	clock frequency		-	-	12	MHz
η	efficiency	V_{bat} = 2.4 V; I_O = 100 mA; R_L = 0.3 Ω	90	93	-	%
R_P	PMOST switch on resistance		-	0.3	-	Ω
R_N	NMOST switch on resistance		-	0.3	-	Ω
ESR_C	maximum ESR_C		-	-	0.7	Ω
DC-to-DC converter for 1.8 V						
V_O	output voltage		1.3	1.85	2.0	V
$V_{O(tol)}$	output voltage tolerance		-	-	50	mV
I_O	output current	V_{bat} = 2.4 V; R_L = 0.3 Ω	100	-	-	mA
		V_{bat} = 2.0 V; R_L = 0.3 Ω	50	-	200	mA
I_{su}	start-up current		-	-	10	mA
I_{sw}	switch current		-	<tbd>	-	mA
f_{switch}	switching frequency		-	-	1	MHz
f_{clk}	clock frequency		-	-	12	MHz
η	efficiency	V_{bat} = 2.4 V; I_O = 50 mA; R_L = 0.3 Ω	92	95	-	%
R_P	PMOST switch on resistance		-	0.9	-	Ω
R_N	NMOST switch on resistance		-	0.9	-	Ω
ESR_C	maximum ESRC		-	-	0.7	Ω
Low-drop-out converter for 3.3 V						
V_O	output voltage	unloaded	-	3.5	-	V
		I_O = 100 mA	-	3.4	-	V
$V_{O(tol)}$	output voltage tolerance		-	-	100	mV
I_O	output current	V_{USB} = 5 V	150	-	200	mA
I_{IDLE}	idle current		-	-	100	µA
Low-drop-out converter for 1.8 V						
V_O	output voltage	unloaded	-	1.95	-	V
		I_O = 50 mA	-	1.85	-	V
$V_{O(tol)}$	output voltage tolerance		-	-	50	mV
I_O	output current	V_{USB} = 5 V	50	-	100	mA

Table 30: DC-to-DC converter characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Ring oscillator						
I_{DDA}	current consumption		-	-	100	µA
f_{OSC}	oscillator output frequency		-	12	-	MHz

Table 31: SRI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LVDS buffer						
Static						
I_{DDA}	supply current		-	150	-	µA
$I_{DDA(pd)}$	power-down supply current		-	-	1	µA
C_L	load capacitor		-	-	5	pF
R_O	output voltage as ratio of the digital supply voltage		-	0.25	-	
$V_{I(det)}$	input voltage required for detection		-	100	-	mV
Dynamic						
$f_{clk(max)}$	maximum clock frequency		-	-	1	MHz

Table 32: Timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal oscillator						
Static						
$C_{i(XTALH\_IN)}$	parasitic input capacitance pin XTALH_IN		**<tbd>**	**<tbd>**	**<tbd>**	pF
$R_{i(XTALH\_IN)}$	parasitic input resistance pin XTALH_IN	f_i = 12 MHz	**<tbd>**	**<tbd>**	**<tbd>**	Ω
P_{drive}	crystal level of driver power		100	-	500	µW
Dynamic						
f_{osc}	oscillator frequency		-	12	-	MHz
α_{cl}	duty cycle		-	50	-	%
t_{su}	start-up time		-	500	-	ms
Serial interface input and output data timing; see Figure 25						
f_{BCK}	bit clock frequency		-	-	$128f_s$	Hz
$T_{cy(BCK)}$	bit clock cycle time	$T_{cy(s)}$ is sample frequency cycle time	-	-	$^1/_{128}T_{cy(s)}$	s
t_{BCKH}	bit clock HIGH time		30	-	-	ns
t_{BCKL}	bit clock LOW time		30	-	-	ns
t_r	rise time		-	-	20	ns
t_f	fall time		-	-	20	ns
$t_{su(WS)}$	word select setup time		10	-	-	ns
$t_{h(WS)}$	word select hold time		10	-	-	ns
$t_{su(I2SIN)}$	data input setup time		10	-	-	ns
$t_{h(I2SIN)}$	data input hold time		10	-	-	ns

Table 32: Timing characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(I2SOUT)}$	data output hold time		0	-	-	ns
$t_{d(I2SOUT\_BCK)}$	data output to bit clock delay		-	-	30	ns
$t_{d(I2SOUT\_WS)}$	data output to word select delay		-	-	30	ns
Standard mode I^2C-bus; SDA and SCL lines						
100 kHz mode						
f_{SCL}	SCL clock frequency		0	-	100	kHz
t_{LOW}	SCL clock LOW period		4.7	-	-	µs
t_{HIGH}	SCL clock HIGH period		4.0	-	-	µs
$t_{HD;STA}$	hold time start condition		4.0	-	-	µs
$t_{SU;STA}$	setup time start condition		4.7	-	-	µs
$t_{SU;STO}$	setup time stop condition		4.0	-	-	µs
t_{BUF}	bus free time between a stop and start condition		4.7	-	-	µs
$t_{HD;DAT}$	data hold time		5.0	-	0.9	µs
$t_{SU;DAT}$	data setup time		250	-	-	ns
t_r	rise time SDA and SCL		-	-	1000	ns
t_f	fall time SDA and SCL		-	-	300	ns
400 kHz mode						
f_{SCL}	SCL clock frequency		0	-	400	kHz
t_{LOW}	SCL clock LOW period		1.3	-	-	µs
t_{HIGH}	SCL clock HIGH period		0.6	-	-	µs
$t_{HD;STA}$	hold time start condition		0.6	-	-	µs
$t_{SU;STA}$	setup time repeated start		0.6	-	-	µs
$t_{SU;STO}$	setup time stop condition		0.6	-	-	µs
t_{BUF}	bus free time between a stop and start condition		1.3	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	-	µs
$t_{SU;DAT}$	data setup time		100	-	-	ns
t_r	rise time SDA and SCL		$20 + 0.1C_b$	-	300	ns
t_f	fall time SDA and SCL		$20 + 0.1C_b$	-	300	ns
t_{SP}	pulse width of spikes		0	-	50	ns
C_b	capacitive load for each bus line		-	-	400	pF

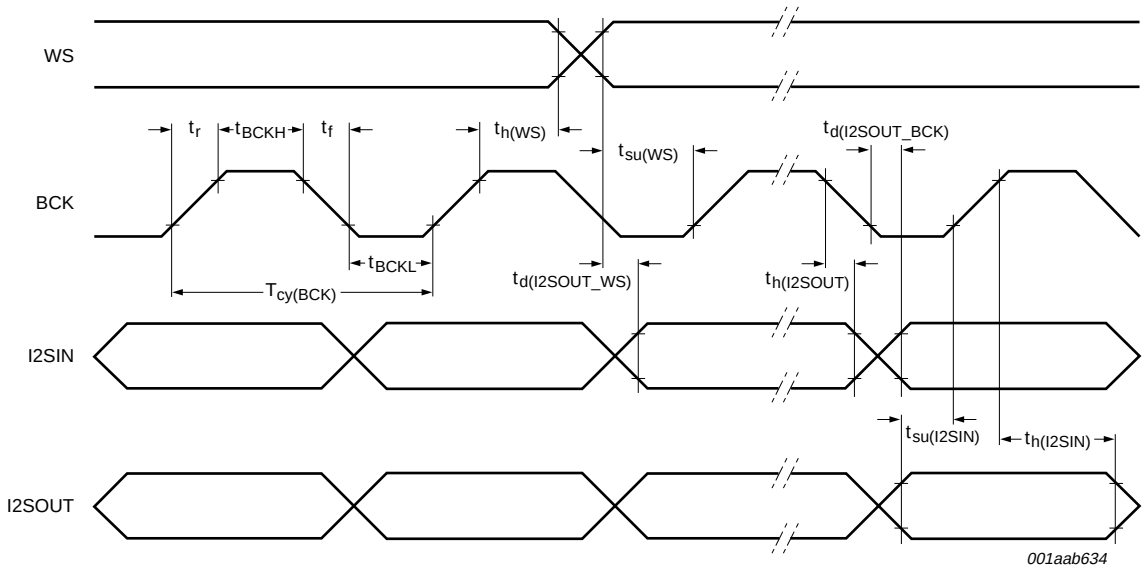


Fig 25. Serial interface input data timing

Table 33: Filter characteristics

Description	Conditions	Value	Unit
Decimation filter			
Pass band ripple	up to $0.45f_s$	±0.02	dB
Stop band	from $0.55f_s$	−60	dB
Overall gain	DC	3	dB
Dynamic range	up to $0.45f_s$	140	dB
Droop	at $0.45f_s$	−0.18	dB
DC blocking filter 1			
Pass band ripple		none	dB
Pass band gain		0	dB
Droop	at $0.00045f_s$	0.5	dB
DC attenuation		> 40	dB
Dynamic range	up to $0.45f_s$	> 110	dB
DC blocking filter 2			
Pass band ripple		none	dB
Pass band gain		0	dB
Droop	at $0.00045f_s$	0.031	dB
DC attenuation		> 40	dB
Dynamic range	up to $0.45f_s$	> 110	dB
Interpolation filter			
pass band ripple	up to $0.4535f_s$	±0.02	dB
stop band	from $0.5465f_s$	−72	dB
gain	pass band	−1.1	dB
dynamic range	up to $0.4535f_s$	>143	dB

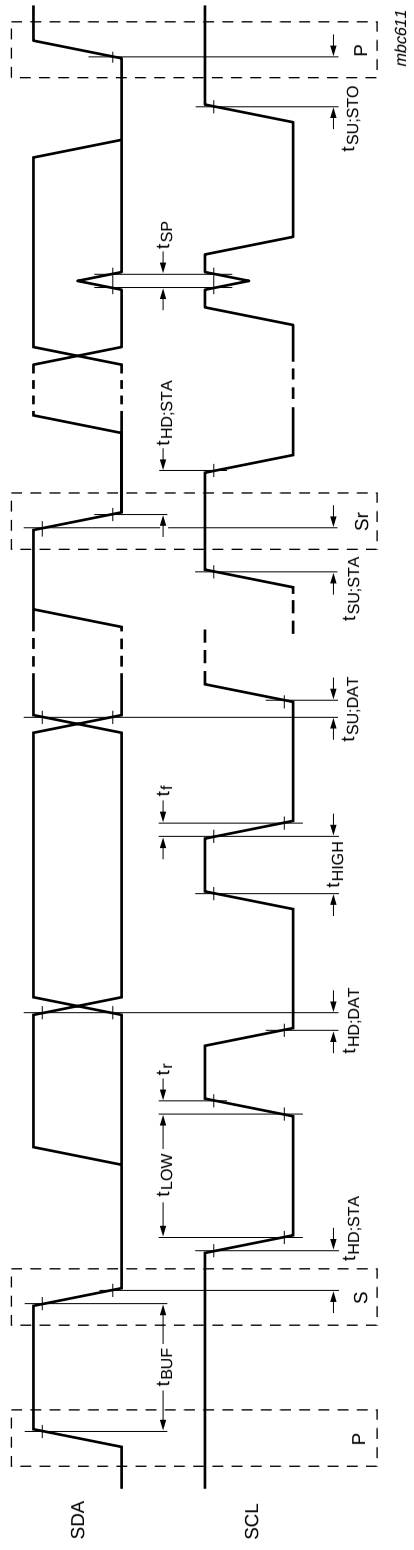


Fig 26. Timing of the I²C-bus transfer

11. Application information

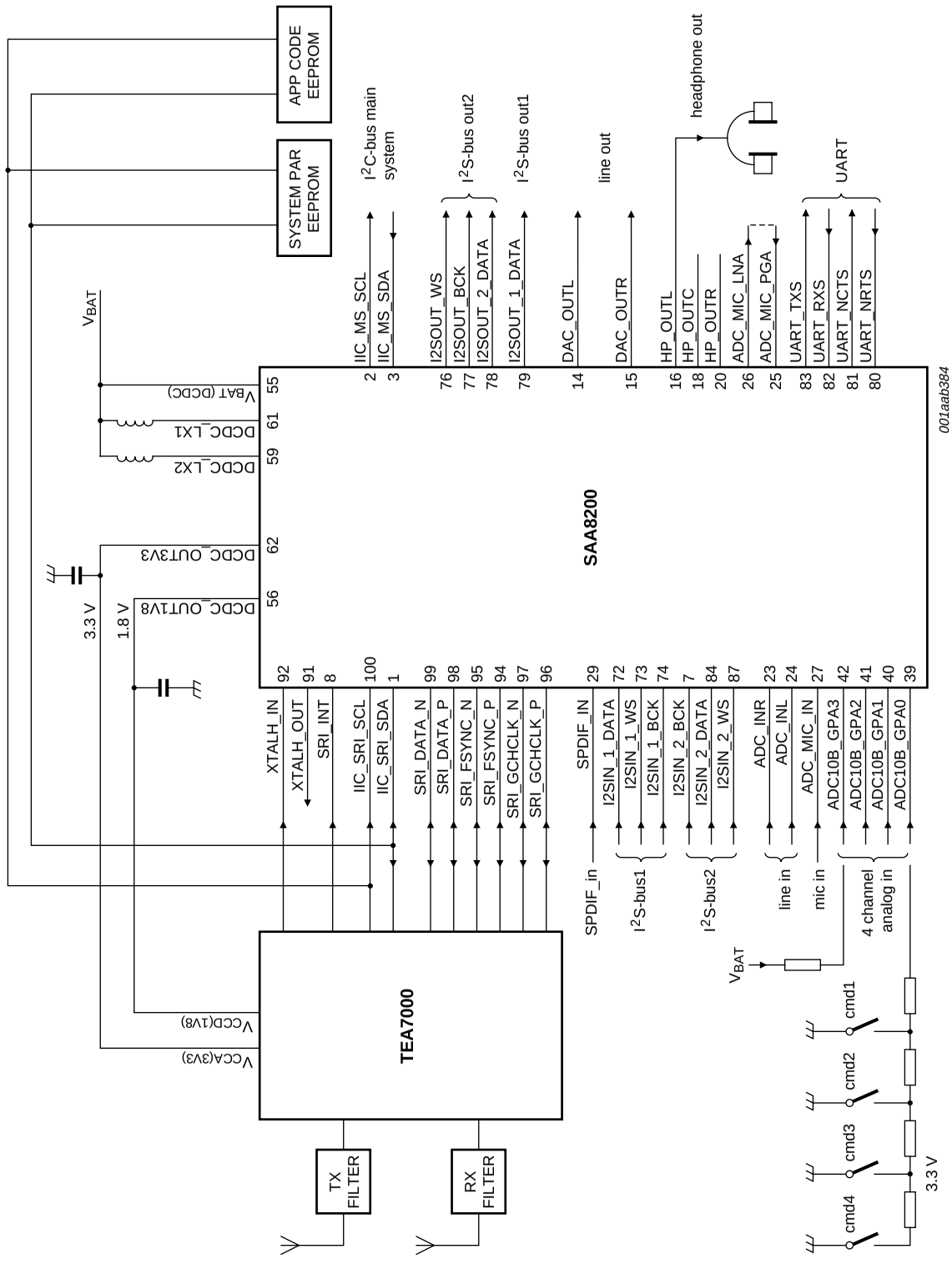
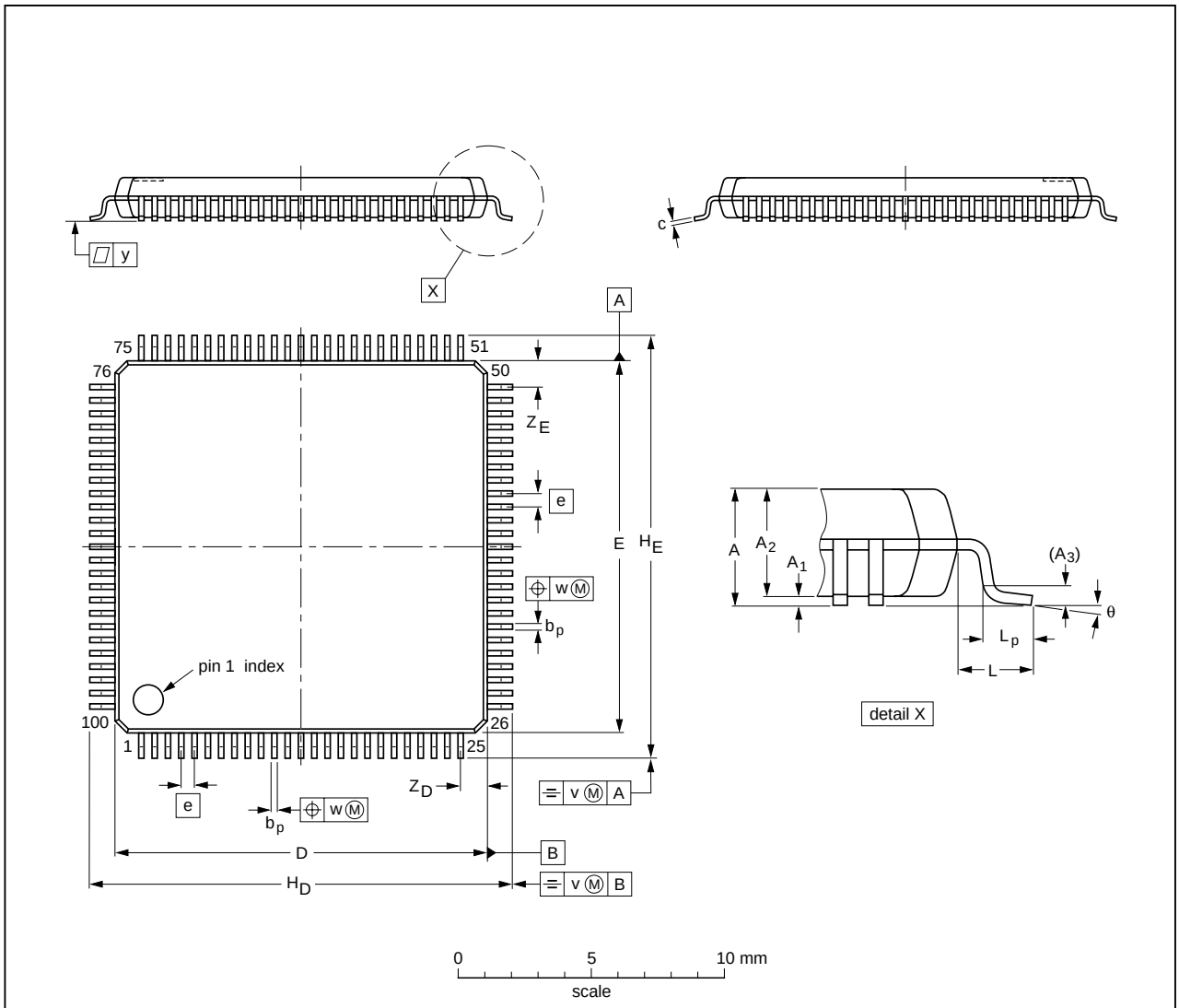


Fig 27. Ensation Link application diagram

12. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 28. Package outline SOT407-1 (LQFP100)

13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 34: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Additional soldering information

15.1 Lead-free solder

Lead-free solder can be used for soldering the TEA7000.

15.2 MSL level

MSL level: **<tbd>**

16. Revision history

Table 35: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SAA8200HL_2	20051017	Preliminary data sheet	-	-	SAA8200HL_1
Modifications:	• Audio ADC supply voltages added (Table 25). • Audio DAC R_L value revised; V_{HP_COM} value corrected; V_{ADC_COM} value added (Table 28). • Dynamic audio characteristics revised (Table 29).				
SAA8200HL_1	20041217	Objective data sheet	-	9397 750 13236	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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