High ESD-Protected, Fail-Safe, Slew-Rate-Limited RS-485 Transceivers BL3085A

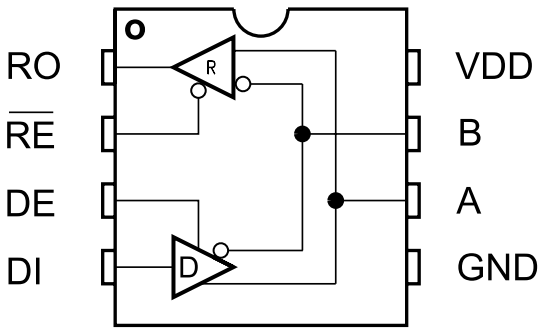
GENERAL DESCRIPTION

The BL3085A is a +/-15kV electrostatic discharge (ESD) protected, high-speed transceiver for RS-485 communication that contain one driver and one receiver. The device feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be logic high even if all transmitters on a terminated bus are disabled. The BL3085A feature reduced slew-rate driver that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps. All transmitter outputs and receiver inputs are protected to +/-15kV using the Human Body Air Gap Model. The transceiver typically draws 500uA of supply current when unloaded, or when fully loaded with the driver disabled. All device have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The BL3085A is intended for half-duplex communications. BL3085A is available in industry-standard 8-pin SO or DIP packages.

APPLICATIONS

RS-485 Communications
Level Translators
Transceivers for EMI-Sensitive Applications
Industrial Control Local Area Networks
Energy Meter Networks
Power Inverters
Building Automation Networks
Telecommunications Equipment

PIN Configuration



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) .....+ 7V
Control Input Voltage (RE, DE).....-0.3V to (VCC + 0.3V
Driver Input Voltage (DI).....-0.3V to (VCC + 0.3V)
Driver Output Voltage (A, B).....-8V to +13V
Receiver Input Voltage (A, B) .....-8V to +13V
Receiver Output Voltage (RO).....-0.3V to (VCC + 0.3V)
Operating Temperature Ranges.....-40°C to +85°C

DC ELECTRICAL CHARACTERISTICS

(VCC = +5V ±5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output (no load)	VOD1	Figure 1				5	V
Differential Driver Output	VOD2	Figure 1, R = 27Ω		1.5			V
Change in Magnitude of Differential Output Voltage (Note 2)	ΔVOD	Figure 1, R = 27Ω				0.2	V
Driver Common-Mode Output Voltage	VOC	Figure 1, R = 27Ω				3	V
Change In Magnitude of Common-Mode Voltage (Note 2)	ΔVOC	Figure 1, R = 27Ω				0.2	V
Input High Voltage	VIH1	DE, DI, RE		2			V
Input Low Voltage	VIL1	DE, DI, RE				0.8	V
DI Input Hysteresis	VHYS				100		mV
Input Current (A and B)	IIN1	DE = GND, VCC = GND or 5.25V	VIN = 12V			125	μA
			VIN = -7V			-75	
Driver Short-Circuit Output Current (Note 3)	IOD1	-7V ≤ VOUT ≤ VCC		-250			mA
		0V ≤ VOUT ≤ 12V				250	
		0V ≤ VOUT ≤ VCC		±25			
RECEIVER							
Receiver Differential Threshold Voltage	VTH	-7V ≤ VCM ≤ 12V		-300	-125	-30	mV
Receiver Input Hysteresis	ΔVTH				25		mV
Receiver Output High Voltage	VOH	IO = -4mA, VID = -50mV		VCC -1.5			V
Receiver Output Low Voltage	VOL	IO = 4mA, VID = -200mV				0.4	V
Three-State Output Current at Receiver	IOZR	0.4V ≤ VO ≤ 2.4V				±1	μA
Receiver Input Resistance	RIN	-7V ≤ VCM ≤ 12V		96			kΩ
Receiver Output Short-Circuit Current	IOSR	0V ≤ VRO ≤ VCC		±7		±95	mA

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY CURRENT							
Supply Current		No load, $\overline{RE}$ = DI = GND or VCC	DE = VCC		475	1000	μA
			DE = GND		420	800	
Supply Current in Shutdown Mode	ISHDN	DE = GND, $V_{\overline{RE}}$ = VCC			1	10	μA

SWITCHING CHARACTERISTICS

(VCC = +5V ±5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	tDPLH	Fig 3 and 5, RDIFF = 54Ω, CL1 = CL2 = 100pF	250	720	2000	ns
	tDPHL		250	720	1000	
Driver Output Skew | tDPLH - tDPHL |	tDSKEW	Fig 3 and 5, RDIFF = 54Ω, CL1 = CL2 = 100pF		-3	±100	ns
Driver Rise or Fall Time	tDR, tDF	Fig 3 and 5, RDIFF = 54Ω, CL1 = CL2 = 100pF	200	530	750	ns
Maximum Data Rate	fMAX		250			kbps
Driver Enable to Output High	tDZH	Figures 4 and 6, CL = 100pF, S2 closed			2500	ns
Driver Enable to Output Low	tDZL	Figures 4 and 6, CL = 100pF, S1 closed			2500	ns
Driver Disable Time from Low	tDLZ	Figures 4 and 6, CL = 15pF, S1 closed			100	ns
Driver Disable Time from High	tDHZ	Figures 4 and 6, CL = 15pF, S2 closed			100	ns
Receiver Input to Output	tRPLH, tRPHL	Figures 7 and 9; | VID | ≥ 2.0V; rise and fall time of VID ≤ 15ns		127	200	ns
| tRPLH - tRPHL | Differential Receiver Skew	tRSKD	Figures 7 and 9; | VID | ≥ 2.0V; rise and fall time of VID ≤ 15ns		3	±30	ns
Receiver Enable to Output Low	tRZL	Figures 2 and 8, CL = 100pF, S1 closed		20	50	ns
Receiver Enable to Output High	tRZH	Figures 2 and 8, CL = 100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	tRLZ	Figures 2 and 8, CL = 100pF, S1 closed		20	50	ns
Receiver Disable Time from High	tRHZ	Figures 2 and 8, CL = 100pF, S2 closed		20	50	ns
Time to Shutdown	tSHDN	(Note 4)	50	200	600	ns
Driver Enable from Shutdown to Output High	tDZH(SHDN)	Figures 4 and 6, CL = 15pF, S2 closed			4500	ns
Driver Enable from Shutdown to Output Low	tDZL(SHDN)	Figures 4 and 6, CL = 15pF, S1 closed			4500	ns
Receiver Enable from Shutdown to Output High	tRZH(SHDN)	Figures 2 and 8, CL = 100pF, S2 closed			3500	ns
Receiver Enable from Shutdown to Output Low	tRZL(SHDN)	Figures 2 and 8, CL = 100pF, S1 closed			3500	ns

Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.
Note 2: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.
Note 3: Maximum current level applies to peak current just prior to foldback-current limiting; minimum current level applies during current limiting.
Note 4: The device is put into shutdown by bringing RE high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

TEST CIRCUITS AND TIMING DIAGRAMS

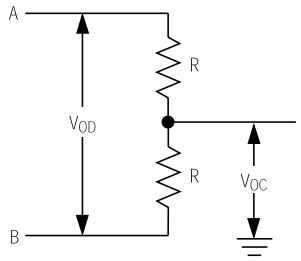


Figure 1. Driver DC Test Load

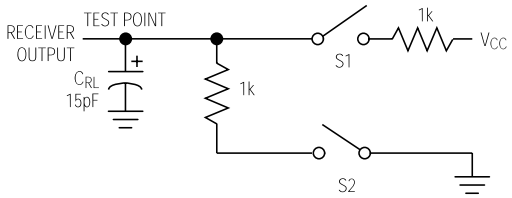


Figure 2. Receiver Enable/Disable Timing Test Load

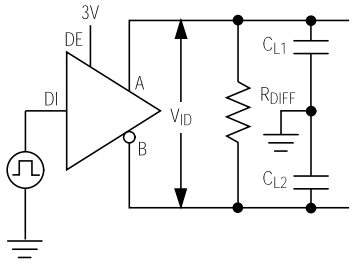


Figure 3. Driver Timing Test Circuit

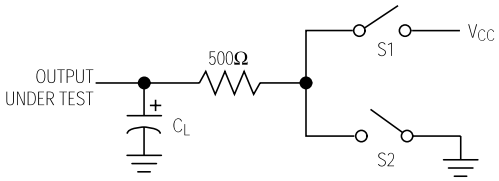


Figure 4. Driver Enable/Disable Timing Test Load

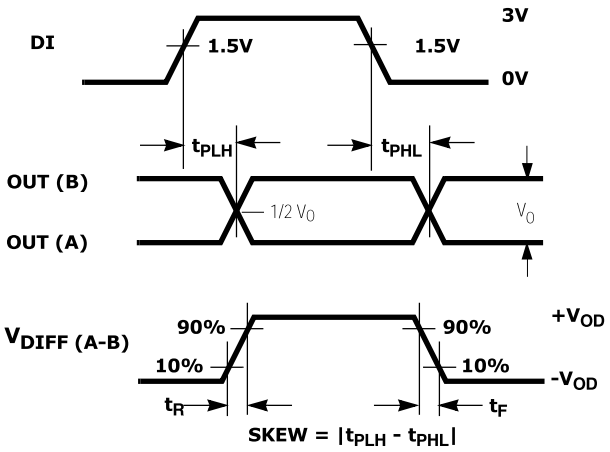


Figure 5. Driver Propagation Delays

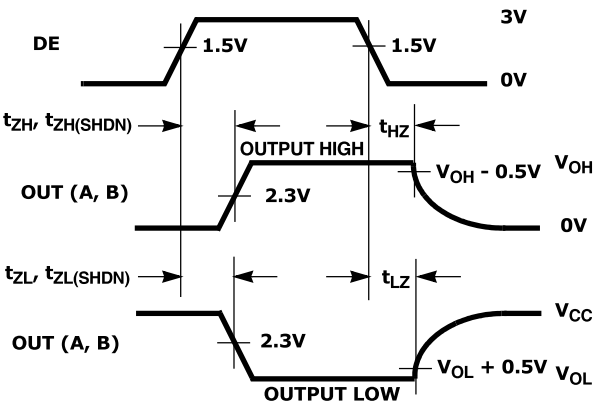


Figure 6. Driver Enable and Disable Times

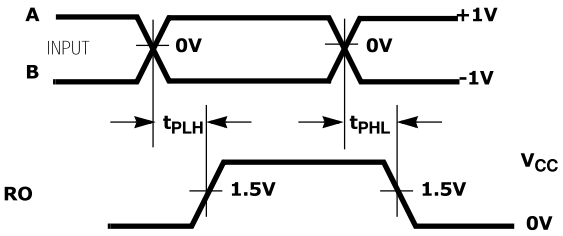


Figure 7. Receiver Propagation Delays

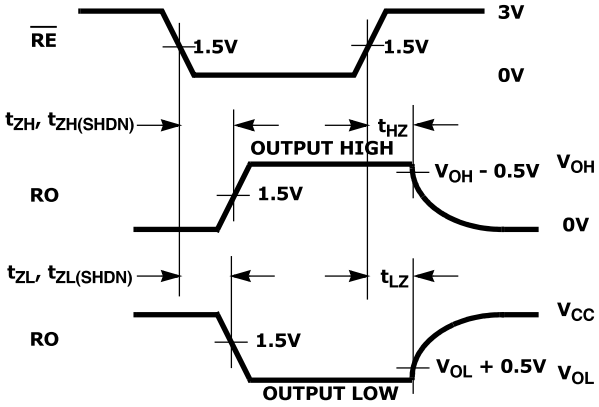


Figure 8. Receiver Enable and Disable Times

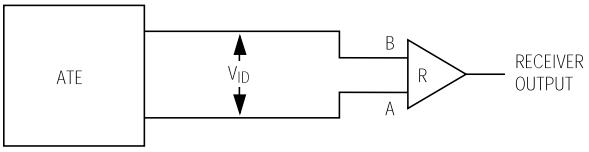


Figure 9. Receiver Propagation Delay Test Circuit

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	RO	Receiver Output. When RE is low and if A - B ≥ -30mV, RO will be high; if A - B ≤ -300mV, RO will be low.
2	RE	Receiver Output Enable. Drive RE low to enable RO; RO is high impedance when RE is high. Drive RE high and DE low to enter low-power shutdown mode.
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive RE high and DE low to enter low-power shutdown mode.
4	DI	Driver Input. With DE high, a low on DI forces noninverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	VCC	Positive Supply 4.75V ≤ VCC ≤ 5.25V

FUNCTION TABLES

TRANSMITTING				
INPUTS			OUTPUTS	
RE	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUT
RE	DE	A-B	RO
0	X	≥ -0.03V	1
0	X	≤ -0.3V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

X = Don't care
Shutdown mode, driver and receiver outputs high impedance

DETAILED DESCRIPTION

The BL3085A high-speed transceiver for RS-485 communication contains one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe section). The BL3085A feature reduced slew-rate driver that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps (see the Reduced EMI and Reflections section). The BL3085A is a half-duplex transceiver. The part operates from a single +5V supply. Drivers are output short-circuit current limited. Thermal shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high impedance state.

RECEIVER INPUT FILTERING

The receiver of the BL3085A, when operating in 250kbps, incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 20% due to this filtering.

FAIL-SAFE

The BL3085A guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -30mV and -300mV. If the input voltage of differential receiver (A-B) is greater than or equal to -30mV, RO is logic high. If A-B is less than or equal to -300mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the BL3085A, this results in a logic high with a 30mV minimum noise margin.

ESD PROTECTION

As with BL3085A, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the BL3085A have extra protection against static electricity. The ESD-protected pins are tested with reference to the ground pin in a powered-down condition. They are tested to +/-15kV using the Human Body Model.

POWER USAGE IN AN RS-485 TRANSCEIVER

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus. The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32mA. The BL3085A is rated as a 1/8 unit load device. The bus input current is less than 1/8mA, allowing up to 256 nodes on a single bus. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120ohm resistor at each end, this sums to 25mA differential output current whenever the bus is active. Typically the BL3085A can drive more than 25mA to a 60ohm load, resulting in a differential output voltage higher than the minimum required by the standard. Overall, the total load current can be 60mA to a loaded RS-485 bus. This is in addition to the current required by the transceiver itself; the BL3085A circuitry requires only about 0.4mA with both driver and receiver enabled, and only 0.3mA with either the driver enabled or with the receiver enabled. In low-power shutdown mode, neither the driver nor receiver is active. And the supply current is very low. Supply current increases with signaling rate primarily due to the totem pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

LOW-POWER SHUTDOWN MODE

When both the driver and receiver are disabled (DE low and RE high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down except over temperature protection circuit, and the supply current is typically 15uA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the DI input after the enable times given by tPZH(SHDN) and tPZL(SHDN) in the driver switching characteristics. If the DI input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature. If only the receiver is re-enabled (RE transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by tPZH(SHDN) and tPZL(SHDN) in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section. If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver.

DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a fold back current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal shutdown circuit, force the driver outputs into a high-impedance state if the die temperature becomes excessive.

LAYOUT CONSIDERATION

A ground plane is recommended when using a high frequency device like the BL3085A. A 0.1uF ceramic bypass capacitor less than 1/4 inch away from the VDD pin is recommended. Good bypassing is especially needed when operating at maximum frequency or when package to package matching is very important. The PC board traces connected to the A and B outputs must be kept as symmetrical and short as possible to obtain the same parasitic board capacitance. This maintains the good matching characteristics of the low-to-high and high to low transitions of the BL3085A. Note that output A to output B capacitance should also be minimized. If routed adjacent to each other on the same layer, they should be separated by an amount at least as wide as the trace widths. If output A and output B are routed on different signal planes, they should not be routed directly on top of each other. A trace width lateral separation is also recommended. As mentioned before, care should also be taken when routing the DI input. To achieve consistent board-to board propagation delay, the ringing on this signal should be kept below a few hundred millivolts.