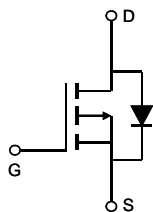# AON2407
30V P-Channel MOSFET

General Description

The AON2407 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

Features

V_{DS}	-30V
I_D (at V_{GS}=-10V)	-6.3A
$R_{DS(ON)}$ (at V_{GS} =-10V)	< 37.5mΩ
$R_{DS(ON)}$ (at V_{GS} =-4.5V)	< 46mΩ
$R_{DS(ON)}$ (at V_{GS} =-2.5V)	< 70mΩ

Green Product

Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25℃	I_D	-6.3	A
	T_A=70℃		-5	
Pulsed Drain Current [C]		I_{DM}	-34	
Power Dissipation [A]	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	37	45	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		66	80	℃/W

Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=-250µA, V$_{GS}$=0V		-30			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=-30V, V$_{GS}$=0V				-1	µA
			T$_J$=55℃			-5	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±12V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$, I$_D$=-250µA		-0.4	-0.93	-1.5	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=-10V, V$_{DS}$=-5V		-34			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=-10V, I$_D$=-6.3A			31	37.5	mΩ
			T$_J$=125℃		51.5	62	
		V$_{GS}$=-4.5V, I$_D$=-5A			36.5	46	mΩ
		V$_{GS}$=-2.5V, I$_D$=-3A			50.3	70	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=-5V, I$_D$=-6.3A			24		S
V$_{SD}$	Diode Forward Voltage	I$_S$=-1A,V$_{GS}$=0V			-0.7	-1	V
I$_S$	Maximum Body-Diode Continuous Current					-3.5	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=-15V, f=1MHz			746		pF
C$_{oss}$	Output Capacitance				105		pF
C$_{rss}$	Reverse Transfer Capacitance				70		pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz			9.5	19	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge	V$_{GS}$=-10V, V$_{DS}$=-15V, I$_D$=-6.3A			17.2	21	nC
Q$_g$(4.5V)	Total Gate Charge				8	10	nC
Q$_{gs}$	Gate Source Charge				1.4		nC
Q$_{gd}$	Gate Drain Charge				2.8		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=-10V, V$_{DS}$=-15V, R$_L$=2.4Ω, R$_{GEN}$=3Ω			5.8		ns
t$_r$	Turn-On Rise Time				7.0		ns
t$_{D(off)}$	Turn-Off DelayTime				62.0		ns
t$_f$	Turn-Off Fall Time				23.2		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=-6.3A, dI/dt=500A/µs			19		ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=-6.3A, dI/dt=500A/µs			46		nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25° C. The Power dissipation P$_{DSM}$ is based on R$_{θJA}$ t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25° C.
D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25° C.

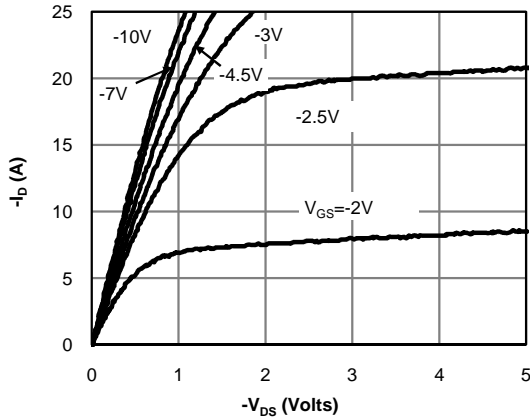**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

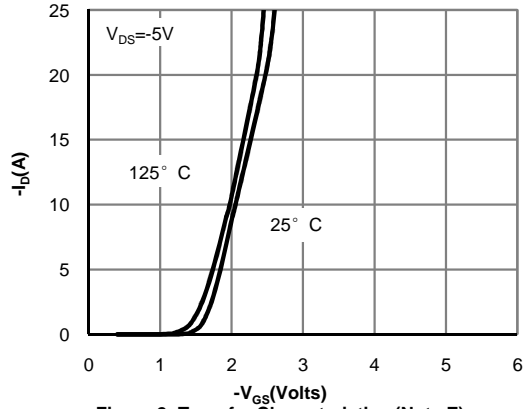**Fig 1: On-Region Characteristics (Note E)**

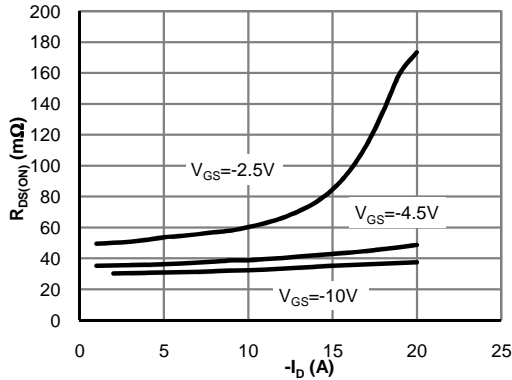**Figure 2: Transfer Characteristics (Note E)**

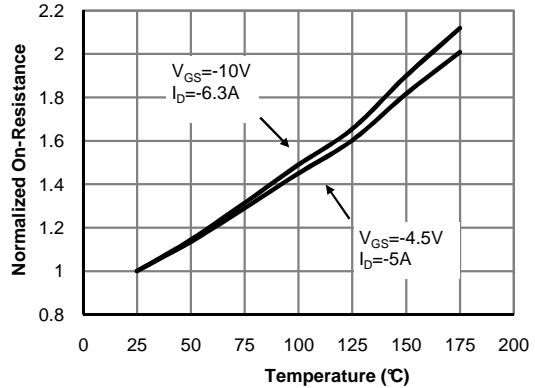**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

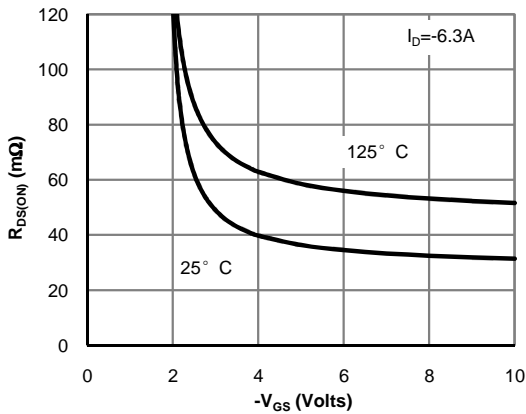**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

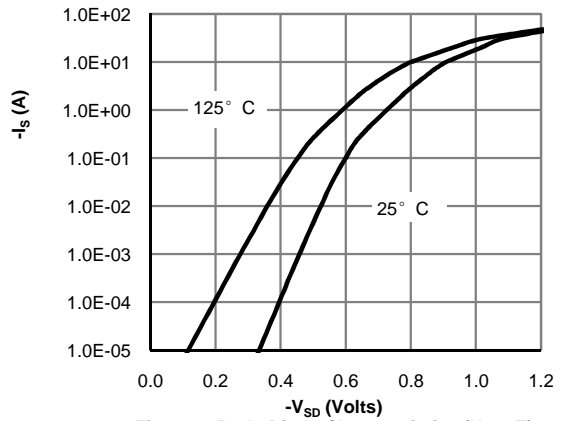**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

Figure 6: Body-Diode Characteristics (Note E)
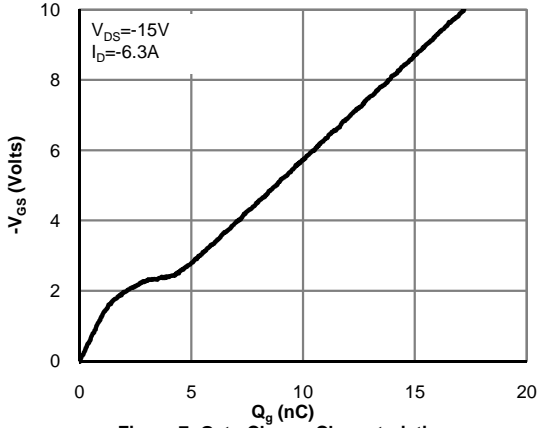
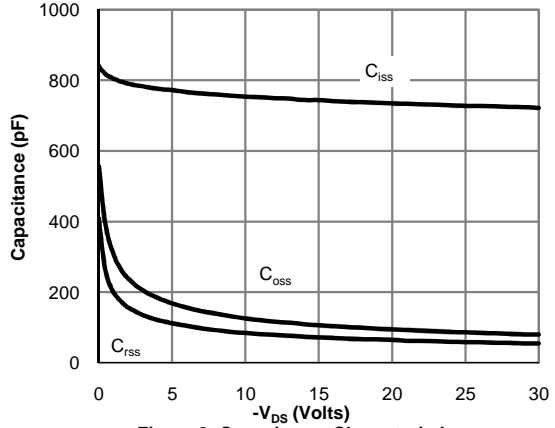## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

V_{DS}=-15V
I_D=-6.3A

Figure 8: Capacitance Characteristics

C_{iss}
C_{oss}
C_{rss}

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

$R_{DS(ON)}$ limited
DC
10μs
100μs
1ms
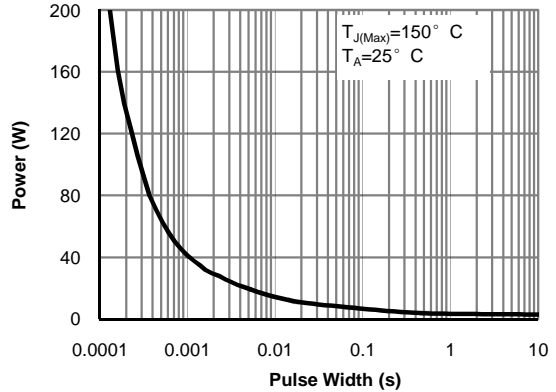10ms
100ms
1s
$T_{J(Max)}$=150°C
T_A=25°C

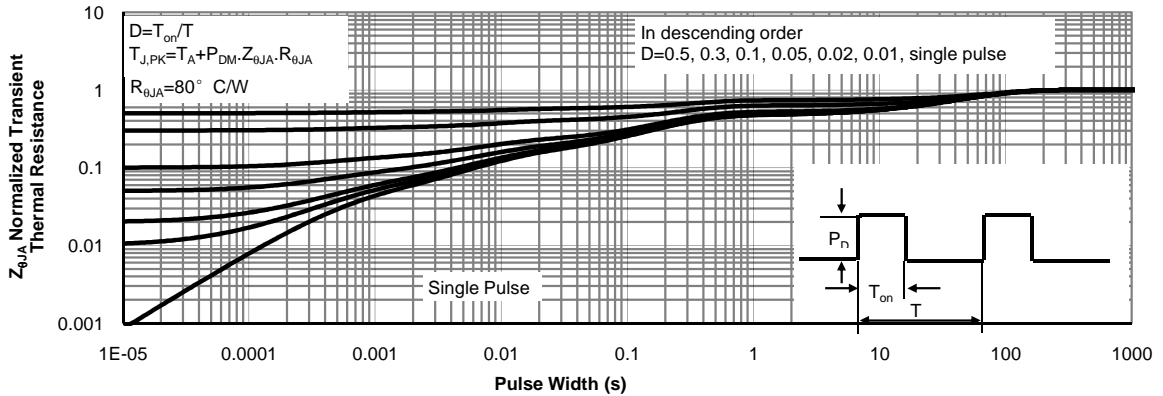**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)**

$T_{J(Max)}$=150°C
T_A=25°C

Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

$D=T_{on}/T$
$T_{J,PK}=T_A+P_{DM}\cdot Z_{\theta JA}\cdot R_{\theta JA}$
$R_{\theta JA}$=80°C/W
In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse
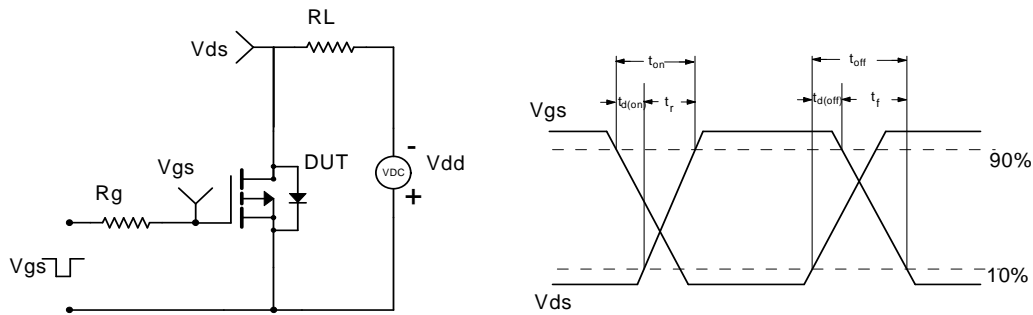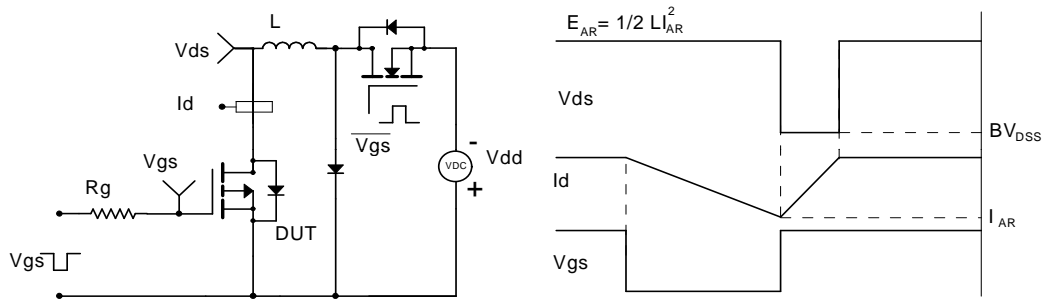Single Pulse

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2\ LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$