

BUJ105AD

Silicon diffused power transistor

Rev. 01 — 14 December 2004

Product data sheet

1. Product profile

1.1 General description

High-voltage, high-speed planar-passivated NPN power switching transistor in a SOT428 (D-PAK) surface mounted package.

1.2 Features

- Low thermal resistance
- Fast switching

1.3 Applications

- Electronic lighting ballast
- DC-to-DC converters
- Inverters
- Motor control systems

1.4 Quick reference data

- $V_{CESM} \leq 700$ V
- $I_C \leq 8$ A
- $P_{tot} \leq 80$ W
- $h_{FEsat} = 11$ (typ)

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	base	<p>SOT428 (D-PAK)</p>	
2	collector ^[1]		
3	emitter		
mb	mounting base; connected to collector		

[1] It is not possible to make a connection to pin 2 of the SOT428 (D-PAK) package.

3. Ordering information

Table 2: Ordering information

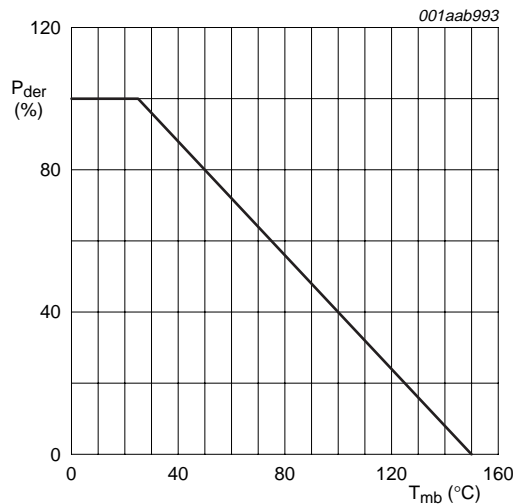
Type number	Package		Version
	Name	Description	
BUJ105AD	D-PAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CESM}	peak collector-emitter voltage	$V_{BE} = 0\text{ V}$	-	700	V
V_{CEO}	collector-emitter voltage	open base	-	400	V
V_{CBO}	collector-base voltage	open emitter	-	700	V
I_C	collector current (DC)		-	8	A
I_{CM}	peak collector current		-	16	A
I_B	base current (DC)		-	4	A
I_{BM}	peak base current		-	8	A
P_{tot}	total power dissipation	$T_{mb} = \leq 25\text{ }^\circ\text{C}$; see Figure 1	-	80	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$



$$P_{der}(\%) = \frac{P_{tot}}{P_{tot(25\text{ }^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 2	-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	75	-	K/W

[1] Device mounted on a printed-circuit board; minimum footprint

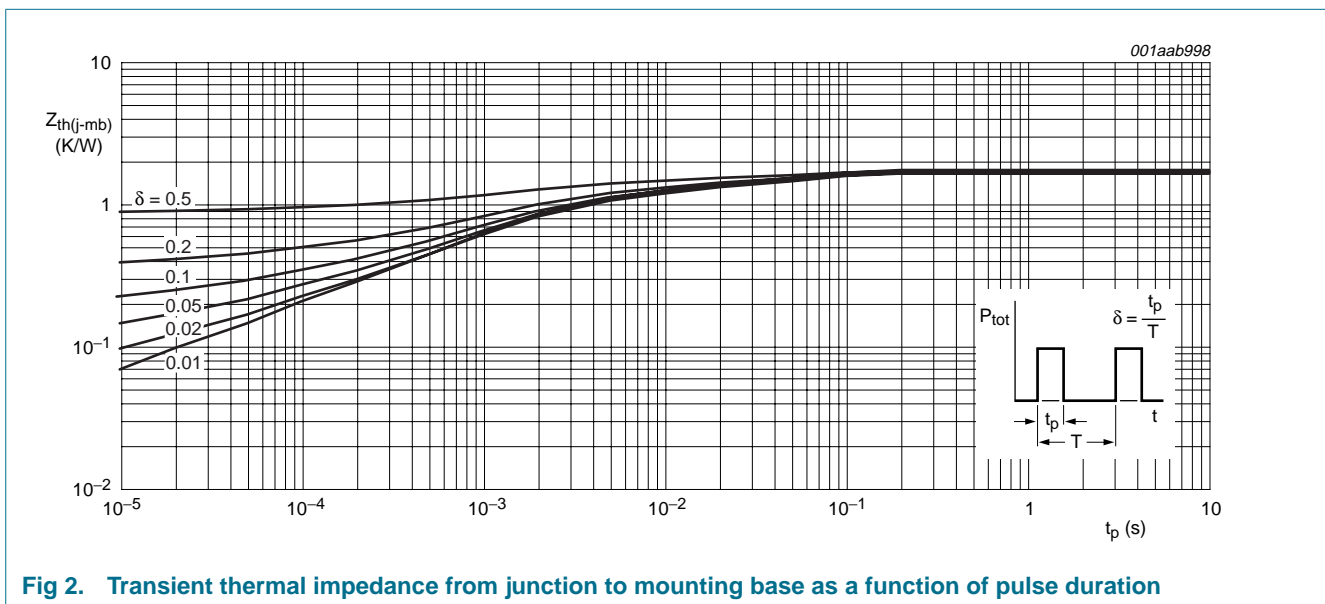


Fig 2. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5: Characteristics

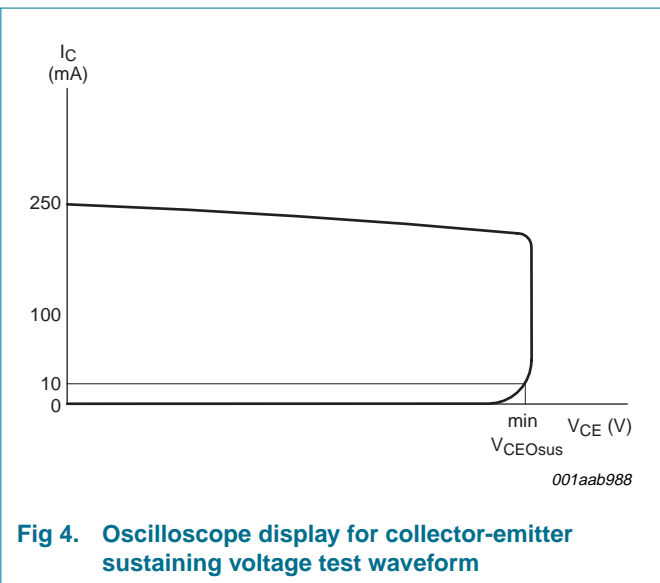
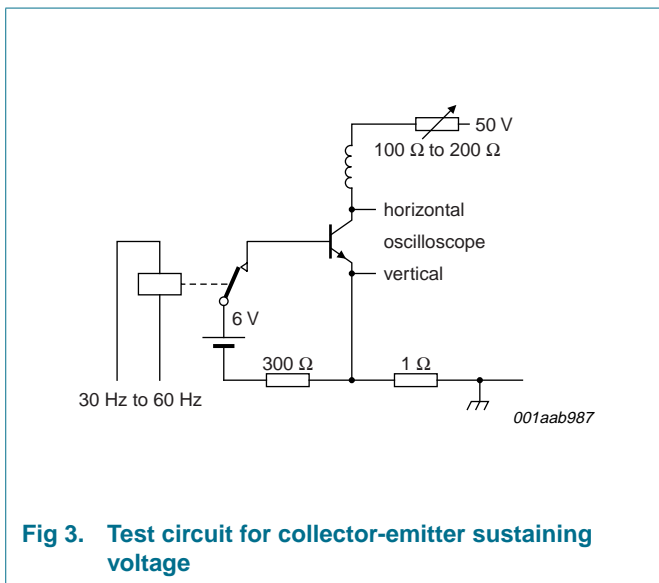
$T_{mb} = 25\text{ }^\circ\text{C}$; unless otherwise specified.

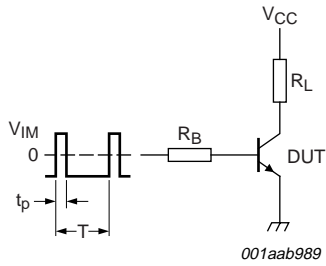
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{CES}	collector-emitter cut-off current	$V_{BE} = 0\text{ V}; V_{CE} = V_{CESMmax}$	[1]	-	0.2	mA
		$V_{BE} = 0\text{ V}; V_{CE} = V_{CESMmax}; T_j = 125\text{ }^\circ\text{C}$	[1]	-	0.5	mA
I_{CBO}	collector-base cut-off current	$V_{BE} = 0\text{ V}; V_{CE} = V_{CESMmax}$	[1]	-	0.2	mA
I_{CEO}	collector-emitter cut-off current	$V_{CEO} = V_{CEOMmax} = 400\text{ V}$	[1]	-	0.1	mA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 9\text{ V}; I_C = 0\text{ A}$	-	-	1	mA
V_{CE0sus}	collector-emitter sustaining voltage	$I_B = 0\text{ A}; I_C = 10\text{ mA}; L = 25\text{ mH}$; see Figure 3 and 4	400	-	-	V
V_{CEsat}	collector-emitter saturation voltage	$I_C = 4.0\text{ A}; I_B = 0.8\text{ A}$; see Figure 11	-	0.3	1.0	V
V_{BEsat}	base-emitter saturation voltage	$I_C = 4.0\text{ A}; I_B = 0.8\text{ A}$; see Figure 12	-	1.0	1.5	V
h_{FE}	DC current gain	$I_C = 1\text{ mA}; V_{CE} = 5\text{ V}$	10	14	34	
		$I_C = 500\text{ mA}; V_{CE} = 5\text{ V}$; see Figure 10	13	23	36	
h_{FEsat}	DC saturation current gain	$I_C = 4.0\text{ A}; V_{CE} = 5\text{ V}$	8	11	15	

Table 5: Characteristics ...continued
 $T_{mb} = 25\text{ }^\circ\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Switching times (resistive load); see Figure 5 and 6						
t_{on}	turn-on time	$I_{Con} = 5\text{ A}$; $I_{Bon} = -I_{Boff} = 1\text{ A}$; $R_L = 75\ \Omega$	-	0.65	1	μs
t_{stg}	storage time		-	1.8	2.5	μs
t_f	fall time		-	0.3	0.5	μs
Switching times (inductive load); see Figure 7 and 8						
t_{stg}	storage time	$I_{Con} = 5\text{ A}$; $I_{Bon} = 1\text{ A}$; $L_B = 1\ \mu\text{H}$;	-	1.2	1.7	μs
t_f	fall time	$V_{BB} = -5\text{ V}$	-	20	50	ns
Switching times (inductive load); see Figure 7 and 8						
t_{stg}	storage time	$I_{Con} = 5\text{ A}$; $I_{Bon} = 1\text{ A}$; $L_B = 1\ \mu\text{H}$;	-	1.4	1.9	μs
t_f	fall time	$V_{BB} = -5\text{ V}$; $T_j = 100\text{ }^\circ\text{C}$	-	25	100	ns

[1] Measured with half sine-wave voltage (curve tracer).





$V_{IM} = -6\text{ V to }+8\text{ V}$; $V_{CC} = 250\text{ V}$; $t_p = 20\text{ }\mu\text{s}$;
 $\delta = t_p/T = 0.01$.
 R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig 5. Test circuit for resistive load switching

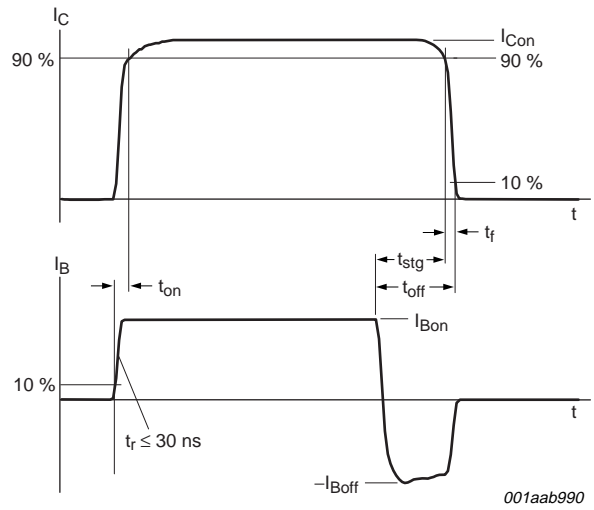
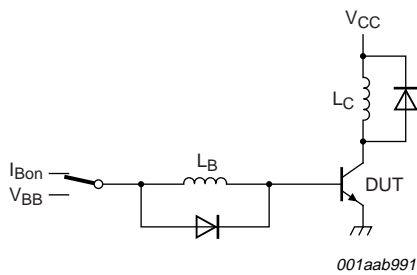


Fig 6. Switching times waveforms for resistive load



$V_{CC} = 300\text{ V}$; $V_{BB} = -5\text{ V}$; $L_C = 200\text{ }\mu\text{H}$; $L_B = 1\text{ }\mu\text{H}$.

Fig 7. Test circuit for inductive load switching

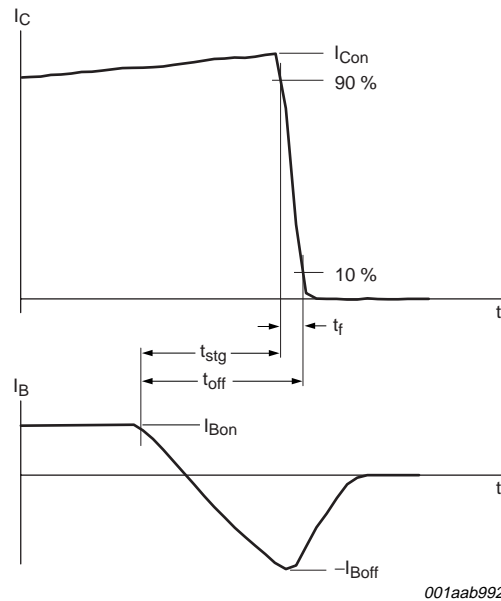


Fig 8. Switching times waveforms for inductive load

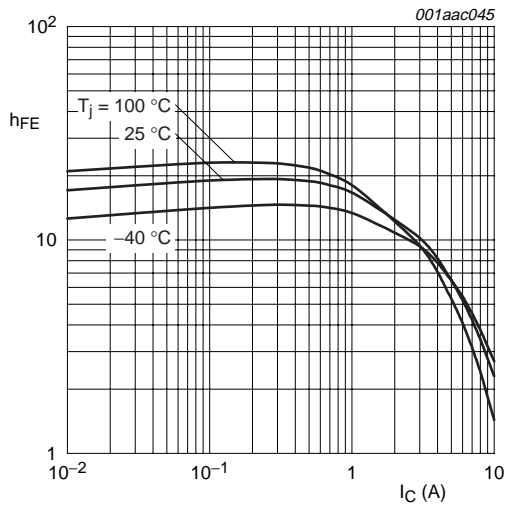


Fig 9. DC current gain as a function of collector current; typical values at $V_{CE} = 1\text{ V}$

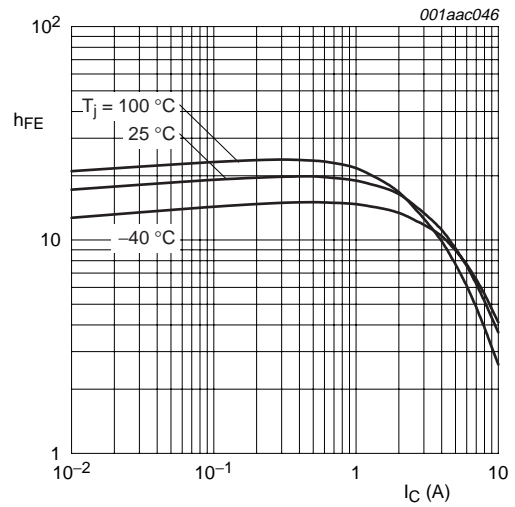
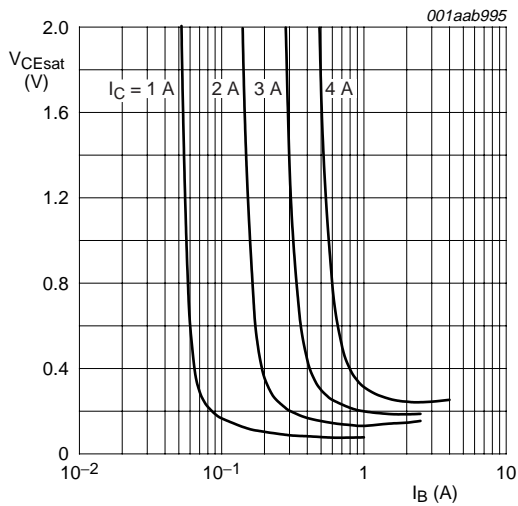
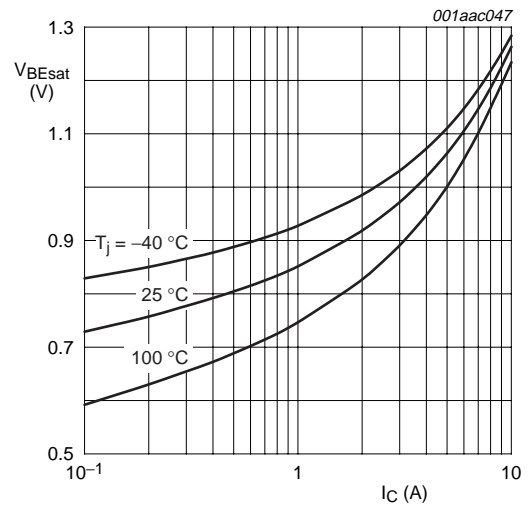


Fig 10. DC current gain as a function of collector current; typical values at $V_{CE} = 5\text{ V}$



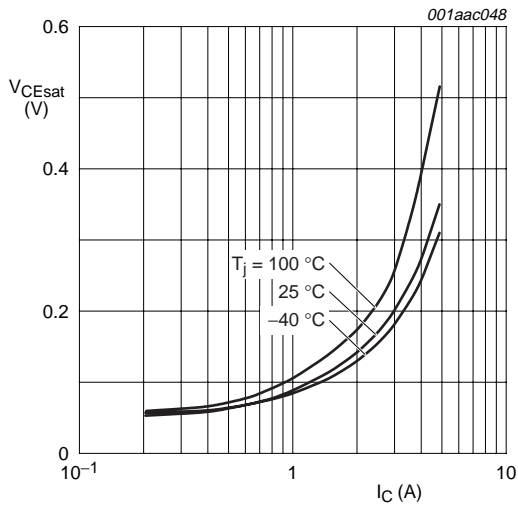
$T_j = 25\text{ °C.}$

Fig 11. Collector-emitter saturation voltage as a function of base current; typical values



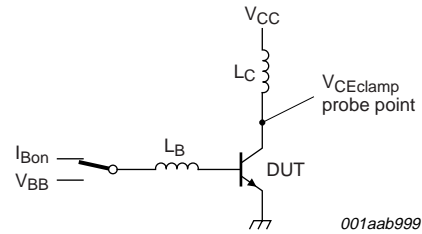
$I_C/I_B = 4.$

Fig 12. Base-emitter saturation voltage as a function of collector current; typical values



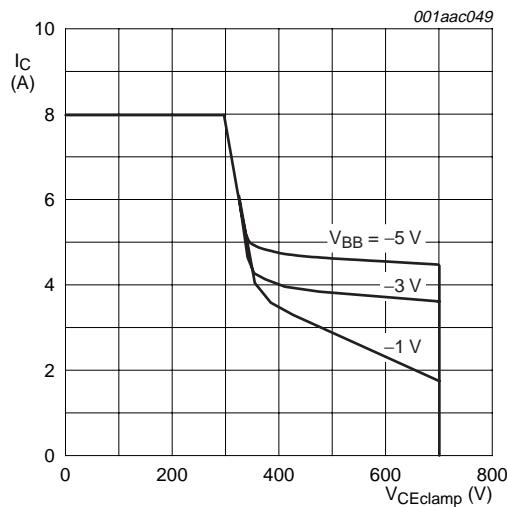
$I_C/I_B = 4$.

Fig 13. Collector-emitter saturation voltage as a function of collector current; typical values



$V_{CEclamp} < 700\text{ V}$; $V_{CC} = 150\text{ V}$; $V_{BB} = -5\text{ V}, -3\text{ V}$ and -1 V ; $L_B = 1\ \mu\text{H}$; $L_C = 200\ \mu\text{H}$.

Fig 14. Test circuit for reverse bias safe operating area



$T_j < T_{j(max)}$.

Fig 15. Reverse bias safe operating area

7. Package information

Epoxy meets requirements of UL94 V-0 at $1/8$ inch.

8. Package outline

Plastic single-ended surface mounted package (D-PAK); 3 leads (one lead cropped)

SOT428

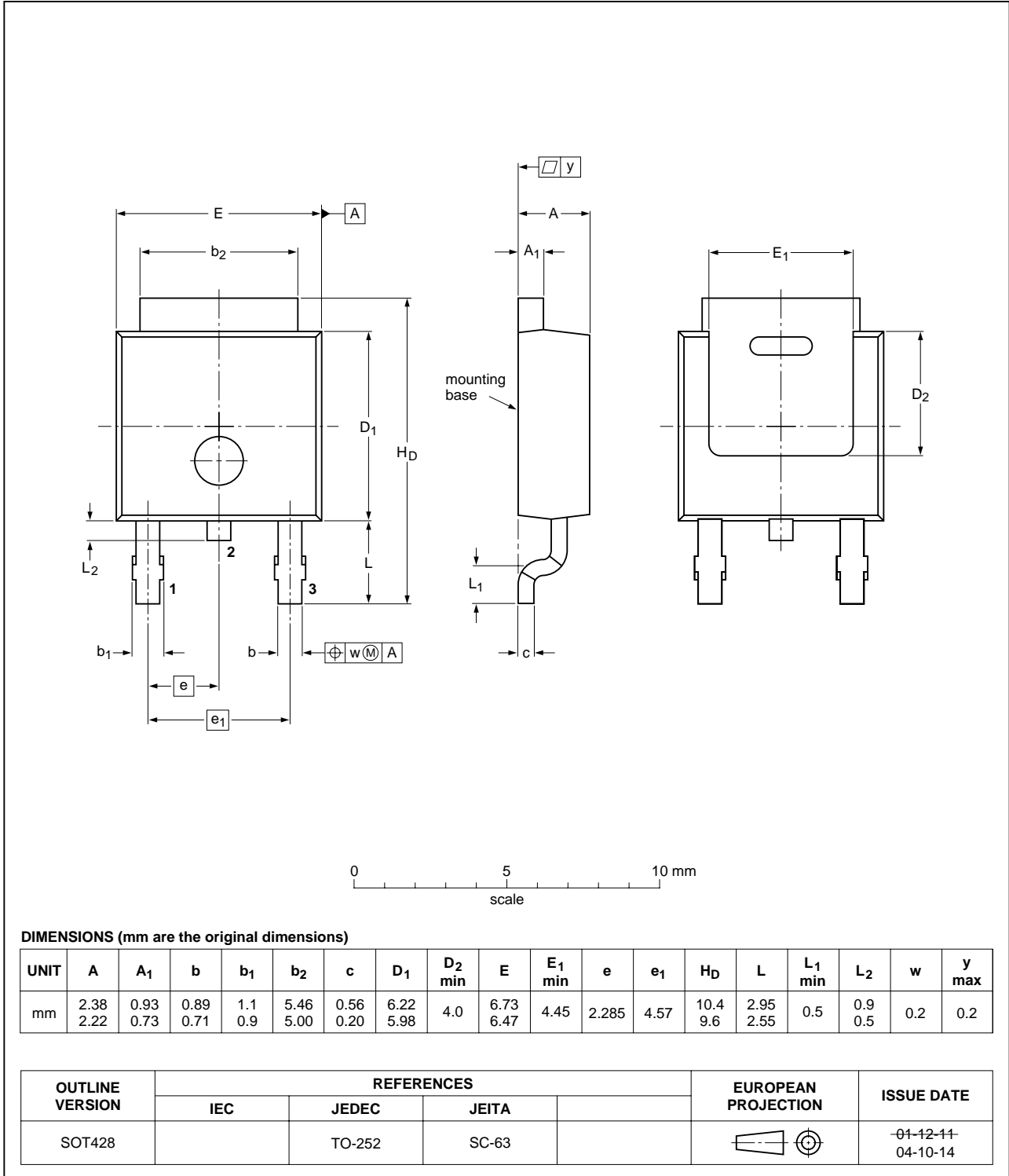
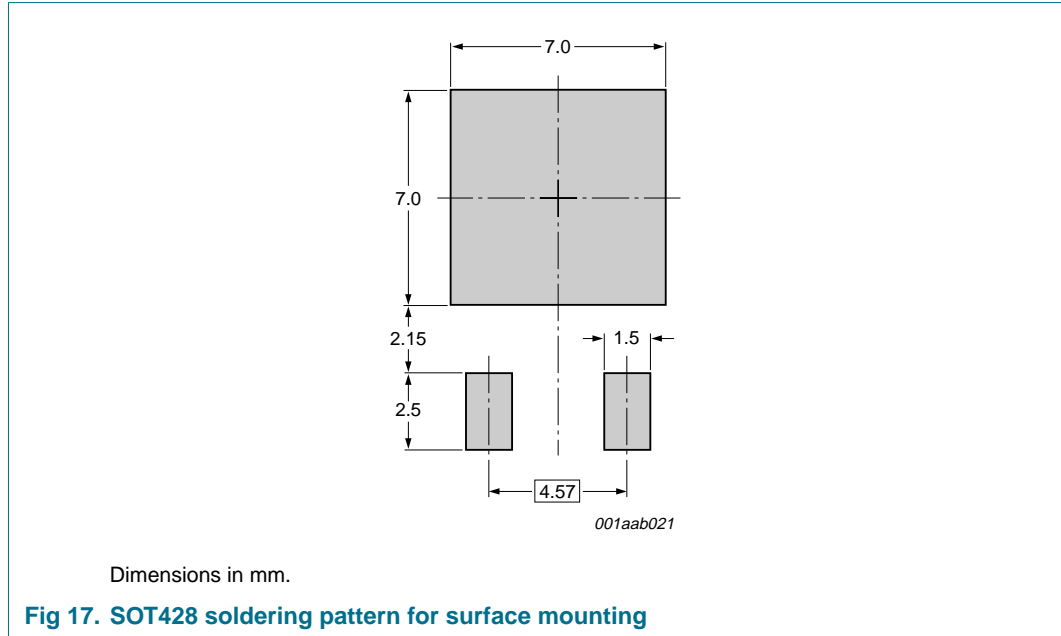


Fig 16. Package outline SOT428 (SC-63)

9. Mounting





10. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BUJ105AD_1	20041214	Product data sheet	-	9397 750 14196	-

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Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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