
HB56UW264DB-6BL/7BL/8BL

2,097,152-word × 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-523B(Z)

Rev.2.0

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Description

The HB56UW264DB is a 2M × 64 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 8 pieces of 16-Mbit DRAM (HM51W17805BLTT) sealed in TSOP package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD).

The HB56UW264DB offers Extended Data Out (EDO) Page Mode as a high speed access mode.

An outline of the HB56UW264DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56UW264DB makes high density mounting possible without surface mount technology. The HB56UW264DB provides common data inputs and outputs.

Decoupling capacitors are mounted beside TSOP on the module board.

Features

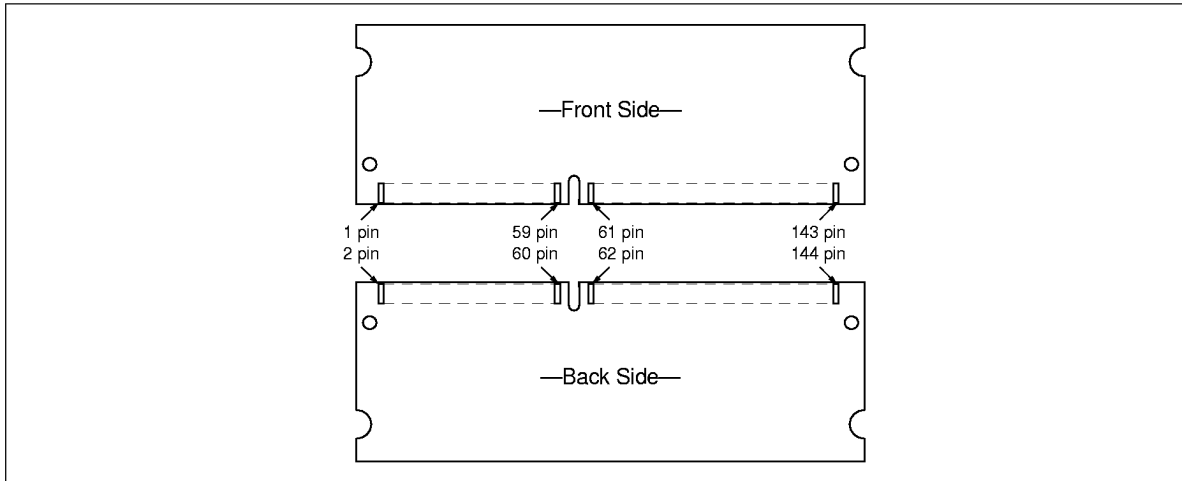
- 144-pin Zig Zag Dual tabs socket type
 - Lead pitch: 0.80 mm
- Single 3.3 V (±0.3 V) supply
- High speed
 - Access time: $t_{RAC} = 60/70/80\text{ns}$ (max)
 - Access time: $t_{CAC} = 15/18/20\text{ns}$ (max)
- Low power dissipation
 - Active mode: 3.46/3.17/2.88 W (max)
 - Standby mode (TTL): 57.6 mW (max)
 - Standby mode (CMOS): 4.32 mW (max)
- EDO mode capability
- 2,048 refresh cycle: 128 ms
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW264DB-6BL	60 ns	Small Outline DIMM (144-pin)	Gold
HB56UW264DB-7BL	70 ns	Small Outline DIMM (144-pin)	Gold
HB56UW264DB-8BL	80 ns	Small Outline DIMM (144-pin)	Gold

Pin Arrangement



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Pin Arrangement

Front Side				Back Side			
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	73	$\overline{\text{OE}}$	2	V _{SS}	74	NC
3	DQ0	75	V _{SS}	4	DQ32	76	V _{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V _{CC}	10	DQ35	82	V _{CC}
11	V _{CC}	83	DQ16	12	V _{CC}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V _{SS}	20	DQ39	92	V _{SS}
21	V _{SS}	93	DQ20	22	V _{SS}	94	DQ52
23	$\overline{\text{CE0}}$	95	DQ21	24	$\overline{\text{CE4}}$	96	DQ53
25	$\overline{\text{CE1}}$	97	DQ22	26	$\overline{\text{CE5}}$	98	DQ54
27	V _{CC}	99	DQ23	28	V _{CC}	100	DQ55
29	A0	101	V _{CC}	30	A3	102	V _{CC}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	NC
35	V _{SS}	107	V _{SS}	36	V _{SS}	108	V _{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10	40	DQ41	112	NC
41	DQ10	113	V _{CC}	42	DQ42	114	V _{CC}
43	DQ11	115	$\overline{\text{CE2}}$	44	DQ43	116	$\overline{\text{CE6}}$
45	V _{CC}	117	$\overline{\text{CE3}}$	46	V _{CC}	118	$\overline{\text{CE7}}$
47	DQ12	119	V _{SS}	48	DQ44	120	V _{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V _{SS}	127	DQ27	56	V _{SS}	128	DQ59
57	NC	129	V _{CC}	58	NC	130	V _{CC}
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	V _{CC}	135	DQ30	64	V _{CC}	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63
67	$\overline{\text{WE}}$	139	V _{SS}	68	NC	140	V _{SS}
69	$\overline{\text{RE0}}$	141	SDA	70	NC	142	SCL
71	NC	143	V _{CC}	72	NC	144	V _{CC}

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Pin Description

Pin Name	Function
A0 to A10	Address Input: A0 to A10 Row Address: A0 to A10 Column Address: A0 to A9 Refresh Address: A0 to A10
DQ0 to DQ63	Data-in/Data-out
$\overline{RE0}$	Row Address Strobe (\overline{RAS})
$\overline{CE0}$ to $\overline{CE7}$	Column Address Strobe (\overline{CAS})
\overline{WE}	Read/Write Enable
\overline{OE}	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
SDA	Serial Data for PD
SCL	Serial Clock for PD
NC	Non Connection

Note: Serial-PD Data are not protected.

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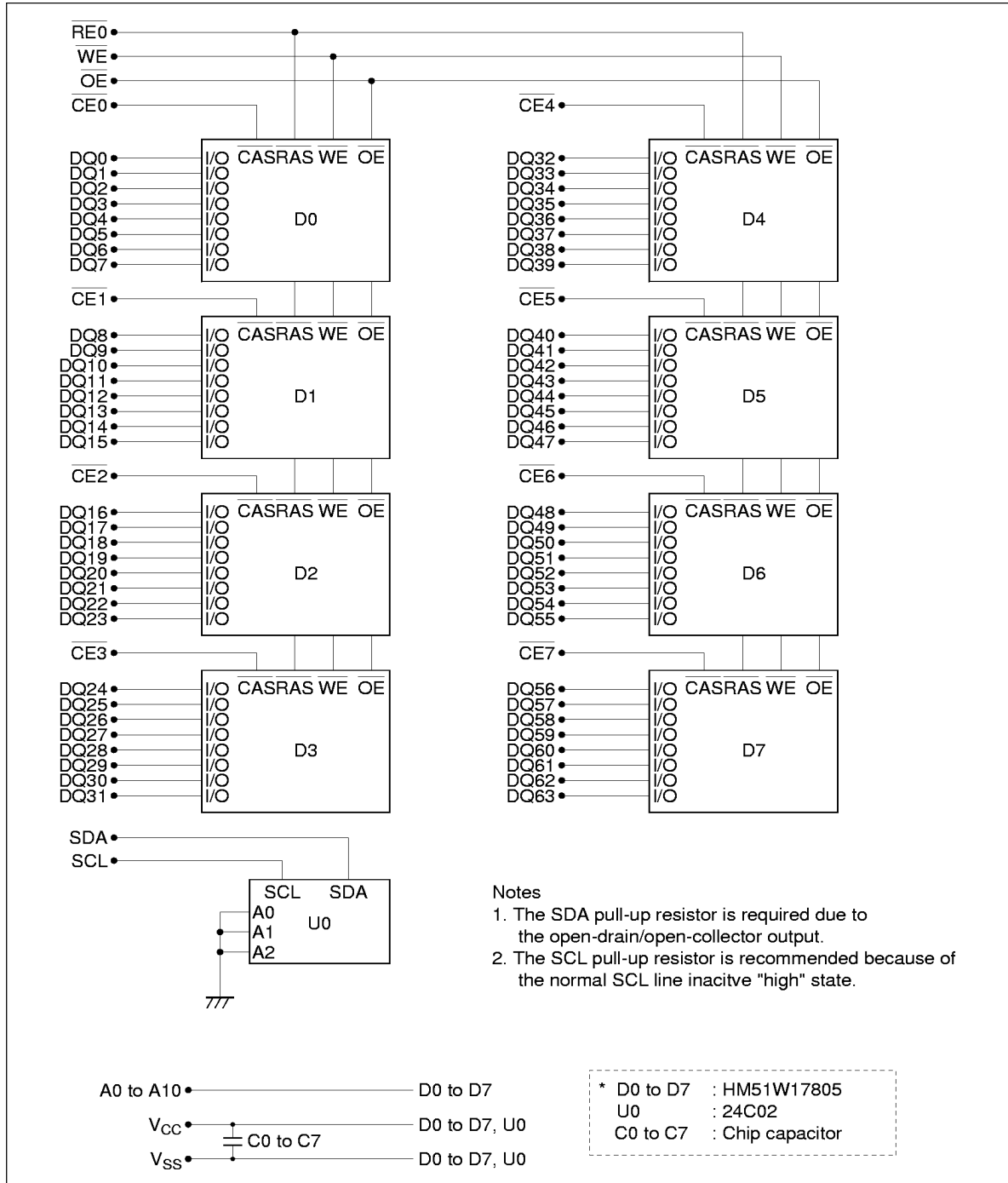
Serial PD Matrix

Byte Number	Function Described	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note
0	Number Serial PD Bytes	0	0	0	0	1	1	0	1	13
1	Serial Memory	0	0	0	0	1	0	0	0	256 Bytes
2	Fundamental Memory Type	0	0	0	0	0	0	1	0	EDO
3	Number of Rows	0	0	0	0	1	0	1	1	11
4	Number of Columns	0	0	0	0	1	0	1	0	10
5	Number of Banks	0	0	0	0	0	0	0	1	1
6	Data Width	0	1	0	0	0	0	0	0	64
7	Data Width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Voltage Interface	0	0	0	0	0	0	0	1	LVTTL (3.3 V)
9	$\overline{\text{RAS}}$ Access Time 60 ns	0	0	1	1	1	1	0	0	
9	$\overline{\text{RAS}}$ Access Time 70 ns	0	1	0	0	0	1	1	0	
9	$\overline{\text{RAS}}$ Access Time 80 ns	0	1	0	1	0	0	0	0	
10	$\overline{\text{CAS}}$ Access Time 15 ns	0	0	0	0	1	1	1	1	
10	$\overline{\text{CAS}}$ Access Time 18 ns	0	0	0	1	0	0	1	0	
10	$\overline{\text{CAS}}$ Access Time 20 ns	0	0	0	1	0	1	0	0	
11	Error Detection/Correction	0	0	0	0	0	0	0	0	None
12	Refresh Period	1	0	0	0	0	1	0	0	Self Refresh (62.5 μs)

Note: 1: High Level (Serial Data)
0: Low Level (Serial Data)

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	8.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

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DC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V)

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Test condition	Note
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	960	—	880	—	800	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	16	—	16	—	16	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
Standby current	I _{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	960	—	880	—	800	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	40	—	40	—	40	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	960	—	880	—	800	mA	t _{RC} = min	
EDO page mode current	I _{CC7}	—	960	—	880	—	800	mA	t _{HPC} = min	1, 3
Battery backup current (Standby with CBR refresh)	I _{CC10}	—	3.2	—	3.2	—	3.2	mA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 62.5 μs t _{RAS} ≤ 0.3 μs	4
Self refresh mode current	I _{CC11}	—	2	—	2	—	2	mA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z	
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while RAS = V_{IL}.
 3. Address can be changed once or less while CAS = V_{IH}.
 4. CAS = L (≤ 0.2 V) while RAS = L (≤ 0.2 V).

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{i1}	—	60	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C_{i2}	—	76	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C_{i3}	—	22	pF	1
I/O capacitance (DQ)	$C_{i/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

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AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *1, *2, *18

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	104	—	124	—	144	—	ns	
RAS precharge time	t _{RP}	40	—	50	—	60	—	ns	
CAS precharge time	t _{CP}	10	—	13	—	15	—	ns	
RAS pulse width	t _{RAS}	60	10000	70	10000	80	10000	ns	
CAS pulse width	t _{CAS}	10	10000	13	10000	15	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	15	—	ns	
RAS to CAS delay time	t _{RCD}	20	45	20	52	20	60	ns	3
RAS to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	4
RAS hold time	t _{RSH}	15	—	18	—	20	—	ns	
CAS hold time	t _{CSH}	48	—	58	—	68	—	ns	
CAS to RAS precharge time	t _{CRP}	5	—	5	—	5	—	ns	
OE to Din delay time	t _{OED}	15	—	18	—	20	—	ns	5
OE delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	6
CAS delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	7
Refresh period (2,048 cycles)	t _{REF}	—	128	—	128	—	128	ms	

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Read Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	—	20	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	—	20	ns	9
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	80	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	28	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	—	15	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	20	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	—	15	ns	
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	20	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	20	—	ns	

Write Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	10	—	13	—	15	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	10	—	13	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	15	—	ns	15

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Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	149	—	175	—	199	—	ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	82	—	95	—	107	—	ns	14
\overline{CAS} to \overline{WE} delay time	t_{CWD}	37	—	43	—	47	—	ns	14
Column address to \overline{WE} delay time	t_{AWD}	52	—	60	—	67	—	ns	14
\overline{OE} hold time from \overline{WE}	t_{OEH}	15	—	18	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
\overline{CAS} setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
\overline{CAS} hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
\overline{WE} setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
\overline{WE} hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	10	—	ns	
\overline{RAS} precharge to \overline{CAS} hold time	t_{RPC}	0	—	0	—	0	—	ns	

EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	25	—	30	—	35	—	ns	19
EDO page mode \overline{RAS} pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from \overline{CAS} precharge	t_{CPA}	—	35	—	40	—	45	ns	9, 17
\overline{RAS} hold time from \overline{CAS} precharge	t_{CPRH}	35	—	40	—	45	—	ns	
Output data hold time from \overline{CAS} low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
\overline{CAS} hold time referred \overline{OE}	t_{COL}	10	—	13	—	15	—	ns	
\overline{CAS} to \overline{OE} setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from \overline{CAS} precharge	t_{RCHC}	35	—	40	—	45	—	ns	

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EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t_{HPRWC}	79	—	90	—	99	—	ns	
$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	t_{CPW}	54	—	62	—	69	—	ns	14

Self-Refresh Cycle

Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ pulse width (self-refresh)	t_{RASS}	100	—	100	—	100	—	μs	
$\overline{\text{RAS}}$ precharge time (self-refresh)	t_{RPS}	110	—	130	—	150	—	ns	
$\overline{\text{CAS}}$ hold time (self-refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	

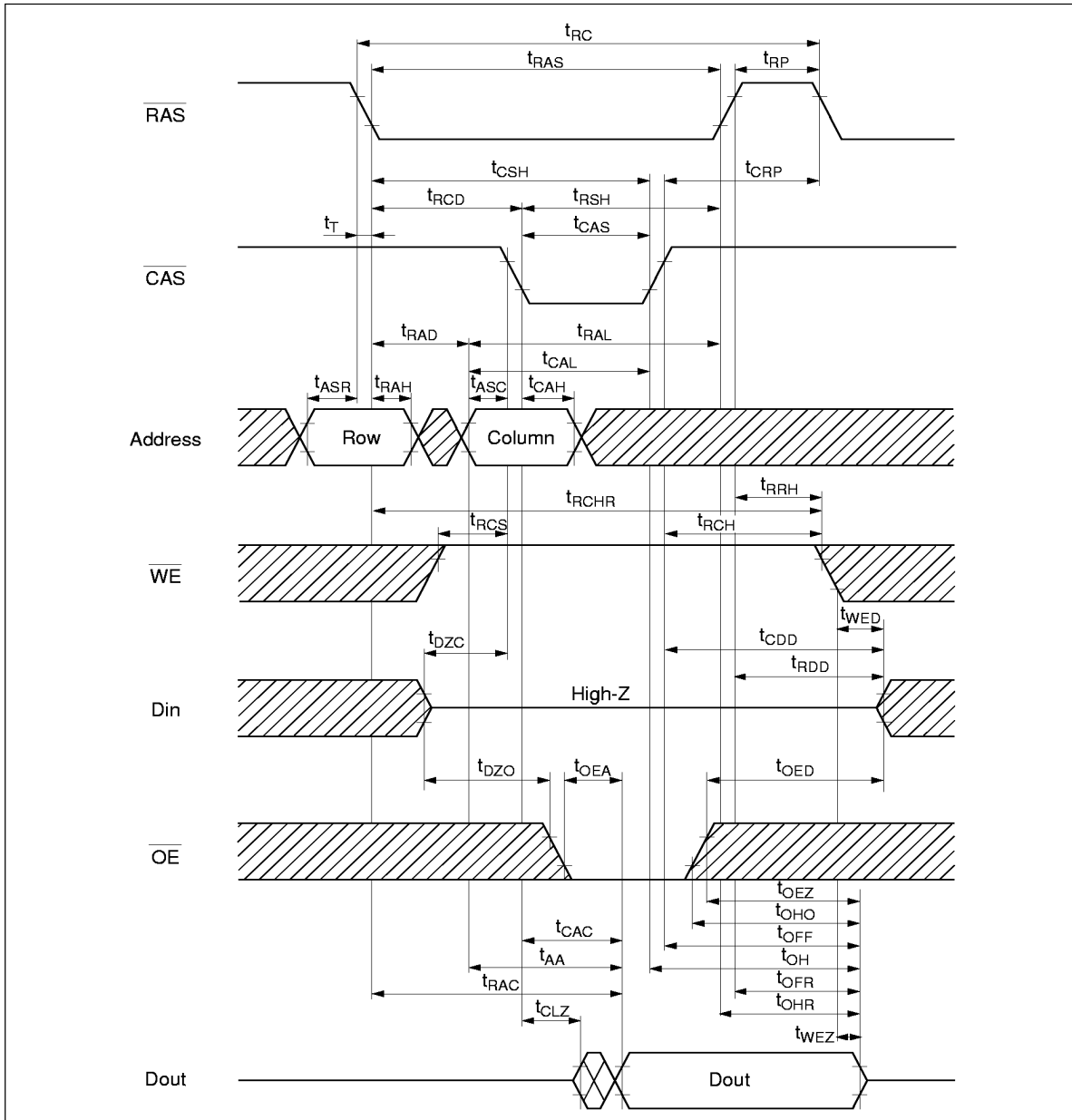
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- Notes:
1. AC measurements assume $t_T = 2 \text{ ns}$.
 2. An initial pause of $200 \mu\text{s}$ is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF .
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max).
 11. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max) and $t_{\text{O EZ}}$ (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), and $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) or $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPW}} \geq t_{\text{CPW}}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. $t_{\text{RAS P}}$ defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the DQ pin will remain open circuit (high impedance); if $t_{\text{OEH}} \leq t_{\text{CWL}}$, invalid data will be out at each DQ.
 19. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).

Timing Waveform

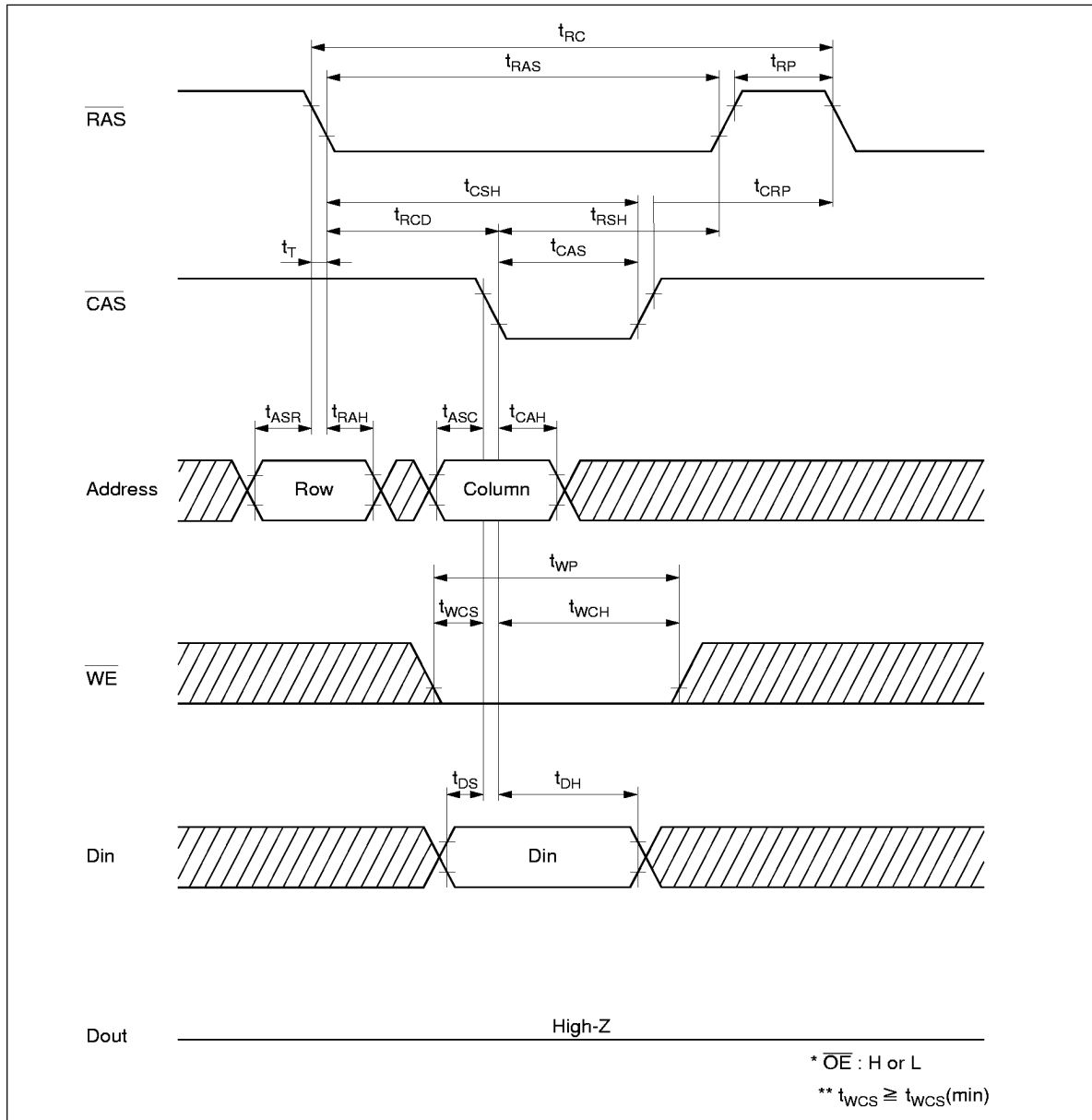
Notes: //: H or L (H: $V_{IH}(\min) \leq V_{in} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{in} \leq V_{IL}(\max)$)
 XXX: Invalid Dout

Read Cycle

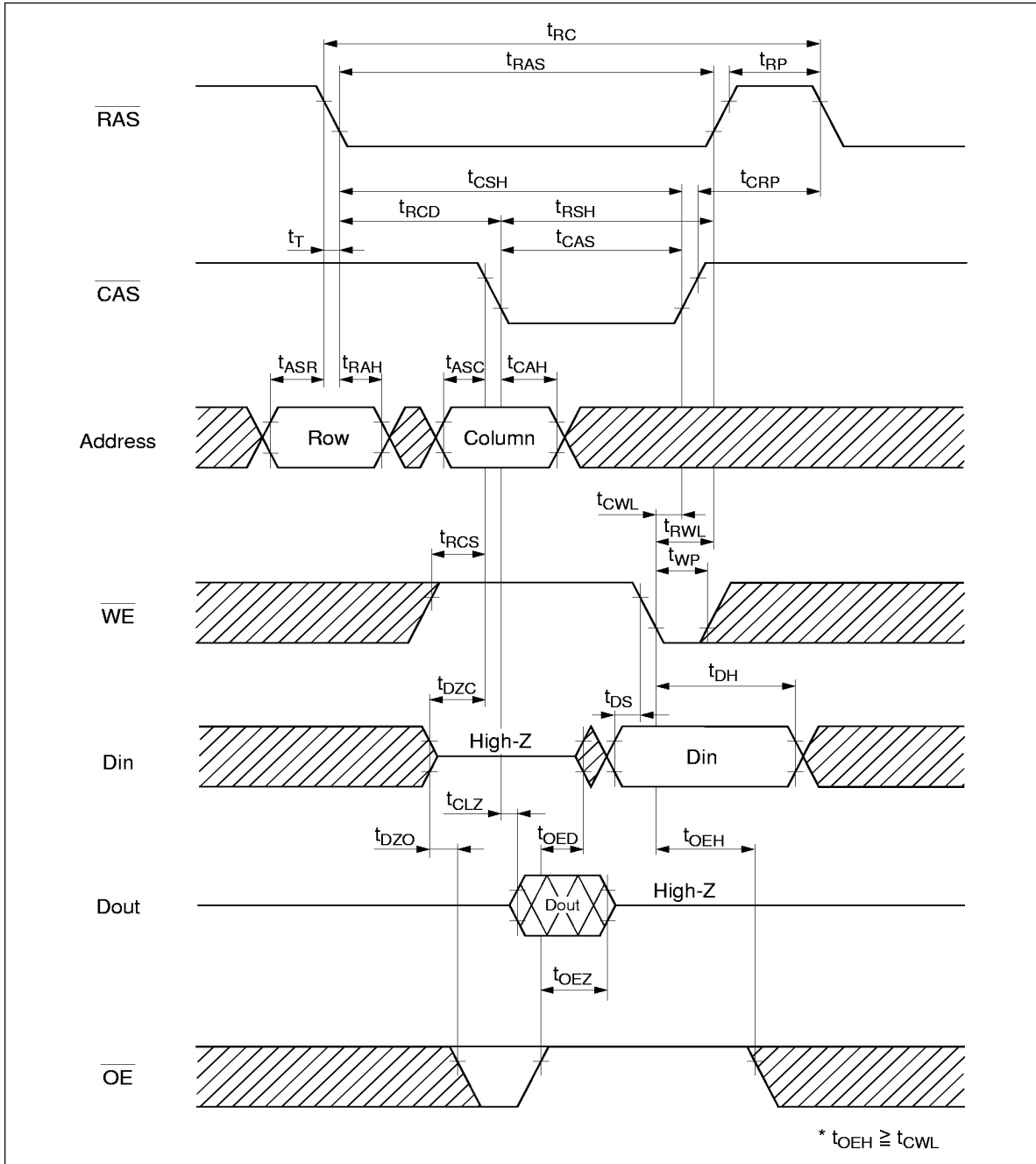


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Early Write Cycle

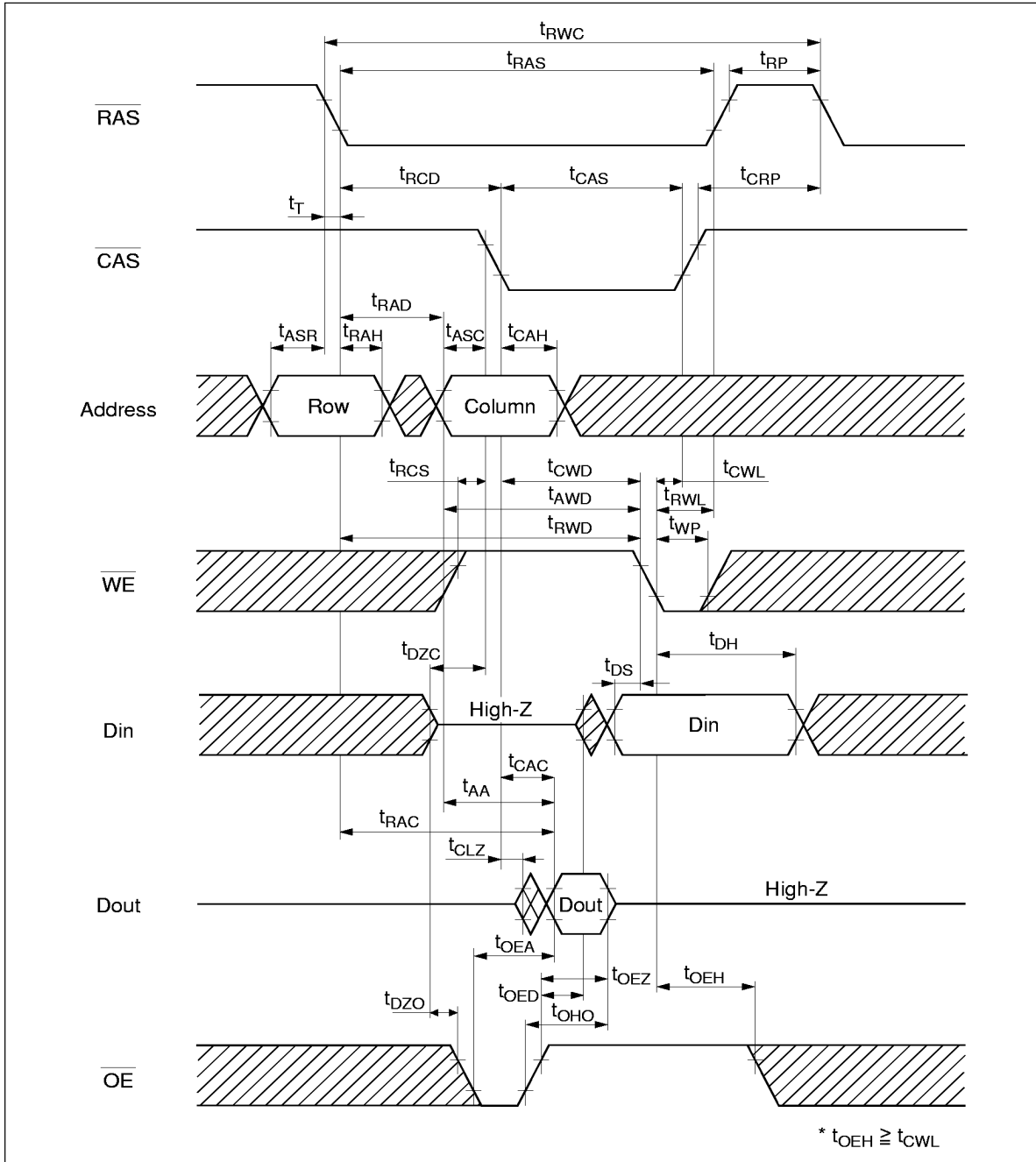


Delay Write Cycle

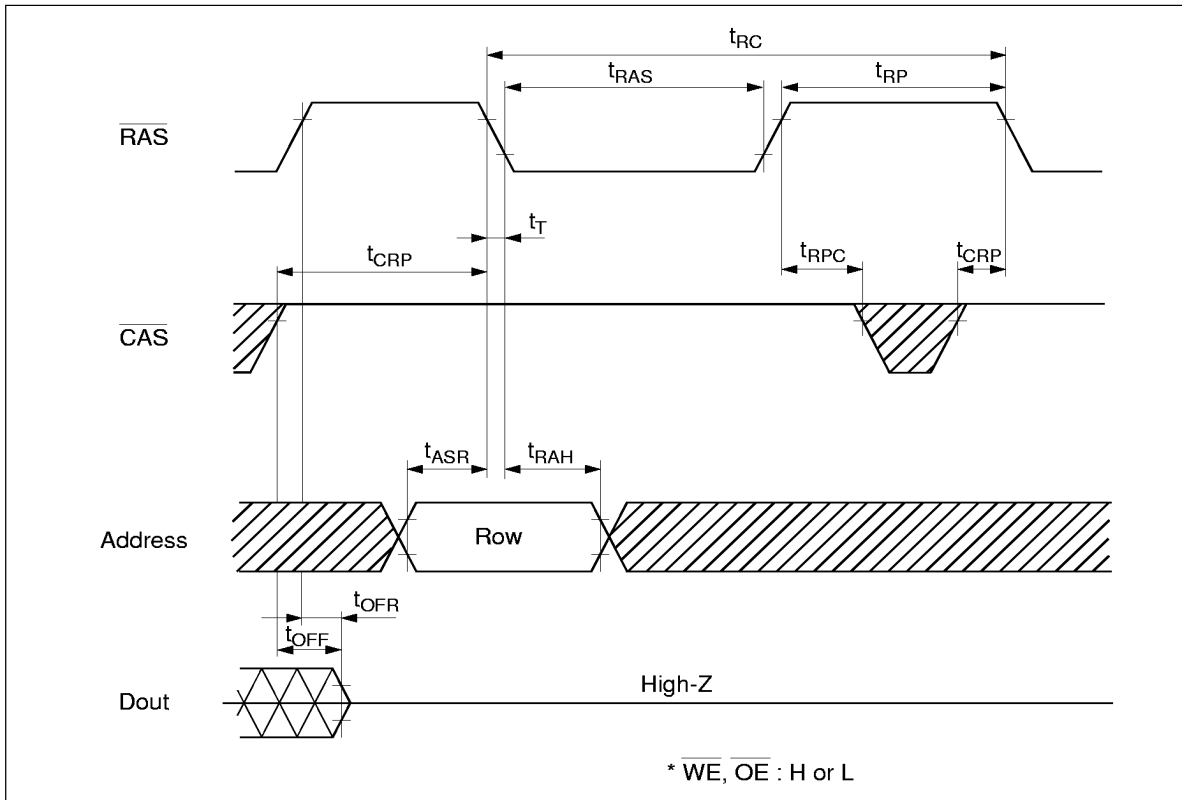


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Read-Modify-Write Cycle

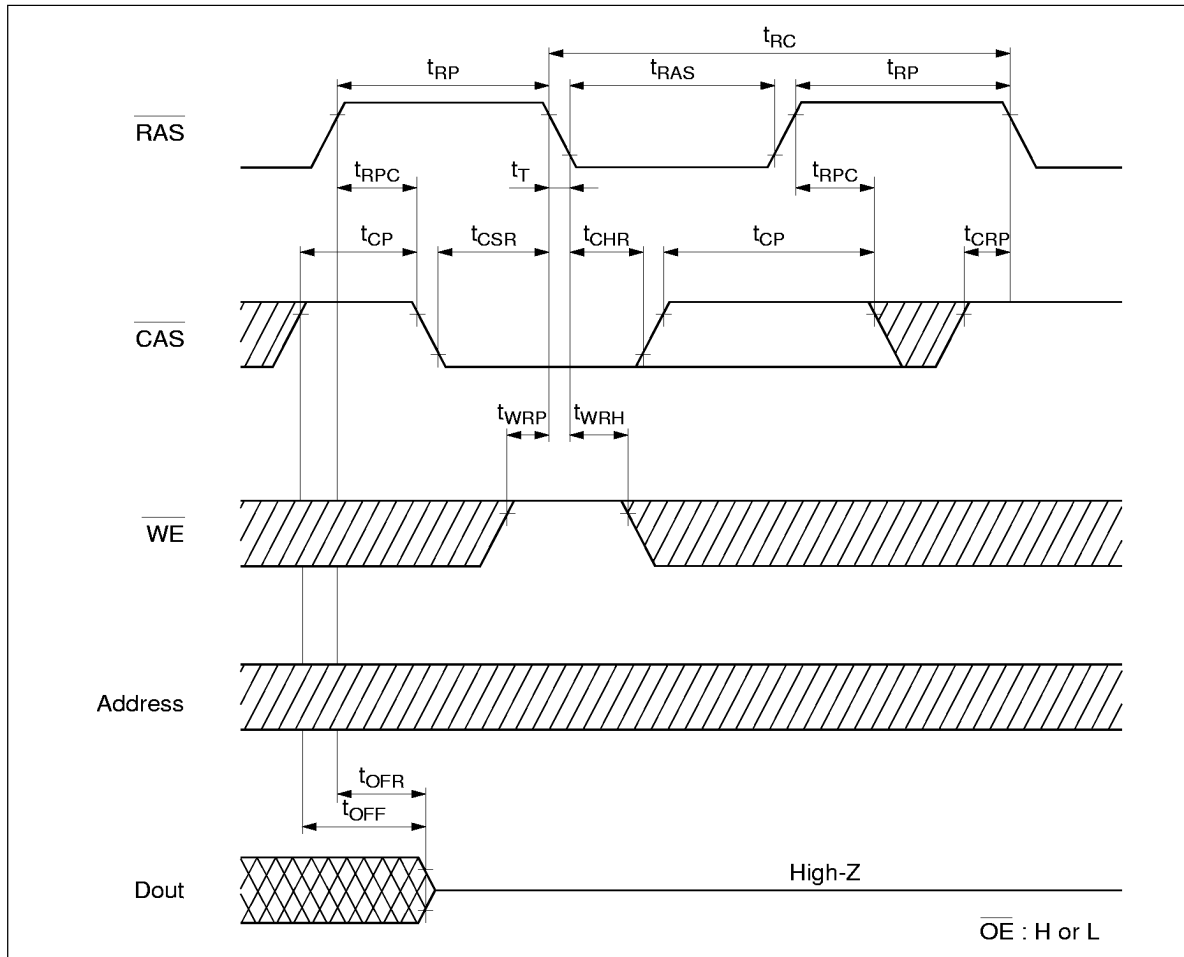


$\overline{\text{RAS}}$ -Only Refresh Cycle

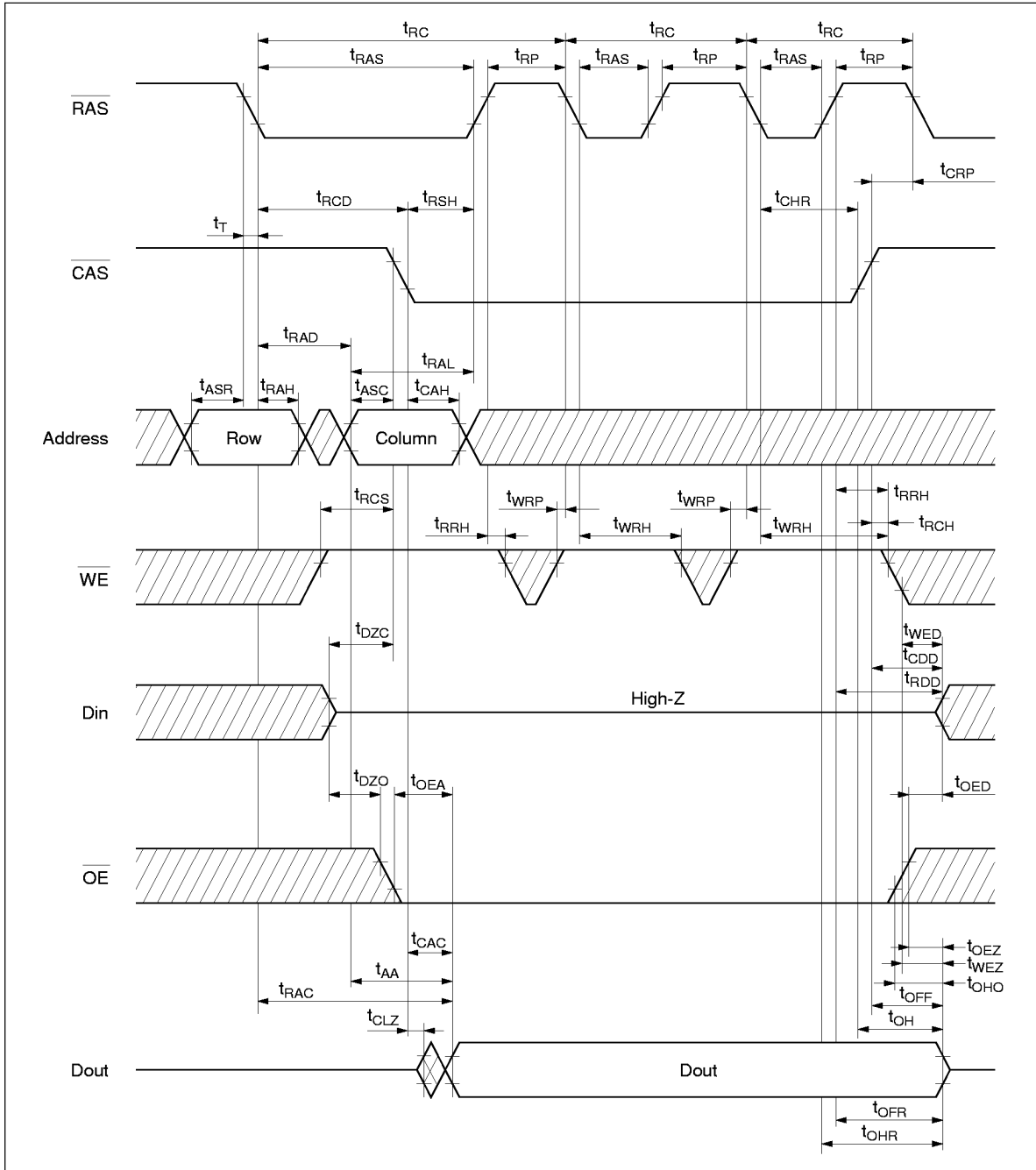


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$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle



Hidden Refresh Cycle

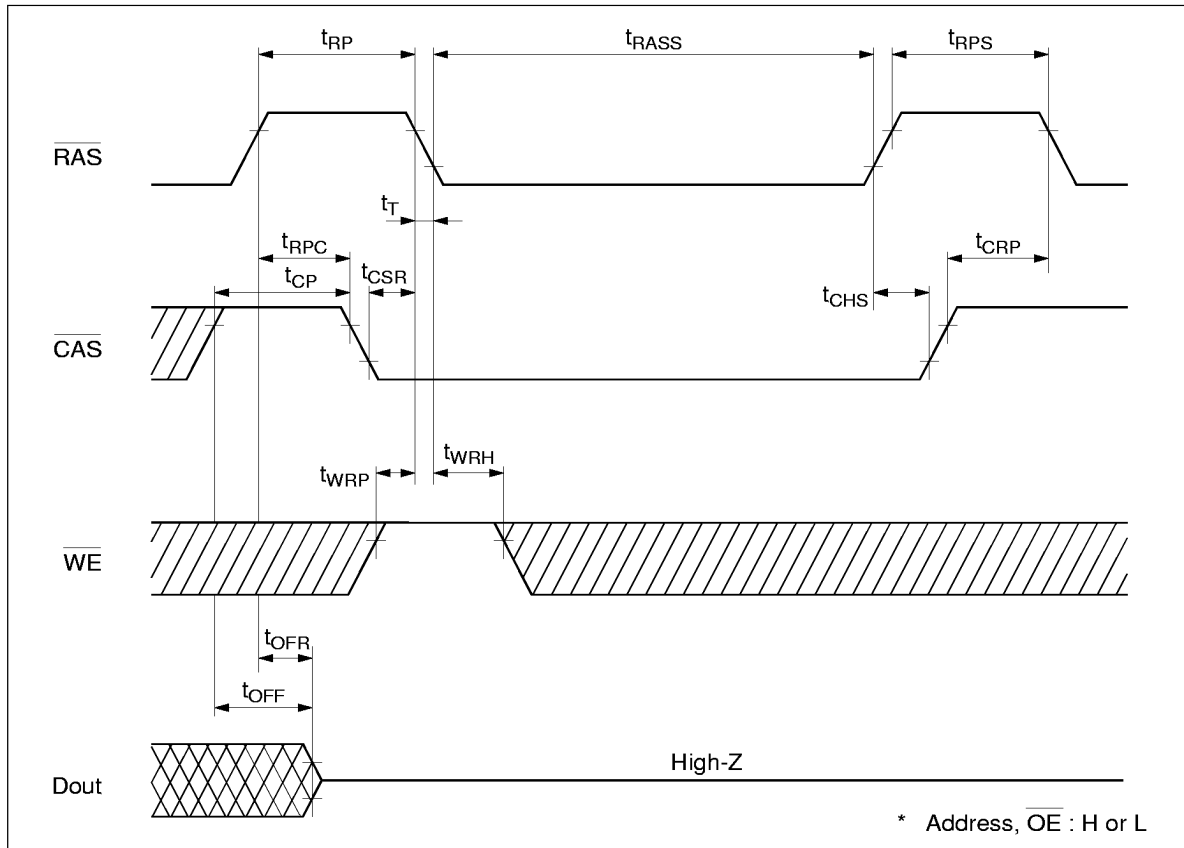


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Self Refresh Cycle

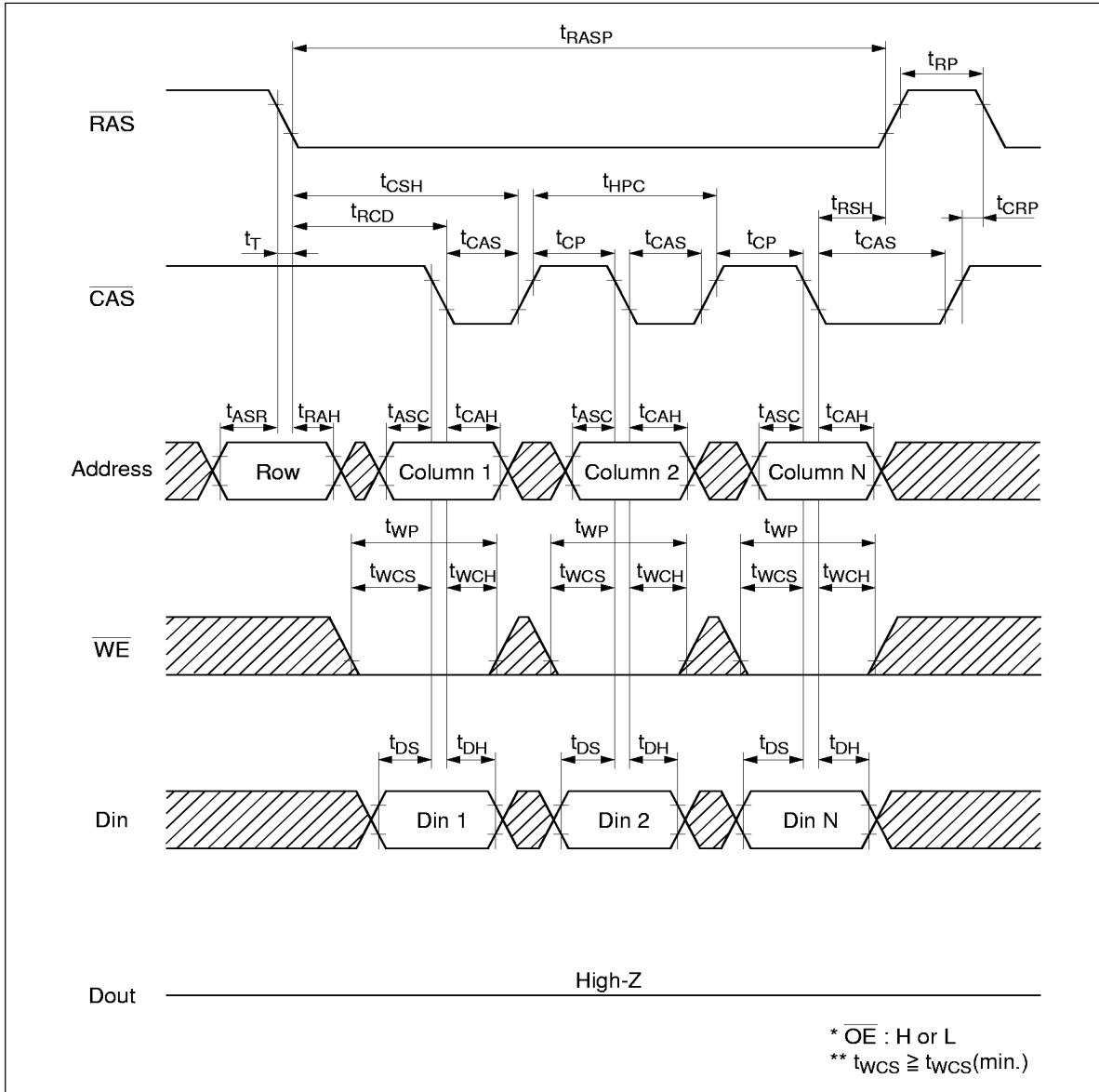
The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then \overline{RAS} precharge time should use t_{RPS} instead of t_{RP} .
2. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read/write cycle, 2048 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

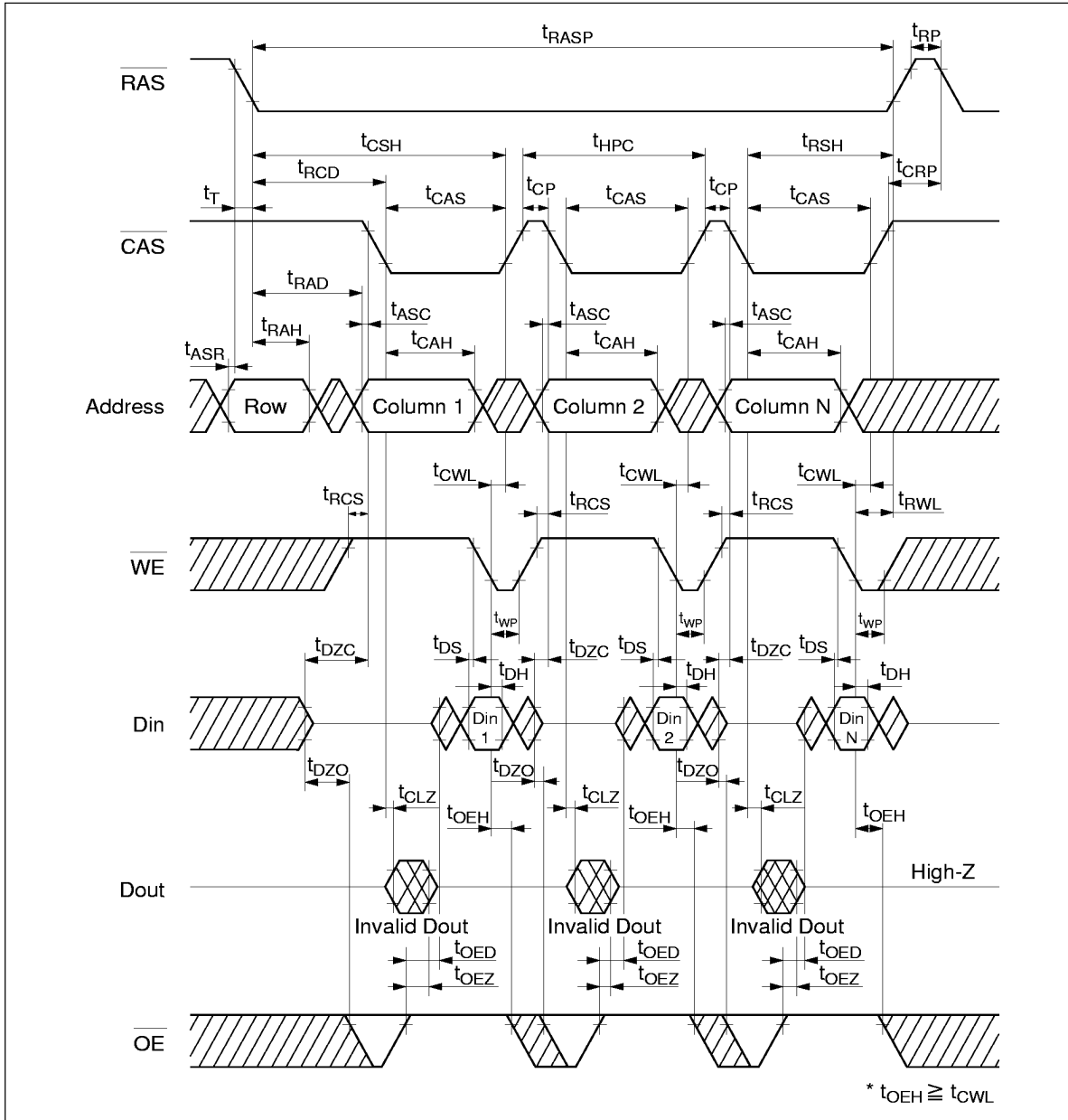


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EDO Page Mode Early Write Cycle

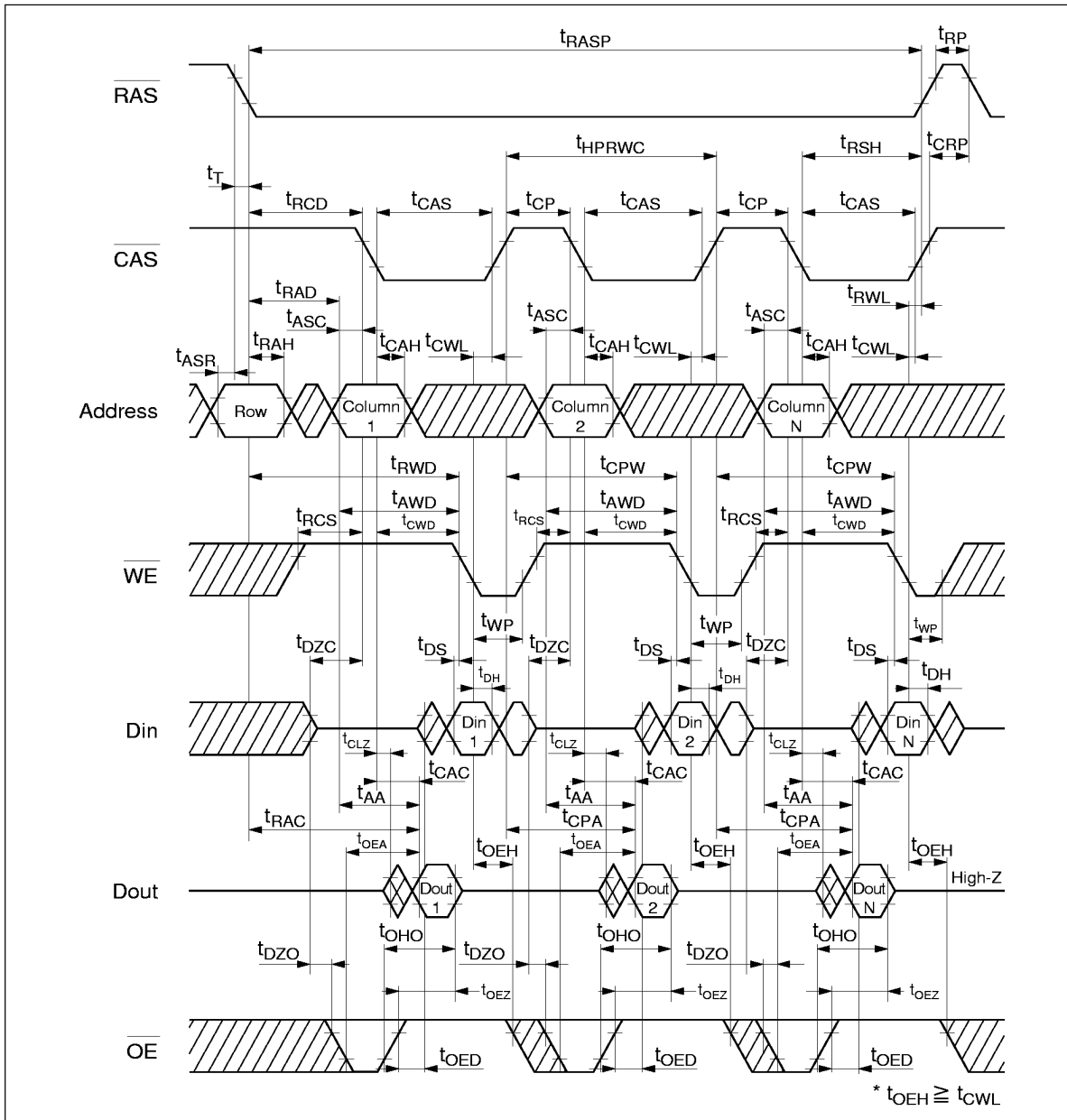


EDO Page Mode Delayed Write Cycle

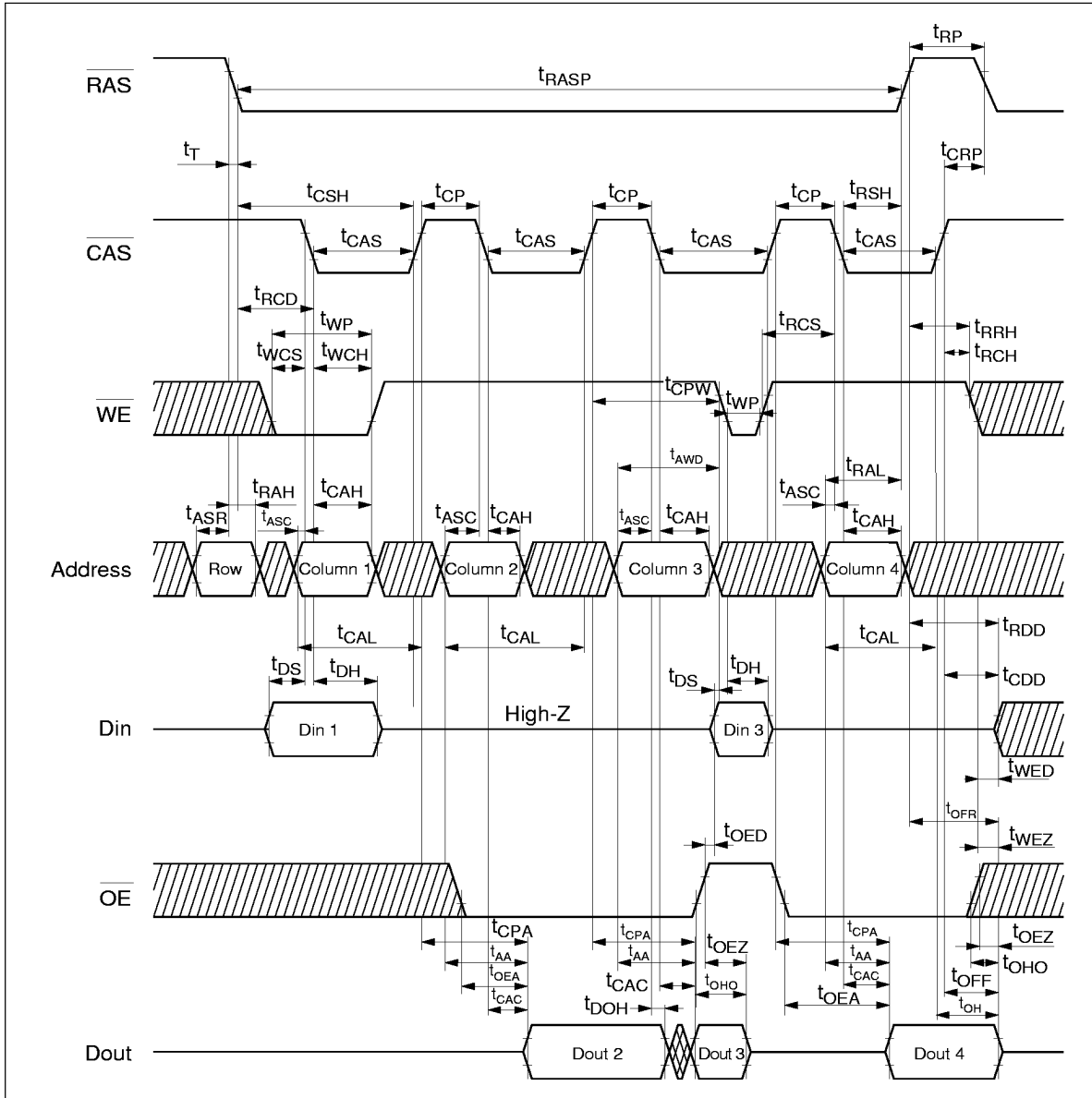


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EDO Page Mode Read-Modify-Write Cycle

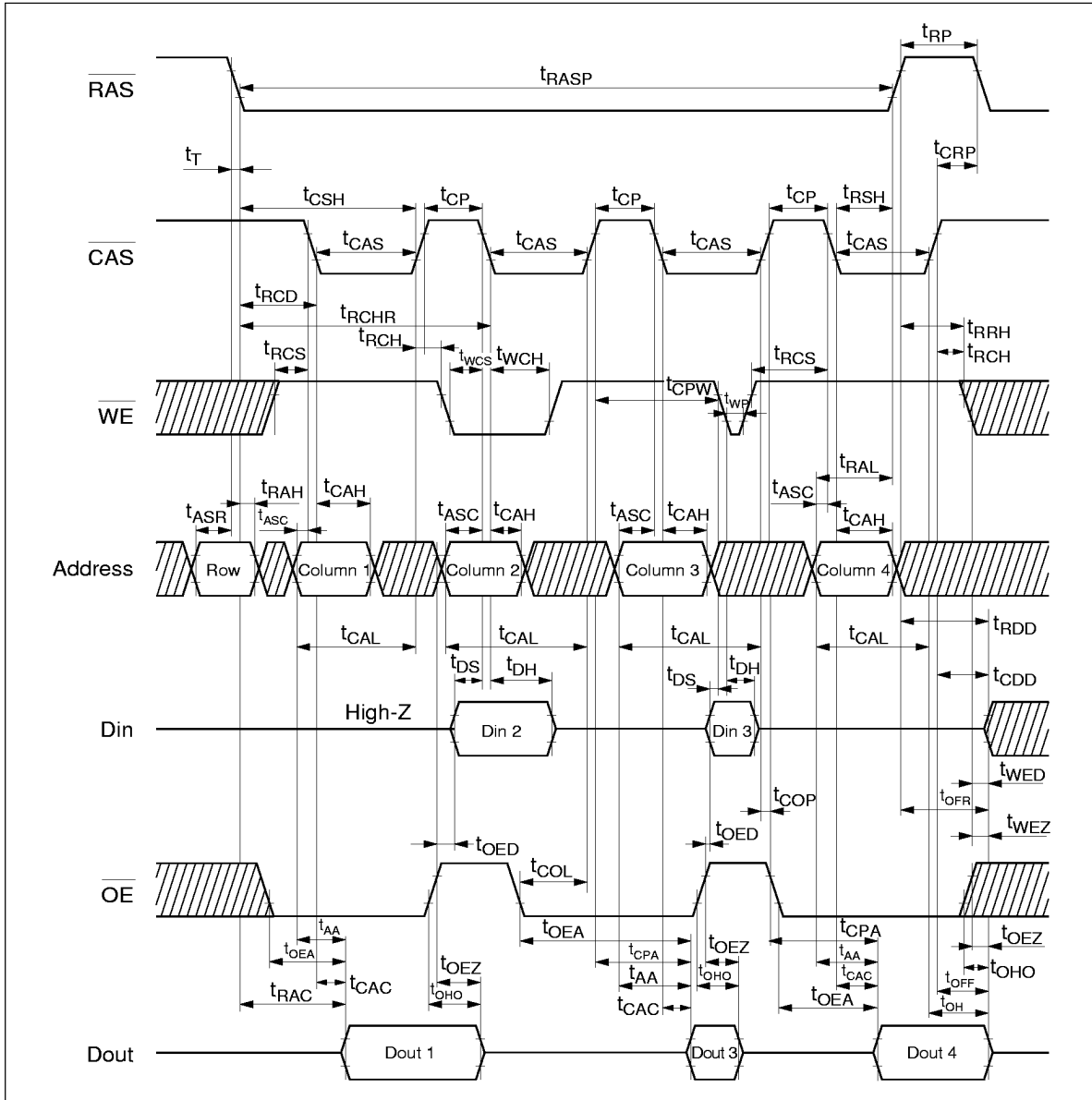


EDO Page Mode Mix Cycle (1)



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EDO Page Mode Mix Cycle (2)



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Physical Outline

Unit: mm/inch

